

## 110 $\mu$ A, High Precision Op Amps

### Features

- Low Offset Voltage:  $\pm 150 \mu\text{V}$  (maximum)
- Low Quiescent Current: 110  $\mu\text{A}$  (typical)
- Rail-to-Rail Input and Output
- Wide Supply Voltage Range: 1.8V to 6.0V
- Gain Bandwidth Product: 1.2 MHz (typical)
- Unity Gain Stable
- Extended Temperature Range:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$
- No Phase Reversal

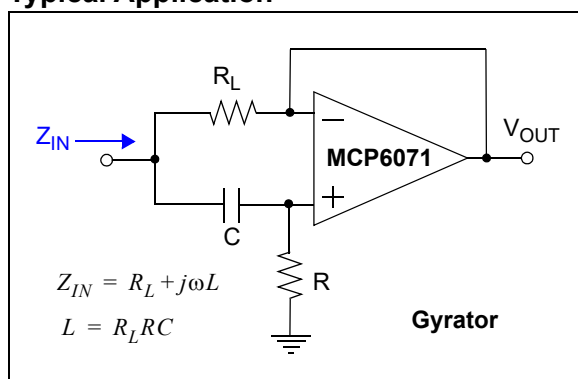
### Applications

- Automotive
- Portable Instrumentation
- Sensor Conditioning
- Battery Powered Systems
- Medical Instrumentation
- Test Equipment
- Analog Filters

### Design Aids

- SPICE Macro Models
- FilterLab<sup>®</sup> Software
- MAPS (Microchip Advanced Part Selector)
- Analog Demonstration and Evaluation Boards
- Application Notes

### Typical Application



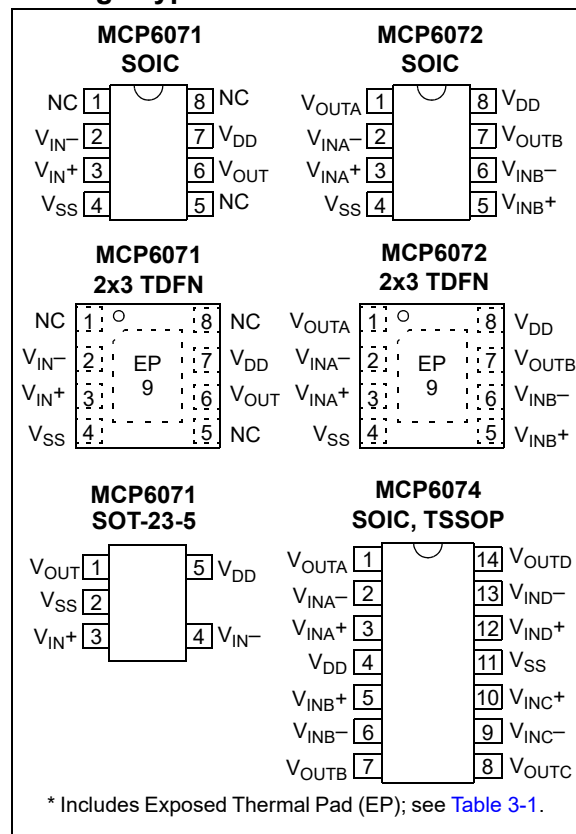
### Description

The Microchip Technology Inc. MCP6071/2/4 family of operational amplifiers (op amps) has low input offset voltage ( $\pm 150 \mu\text{V}$ , maximum) and rail-to-rail input and output operation. This family is unity gain stable and has a gain bandwidth product of 1.2 MHz (typical). These devices operate with a single supply voltage as low as 1.8V, while drawing low quiescent current per amplifier (110  $\mu\text{A}$ , typical). These features make the family of op amps well suited for single-supply, high precision, battery-powered applications.

The MCP6071/2/4 family is offered in single (MCP6071), dual (MCP6072), and quad (MCP6074) configurations.

The MCP6071/2/4 is designed with Microchip's advanced CMOS process. All devices are available in the extended temperature range, with a power supply range of 1.8V to 6.0V.

### Package Types



# MCP6071/2/4

## 1.0 ELECTRICAL CHARACTERISTICS

### 1.1 Absolute Maximum Ratings †

$V_{DD} - V_{SS}$ .....	7.0V
Current at Input Pins .....	$\pm 2$ mA
Analog Inputs ( $V_{IN+}$ , $V_{IN-}$ )†† .....	$V_{SS} - 1.0V$ to $V_{DD} + 1.0V$
All Other Inputs and Outputs .....	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Difference Input Voltage .....	$ V_{DD} - V_{SS} $
Output Short-Circuit Current .....	continuous
Current at Output and Supply Pins .....	$\pm 30$ mA
Storage Temperature .....	$-65^{\circ}C$ to $+150^{\circ}C$
Maximum Junction Temperature ( $T_J$ ) .....	$+150^{\circ}C$
ESD protection on all pins (HBM; MM) .....	$\geq 4$ kV; 400V

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See 4.1.2 “Input Voltage Limits”.

### 1.2 Specifications

TABLE 1-1: DC ELECTRICAL SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated, $V_{DD} = +1.8V$ to $+6.0V$ , $V_{SS} = GND$ , $T_A = +25^{\circ}C$ , $V_{CM} = V_{DD}/2$ , $V_{OUT} \approx V_{DD}/2$ , $V_L = V_{DD}/2$ and $R_L = 10$ k $\Omega$ to $V_L$ . (Refer to Figure 1-1).						
Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Input Offset</b>						
Input Offset Voltage	$V_{OS}$	-150	—	+150	$\mu V$	$V_{DD} = 3.0V$ , $V_{CM} = V_{DD}/3$
Input Offset Drift with Temperature	$\Delta V_{OS}/\Delta T_A$	—	$\pm 1.5$	—	$\mu V/^{\circ}C$	$T_A = -40^{\circ}C$ to $+85^{\circ}C$ , $V_{DD} = 3.0V$ , $V_{CM} = V_{DD}/3$
	$\Delta V_{OS}/\Delta T_A$	—	$\pm 4.0$	—	$\mu V/^{\circ}C$	$T_A = +85^{\circ}C$ to $+125^{\circ}C$ , $V_{DD} = 3.0V$ , $V_{CM} = V_{DD}/3$
Power Supply Rejection Ratio	PSRR	70	87	—	dB	$V_{CM} = V_{SS}$
<b>Input Bias Current and Impedance</b>						
Input Bias Current	$I_B$	—	$\pm 1.0$	100	pA	$T_A = +85^{\circ}C$ $T_A = +125^{\circ}C$
	$I_B$	—	60	—	pA	
	$I_B$	—	1100	5000	pA	
Input Offset Current	$I_{OS}$	—	$\pm 1.0$	—	pA	
Common Mode Input Impedance	$Z_{CM}$	—	$10^{13}  6$	—	$\Omega  pF$	
Differential Input Impedance	$Z_{DIFF}$	—	$10^{13}  6$	—	$\Omega  pF$	
<b>Common Mode</b>						
Common Mode Input Voltage Range	$V_{CMR}$	$V_{SS}-0.15$	—	$V_{DD}+0.15$	V	$V_{DD} = 1.8V$ (Note 1)
	$V_{CMR}$	$V_{SS}-0.3$	—	$V_{DD}+0.3$	V	$V_{DD} = 6.0V$ (Note 1)
Common Mode Rejection Ratio	CMRR	72	89	—	dB	$V_{CM} = -0.15V$ to $1.95V$ , $V_{DD} = 1.8V$
		74	91	—	dB	$V_{CM} = -0.3V$ to $6.3V$ , $V_{DD} = 6.0V$
		72	87	—	dB	$V_{CM} = 3.0V$ to $6.3V$ , $V_{DD} = 6.0V$
		74	89	—	dB	$V_{CM} = -0.3V$ to $3.0V$ , $V_{DD} = 6.0V$

Note 1: Figure 2-13 shows how  $V_{CMR}$  changed across temperature.

**TABLE 1-1: DC ELECTRICAL SPECIFICATIONS (CONTINUED)**

**Electrical Characteristics:** Unless otherwise indicated,  $V_{DD} = +1.8V$  to  $+6.0V$ ,  $V_{SS} = GND$ ,  $T_A = +25^\circ C$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$  and  $R_L = 10\text{ k}\Omega$  to  $V_L$ . (Refer to [Figure 1-1](#)).

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Open-Loop Gain</b>						
DC Open-Loop Gain (Large Signal)	$A_{OL}$	95	115	—	dB	$0.2V < V_{OUT} < (V_{DD}-0.2V)$ $V_{CM} = V_{SS}$
<b>Output</b>						
Maximum Output Voltage Swing	$V_{OL}, V_{OH}$	$V_{SS}+15$	—	$V_{DD}-15$	mV	0.5V input overdrive
Output Short-Circuit Current	$I_{SC}$	—	$\pm 7$	—	mA	$V_{DD} = 1.8V$
		—	$\pm 28$	—	mA	$V_{DD} = 6.0V$
<b>Power Supply</b>						
Supply Voltage	$V_{DD}$	1.8	—	6.0	V	
Quiescent Current per Amplifier	$I_Q$	50	110	170	$\mu A$	$I_O = 0$ , $V_{DD} = 6.0V$ $V_{CM} = 0.9V_{DD}$

**Note 1:** [Figure 2-13](#) shows how  $V_{CMR}$  changed across temperature.

**TABLE 1-2: AC ELECTRICAL SPECIFICATIONS**

**Electrical Characteristics:** Unless otherwise indicated,  $T_A = +25^\circ C$ ,  $V_{DD} = +1.8$  to  $+6.0V$ ,  $V_{SS} = GND$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 60\text{ pF}$ . (Refer to [Figure 1-1](#)).

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>AC Response</b>						
Gain Bandwidth Product	GBWP	—	1.2	—	MHz	
Phase Margin	PM	—	57	—	$^\circ$	$G = +1\text{ V/V}$
Slew Rate	SR	—	0.5	—	$V/\mu s$	
<b>Noise</b>						
Input Noise Voltage	$E_{ni}$	—	4.3	—	$\mu V_{p-p}$	$f = 0.1\text{ Hz to }10\text{ Hz}$
Input Noise Voltage Density	$e_{ni}$	—	19	—	$nV/\sqrt{Hz}$	$f = 10\text{ kHz}$
Input Noise Current Density	$i_{ni}$	—	0.6	—	$fA/\sqrt{Hz}$	$f = 1\text{ kHz}$

**TABLE 1-3: TEMPERATURE SPECIFICATIONS**

**Electrical Characteristics:** Unless otherwise indicated,  $V_{DD} = +1.8V$  to  $+6.0V$  and  $V_{SS} = GND$ .

Parameters	Sym	Min	Typ	Max	Units	Conditions
<b>Temperature Ranges</b>						
Operating Temperature Range	$T_A$	-40	—	+125	$^\circ C$	<a href="#">Note 1</a>
Storage Temperature Range	$T_A$	-65	—	+150	$^\circ C$	
<b>Thermal Package Resistances</b>						
Thermal Resistance, 5L-SOT-23	$\theta_{JA}$	—	220.7	—	$^\circ C/W$	
Thermal Resistance, 8L-2x3 TDFN	$\theta_{JA}$	—	52.5	—	$^\circ C/W$	
Thermal Resistance, 8L-SOIC	$\theta_{JA}$	—	149.5	—	$^\circ C/W$	
Thermal Resistance, 14L-SOIC	$\theta_{JA}$	—	95.3	—	$^\circ C/W$	
Thermal Resistance, 14L-TSSOP	$\theta_{JA}$	—	100	—	$^\circ C/W$	

**Note 1:** The internal junction temperature ( $T_J$ ) must not exceed the absolute maximum specification of  $+150^\circ C$ .

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## 1.3 Test Circuits

The circuit used for most DC and AC tests is shown in [Figure 1-1](#). This circuit can independently set  $V_{CM}$  and  $V_{OUT}$ ; see [Equation 1-1](#). Note that  $V_{CM}$  is not the circuit's common mode voltage ( $(V_P + V_M)/2$ ), and that  $V_{OST}$  includes  $V_{OS}$  plus the effects (on the input offset error,  $V_{OST}$ ) of temperature, CMRR, PSRR and  $A_{OL}$ .

### EQUATION 1-1:

$$G_{DM} = R_F / R_G$$

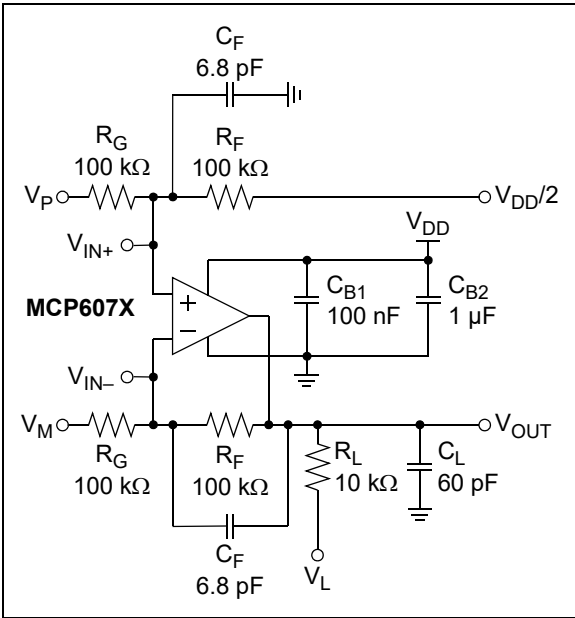
$$V_{CM} = (V_P + V_{DD}/2) / 2$$

$$V_{OST} = V_{IN-} - V_{IN+}$$

$$V_{OUT} = (V_{DD}/2) + (V_P - V_M) + V_{OST}(1 + G_{DM})$$

Where:

$G_{DM}$	= Differential Mode Gain	(V/V)
$V_{CM}$	= Op Amp's Common Mode Input Voltage	(V)
$V_{OST}$	= Op Amp's Total Input Offset Voltage	(mV)



**FIGURE 1-1:** AC and DC Test Circuit for Most Specifications.

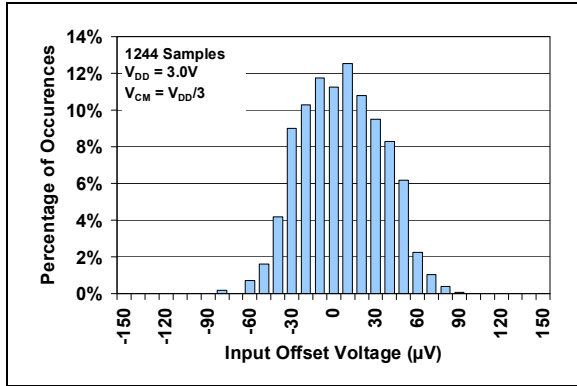
**NOTES:**

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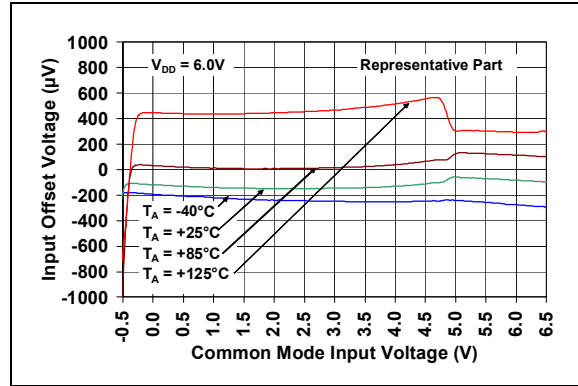
## 2.0 TYPICAL PERFORMANCE CURVES

**Note:** The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

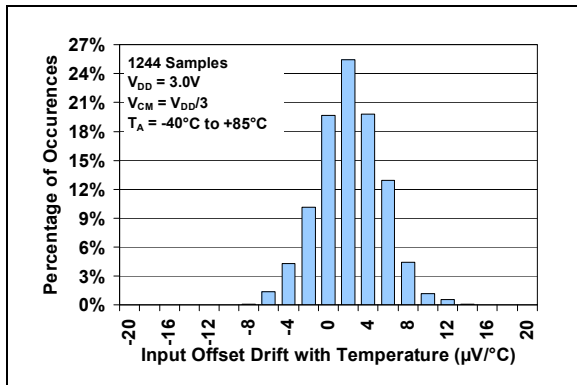
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +1.8\text{V}$  to  $+6.0\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 60\text{ pF}$ .



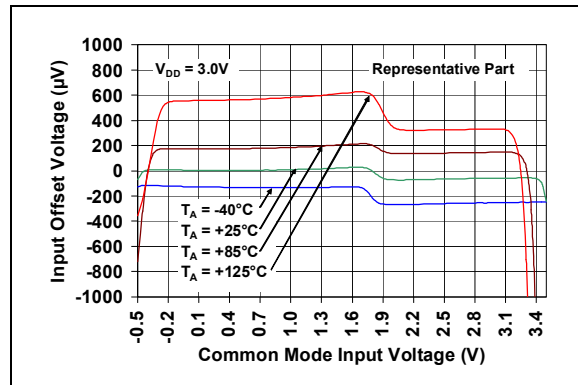
**FIGURE 2-1:** Input Offset Voltage with  $V_{DD} = 3.0\text{V}$ .



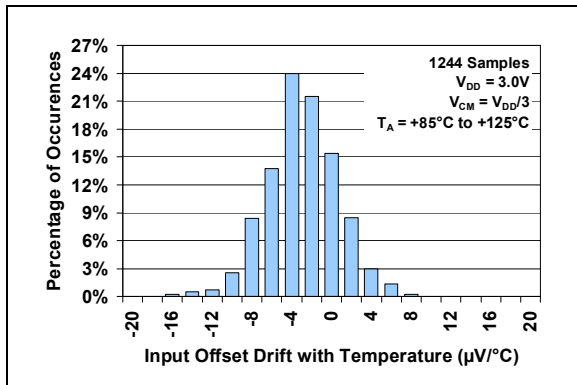
**FIGURE 2-4:** Input Offset Voltage vs. Common Mode Input Voltage with  $V_{DD} = 6.0\text{V}$ .



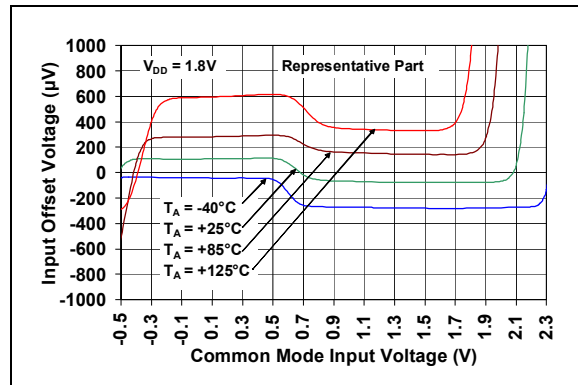
**FIGURE 2-2:** Input Offset Voltage Drift with  $V_{DD} = 3.0\text{V}$  and  $T_A \leq +85^\circ\text{C}$ .



**FIGURE 2-5:** Input Offset Voltage vs. Common Mode Input Voltage with  $V_{DD} = 3.0\text{V}$ .

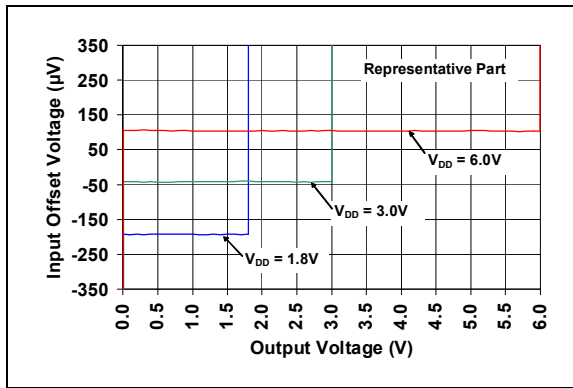


**FIGURE 2-3:** Input Offset Voltage Drift with  $V_{DD} = 3.0\text{V}$  and  $T_A \geq +85^\circ\text{C}$ .

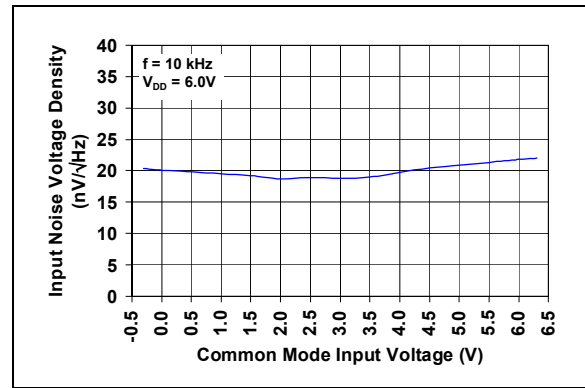


**FIGURE 2-6:** Input Offset Voltage vs. Common Mode Input Voltage with  $V_{DD} = 1.8\text{V}$ .

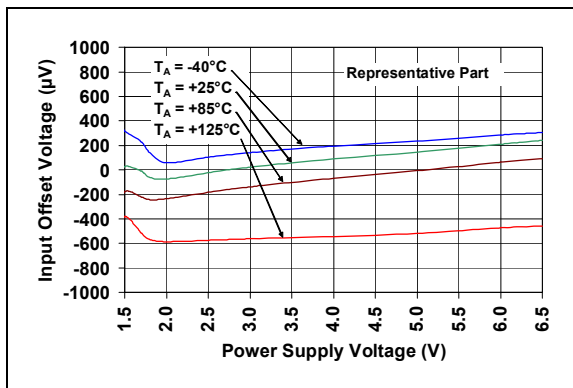
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +1.8\text{V}$  to  $+6.0\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 60\text{ pF}$ .



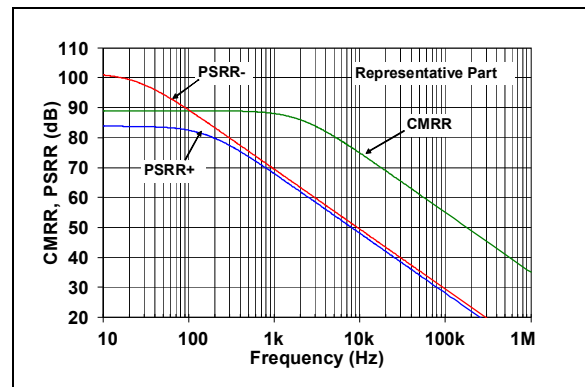
**FIGURE 2-7:** Input Offset Voltage vs. Output Voltage.



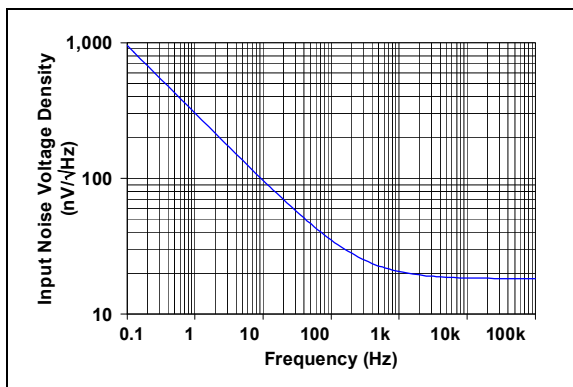
**FIGURE 2-10:** Input Noise Voltage Density vs. Common Mode Input Voltage.



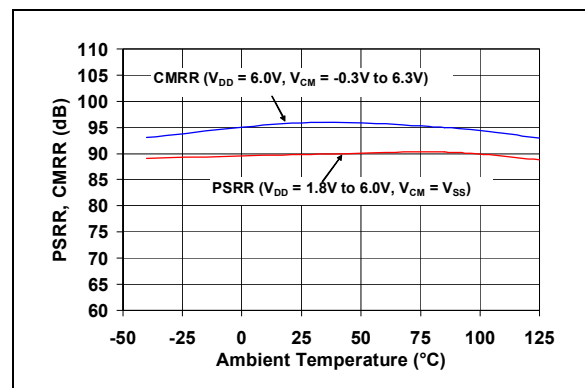
**FIGURE 2-8:** Input Offset Voltage vs. Power Supply Voltage.



**FIGURE 2-11:** CMRR, PSRR vs. Frequency.



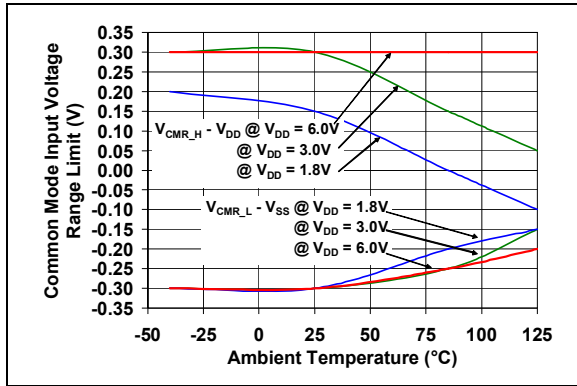
**FIGURE 2-9:** Input Noise Voltage Density vs. Frequency.



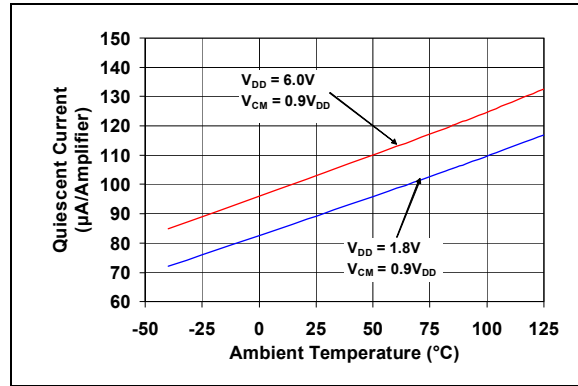
**FIGURE 2-12:** CMRR, PSRR vs. Ambient Temperature.

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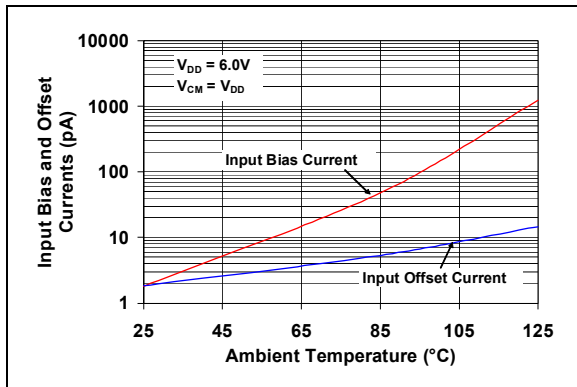
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +1.8\text{V}$  to  $+6.0\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 60\text{ pF}$ .



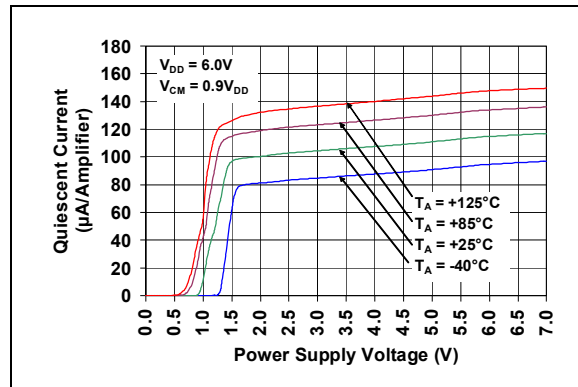
**FIGURE 2-13:** Common Mode Input Voltage Range Limit vs. Ambient Temperature.



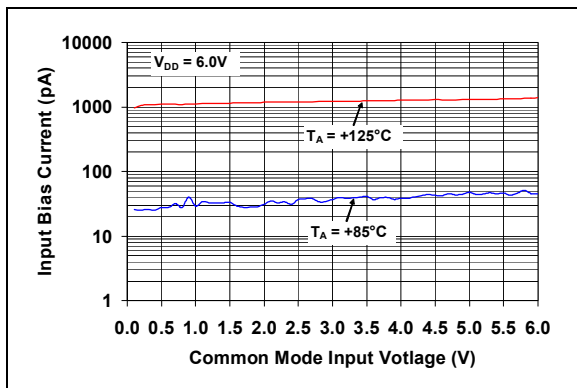
**FIGURE 2-16:** Quiescent Current vs. Ambient Temperature with  $V_{CM} = 0.9V_{DD}$ .



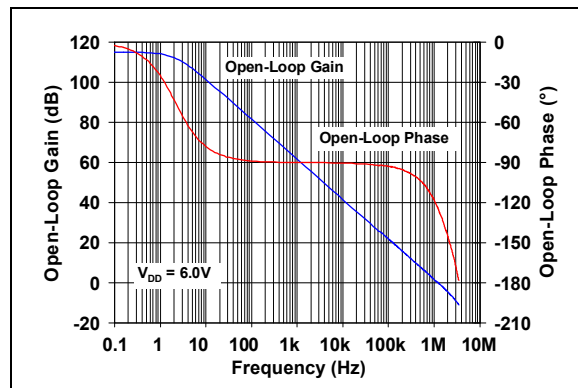
**FIGURE 2-14:** Input Bias, Offset Currents vs. Ambient Temperature.



**FIGURE 2-17:** Quiescent Current vs. Power Supply Voltage with  $V_{CM} = 0.9V_{DD}$ .



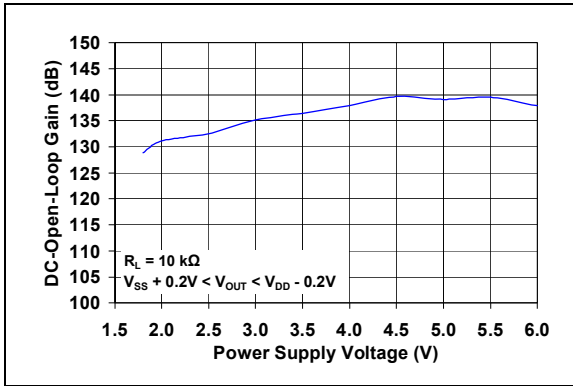
**FIGURE 2-15:** Input Bias Current vs. Common Mode Input Voltage.



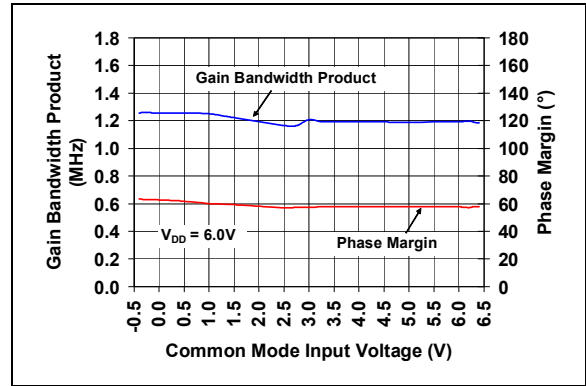
**FIGURE 2-18:** Open-Loop Gain, Phase vs. Frequency.



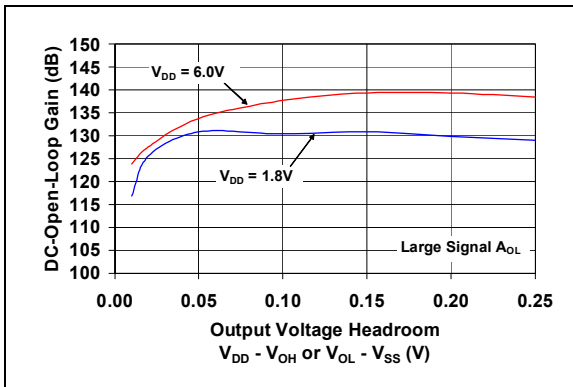
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +1.8\text{V}$  to  $+6.0\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 60\text{ pF}$ .



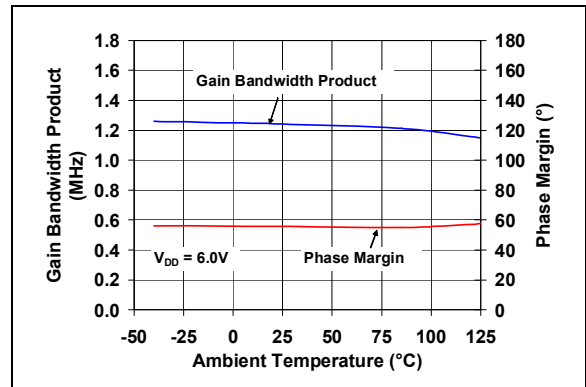
**FIGURE 2-19:** DC Open-Loop Gain vs. Power Supply Voltage.



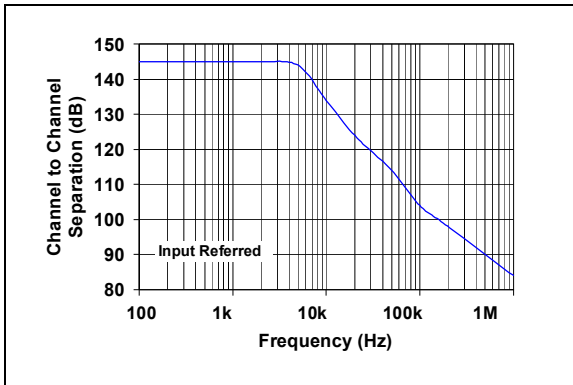
**FIGURE 2-22:** Gain Bandwidth Product, Phase Margin vs. Common Mode Input Voltage.



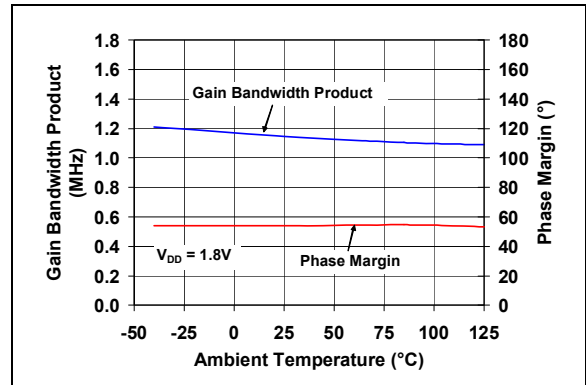
**FIGURE 2-20:** DC Open-Loop Gain vs. Output Voltage Headroom.



**FIGURE 2-23:** Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.



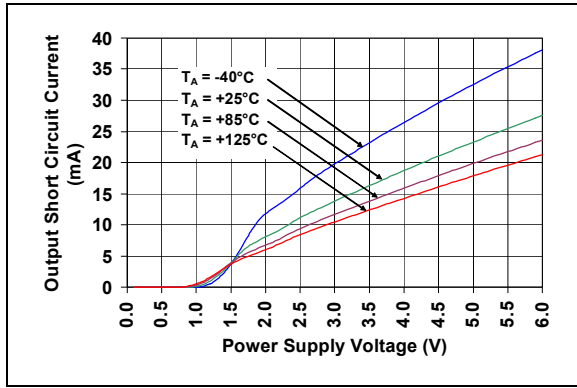
**FIGURE 2-21:** Channel-to-Channel Separation vs. Frequency (MCP6072/4 only).



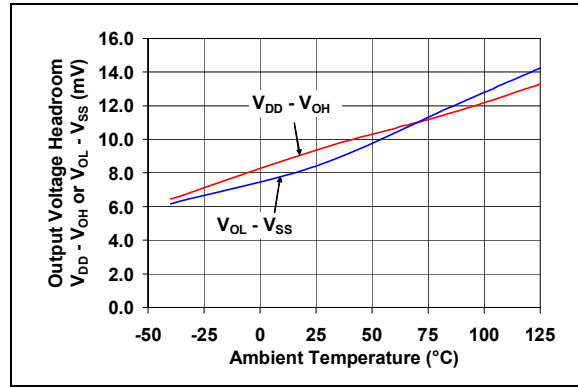
**FIGURE 2-24:** Gain Bandwidth Product, Phase Margin vs. Ambient Temperature.

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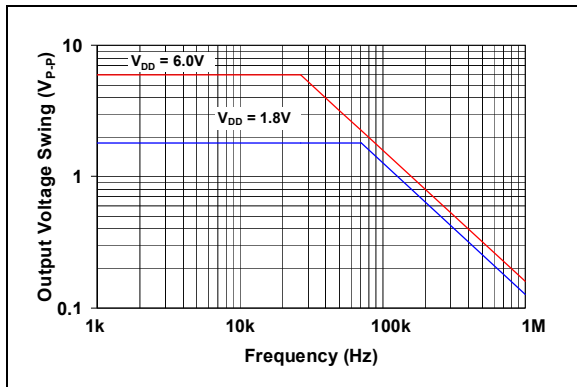
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +1.8\text{V}$  to  $+6.0\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 60\text{ pF}$ .



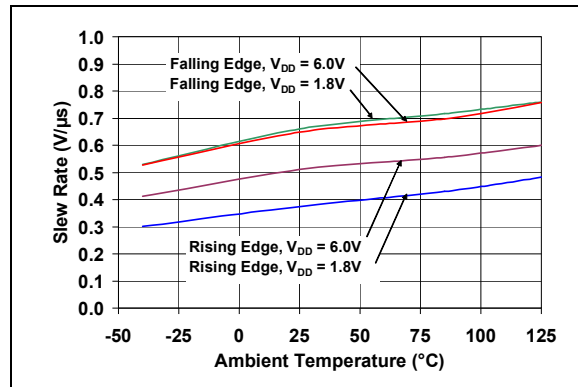
**FIGURE 2-25:** Output Short Circuit Current vs. Power Supply Voltage.



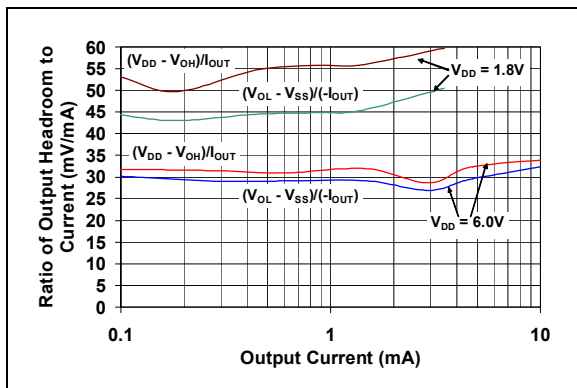
**FIGURE 2-28:** Output Voltage Headroom vs. Ambient Temperature.



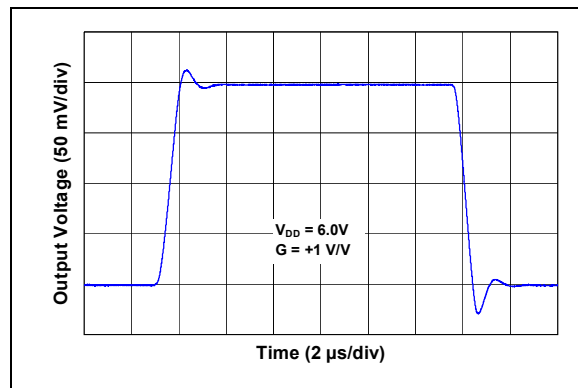
**FIGURE 2-26:** Output Voltage Swing vs. Frequency.



**FIGURE 2-29:** Slew Rate vs. Ambient Temperature.

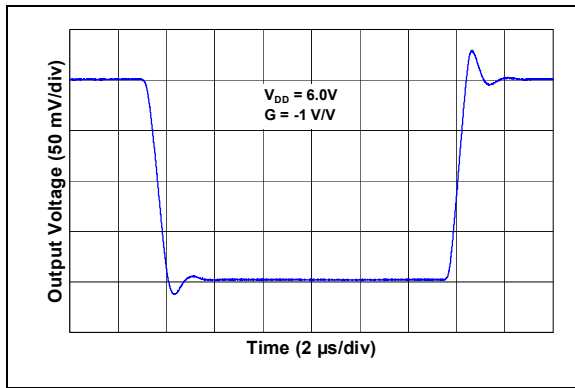


**FIGURE 2-27:** Ratio of Output Voltage Headroom to Output Current vs. Output Current.

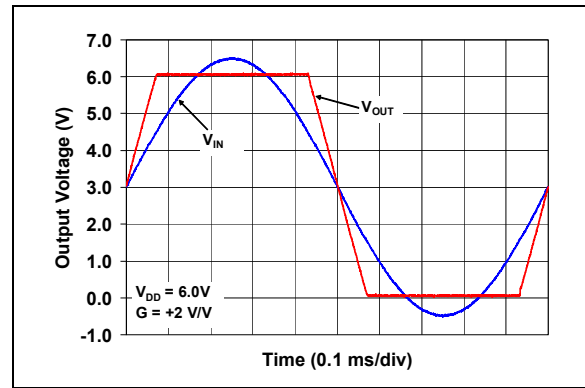


**FIGURE 2-30:** Small Signal Noninverting Pulse Response.

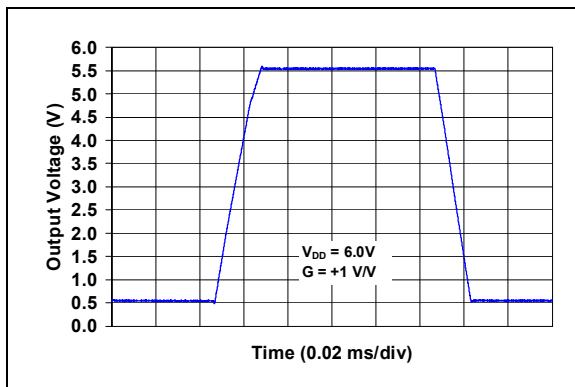
**Note:** Unless otherwise indicated,  $T_A = +25^\circ\text{C}$ ,  $V_{DD} = +1.8\text{V}$  to  $+6.0\text{V}$ ,  $V_{SS} = \text{GND}$ ,  $V_{CM} = V_{DD}/2$ ,  $V_{OUT} \approx V_{DD}/2$ ,  $V_L = V_{DD}/2$ ,  $R_L = 10\text{ k}\Omega$  to  $V_L$  and  $C_L = 60\text{ pF}$ .



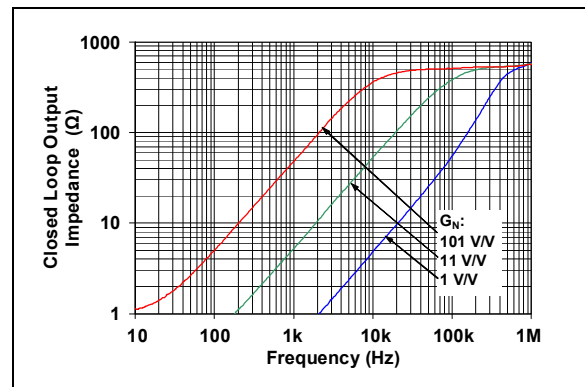
**FIGURE 2-31:** Small Signal Inverting Pulse Response.



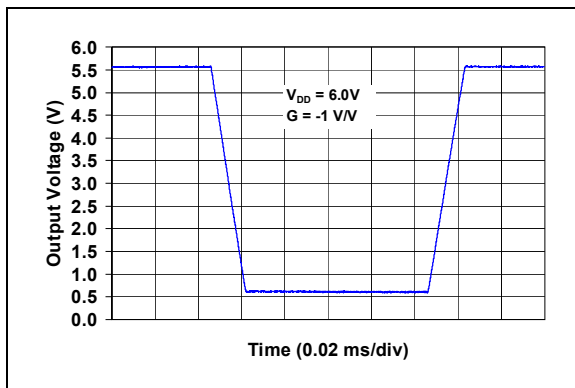
**FIGURE 2-34:** The MCP6071/2/4 Shows No Phase Reversal.



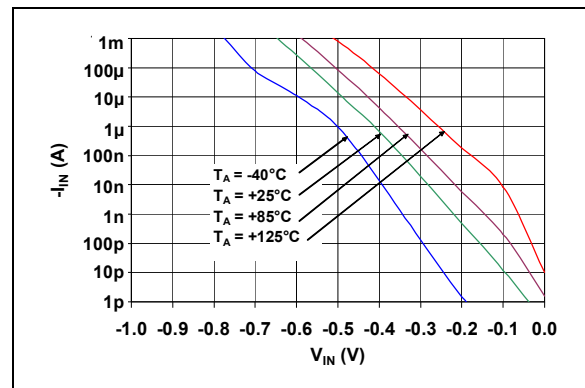
**FIGURE 2-32:** Large Signal Noninverting Pulse Response.



**FIGURE 2-35:** Closed Loop Output Impedance vs. Frequency.



**FIGURE 2-33:** Large Signal Inverting Pulse Response.



**FIGURE 2-36:** Measured Input Current vs. Input Voltage (below  $V_{SS}$ ).

# MCP6071/2/4

## 3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in [Table 3-1](#).

**TABLE 3-1: PIN FUNCTION TABLE**

MCP6071			MCP6072		MCP6074	Symbol	Description
SOIC	SOT-23-5	2x3 TDFN	SOIC	2x3 TDFN	SOIC, TSSOP		
6	1	6	1	1	1	$V_{OUT}, V_{OUTA}$	Analog Output (op amp A)
2	4	2	2	2	2	$V_{IN}^-, V_{INA}^-$	Inverting Input (op amp A)
3	3	3	3	3	3	$V_{IN}^+, V_{INA}^+$	Noninverting Input (op amp A)
7	5	7	8	8	4	$V_{DD}$	Positive Power Supply
—	—	—	5	5	5	$V_{INB}^+$	Noninverting Input (op amp B)
—	—	—	6	6	6	$V_{INB}^-$	Inverting Input (op amp B)
—	—	—	7	7	7	$V_{OUTB}$	Analog Output (op amp B)
—	—	—	—	—	8	$V_{OUTC}$	Analog Output (op amp C)
—	—	—	—	—	9	$V_{INC}^-$	Inverting Input (op amp C)
—	—	—	—	—	10	$V_{INC}^+$	Noninverting Input (op amp C)
4	2	4	4	4	11	$V_{SS}$	Negative Power Supply
—	—	—	—	—	12	$V_{IND}^+$	Noninverting Input (op amp D)
—	—	—	—	—	13	$V_{IND}^-$	Inverting Input (op amp D)
—	—	—	—	—	14	$V_{OUTD}$	Analog Output (op amp D)
1, 5, 8	—	1, 5, 8	—	—	—	NC	No Internal Connection
—	—	9	—	9	—	EP	Exposed Thermal Pad (EP); must be connected to $V_{SS}$ .

### 3.1 Analog Outputs

The output pins are low-impedance voltage sources.

### 3.2 Analog Inputs

The noninverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

### 3.3 Power Supply Pins

The positive power supply ( $V_{DD}$ ) is 1.8V to 6.0V higher than the negative power supply ( $V_{SS}$ ). For normal operation, the other pins are at voltages between  $V_{SS}$  and  $V_{DD}$ .

Typically, these parts are used in a single (positive) supply configuration. In this case,  $V_{SS}$  is connected to ground and  $V_{DD}$  is connected to the supply.  $V_{DD}$  will need bypass capacitors.

### 3.4 Exposed Thermal Pad (EP)

There is an internal electrical connection between the Exposed Thermal Pad (EP) and the  $V_{SS}$  pin; they must be connected to the same potential on the Printed Circuit Board (PCB).

NOTES:

# MCP6071/2/4

## 4.0 APPLICATION INFORMATION

The MCP6071/2/4 family of op amps is manufactured using Microchip's state-of-the-art CMOS process and is specifically designed for low-power, high precision applications.

### 4.1 Rail-to-Rail Input

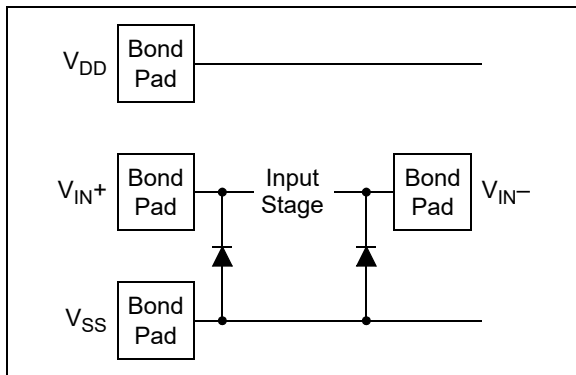
#### 4.1.1 PHASE REVERSAL

The MCP6071/2/4 op amps are designed to prevent phase reversal when the input pins exceed the supply voltages. [Figure 2-34](#) shows the input voltage exceeding the supply voltage without any phase reversal.

#### 4.1.2 INPUT VOLTAGE LIMITS

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the voltages at the input pins (see [Section 1.1, Absolute Maximum Ratings †](#)).

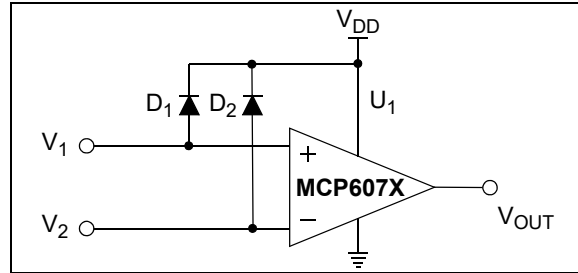
The ESD protection on the inputs can be depicted as shown in [Figure 4-1](#). This structure was chosen to protect the input transistors and to minimize input bias current ( $I_B$ ).



**FIGURE 4-1:** Simplified Analog Input ESD Structures.

The input ESD diodes clamp the inputs when they try to go more than one diode drop below V<sub>SS</sub>. They also clamp any voltages that go well above V<sub>DD</sub>; their breakdown voltage is high enough to allow normal operation, but not low enough to protect against slow over-voltage (beyond V<sub>DD</sub>) events. Very fast ESD events (that meet the spec) are limited so that damage does not occur.

In some applications, it may be necessary to prevent excessive voltages from reaching the op amp inputs. [Figure 4-2](#) shows one approach to protecting these inputs.



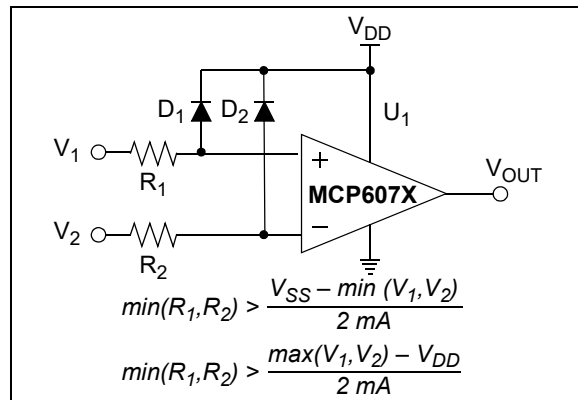
**FIGURE 4-2:** Protecting the Analog Inputs.

A significant amount of current can flow out of the inputs when the Common Mode voltage ( $V_{CM}$ ) is below ground ( $V_{SS}$ ). See [Figure 2-36](#).

#### 4.1.3 INPUT CURRENT LIMITS

In order to prevent damage and/or improper operation of these amplifiers, the circuit must limit the voltages at the input pins (see [Section 1.1, Absolute Maximum Ratings †](#)).

[Figure 4-3](#) shows one approach to protecting these inputs. The resistors R<sub>1</sub> and R<sub>2</sub> limit the possible currents in or out of the input pins (and the ESD diodes, D<sub>1</sub> and D<sub>2</sub>). The diode currents will go through either V<sub>DD</sub> or V<sub>SS</sub>.



**FIGURE 4-3:** Protecting the Analog Inputs.

#### 4.1.4 NORMAL OPERATION

The input stage of the MCP6071/2/4 op amps use two differential input stages in parallel. One operates at a low common mode input voltage ( $V_{CM}$ ), while the other operates at a high  $V_{CM}$ . With this topology, the device operates with a  $V_{CM}$  up to 300 mV above V<sub>DD</sub> and 300 mV below V<sub>SS</sub>. (See [Figure 2-13](#)). The input offset voltage is measured at  $V_{CM} = V_{SS} - 0.3V$  and V<sub>DD</sub> + 0.3V to ensure proper operation.

The transition between the input stages occurs when  $V_{CM}$  is near V<sub>DD</sub> - 1.1V (See [Figures 2-4, 2-5](#) and [Figure 2-6](#)). For the best distortion performance and gain linearity, with noninverting gains, avoid this region of operation.

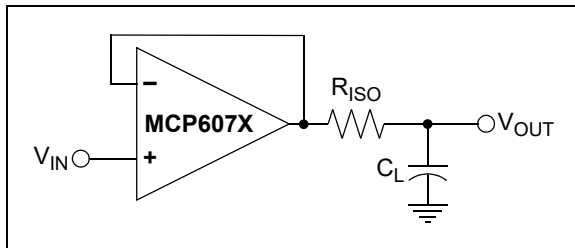
## 4.2 Rail-to-Rail Output

The output voltage range of the MCP6071/2/4 op amps is  $V_{SS} + 15\text{ mV}$  (minimum) and  $V_{DD} - 15\text{ mV}$  (maximum) when  $R_L = 10\text{ k}\Omega$  is connected to  $V_{DD}/2$  and  $V_{DD} = 6.0\text{V}$ . Refer to [Figures 2-27](#) and [2-28](#) for more information.

## 4.3 Capacitive Loads

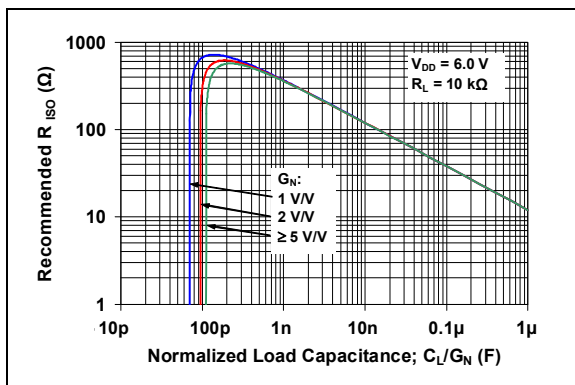
Driving large capacitive loads can cause stability problems for voltage feedback op amps. As the load capacitance increases, the feedback loop's phase margin decreases and the closed-loop bandwidth is reduced. This produces gain peaking in the frequency response, with overshoot and ringing in the step response. While a unity-gain buffer ( $G = +1$ ) is the most sensitive to capacitive loads, all gains show the same general behavior.

When driving large capacitive loads with these op amps (e.g.,  $> 100\text{ pF}$  when  $G = +1$ ), a small series resistor at the output ( $R_{ISO}$  in [Figure 4-4](#)) improves the feedback loop's phase margin (stability) by making the output load resistive at higher frequencies. The bandwidth will be generally lower than the bandwidth with no capacitance load.



**FIGURE 4-4:** Output Resistor,  $R_{ISO}$  Stabilizes Large Capacitive Loads.

[Figure 4-5](#) gives recommended  $R_{ISO}$  values for different capacitive loads and gains. The x-axis is the normalized load capacitance ( $C_L/G_N$ ), where  $G_N$  is the circuit's noise gain. For noninverting gains,  $G_N$  and the Signal Gain are equal. For inverting gains,  $G_N$  is  $1 + |\text{Signal Gain}|$  (e.g.,  $-1\text{ V/V}$  gives  $G_N = +2\text{ V/V}$ ).



**FIGURE 4-5:** Recommended  $R_{ISO}$  Values for Capacitive Loads.

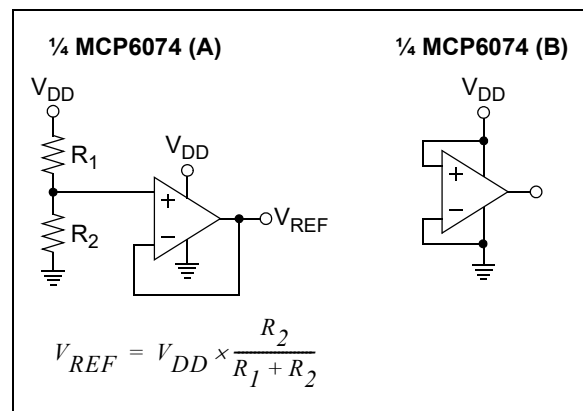
After selecting  $R_{ISO}$  for your circuit, double-check the resulting frequency response peaking and step response overshoot. Modify  $R_{ISO}$ 's value until the response is reasonable. Bench evaluation and simulations with the MCP6071/2/4 SPICE macro model are very helpful.

## 4.4 Supply Bypass

With this family of operational amplifiers, the power supply pin ( $V_{DD}$  for single-supply) should have a local bypass capacitor (i.e.,  $0.01\text{ }\mu\text{F}$  to  $0.1\text{ }\mu\text{F}$ ) within 2 mm for good high frequency performance. It can use a bulk capacitor (i.e.,  $1\text{ }\mu\text{F}$  or larger) within 100 mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

## 4.5 Unused Op Amps

An unused op amp in a quad package (MCP6074) should be configured as shown in [Figure 4-6](#). These circuits prevent the output from toggling and causing crosstalk. Circuit A sets the op amp at its minimum noise gain. The resistor divider produces any desired reference voltage within the output voltage range of the op amp; the op amp buffers that reference voltage. Circuit B uses the minimum number of components and operates as a comparator, but it may draw more current.



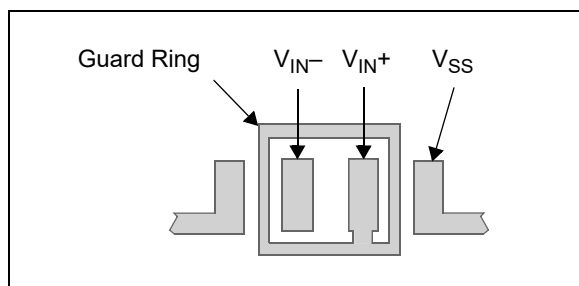
**FIGURE 4-6:** Unused Op Amps.

# MCP6071/2/4

## 4.6 PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is  $10^{12}\Omega$ . A 5V difference would cause 5 pA of current to flow; which is greater than the MCP6071/2/4 family's bias current at +25°C ( $\pm 1.0$  pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-7.



**FIGURE 4-7:** Example Guard Ring Layout for Inverting Gain.

1. Noninverting Gain and Unity-Gain Buffer:
  - a. Connect the noninverting pin ( $V_{IN+}$ ) to the input with a wire that does not touch the PCB surface.
  - b. Connect the guard ring to the inverting input pin ( $V_{IN-}$ ). This biases the guard ring to the common mode input voltage.
2. Inverting Gain and Transimpedance Gain Amplifiers (convert current to voltage, such as photo detectors):
  - a. Connect the guard ring to the noninverting input pin ( $V_{IN+}$ ). This biases the guard ring to the same reference voltage as the op amp (e.g.,  $V_{DD}/2$  or ground).
  - b. Connect the inverting pin ( $V_{IN-}$ ) to the input with a wire that does not touch the PCB surface.

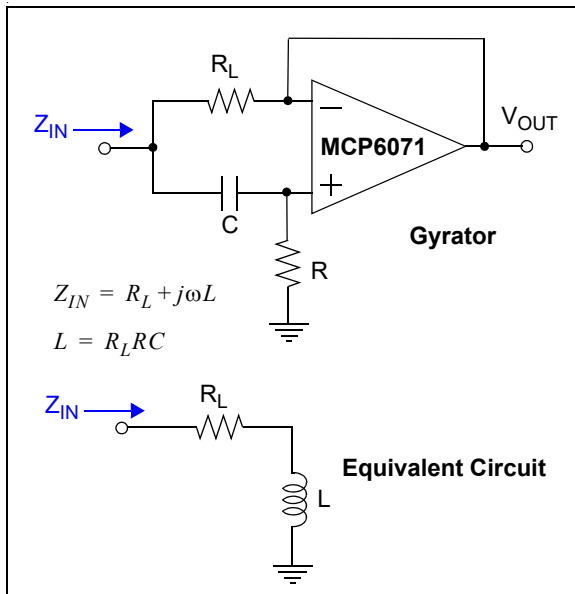


## 4.7 Application Circuits

### 4.7.1 GYRATOR

The MCP6071/2/4 op amps can be used in gyrator applications. The gyrator is an electric circuit which can make a capacitive circuit behave inductively.

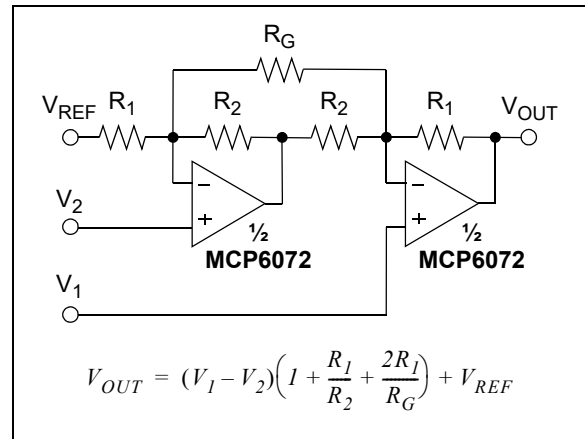
Figure 4-8 shows an example of a gyrator simulating inductance, with an approximately equivalent circuit below. The two  $Z_{IN}$  have similar values in typical applications. The primary application for a gyrator is to reduce the size and cost of a system by removing the need for bulky, heavy and expensive inductors. For example, RLC bandpass filter characteristics can be realized with capacitors, resistors and operational amplifiers without using inductors. Moreover, gyrators will typically have higher accuracy than real inductors, due to the lower cost of precision capacitors than inductors.



**FIGURE 4-8:** Gyrator.

### 4.7.2 INSTRUMENTATION AMPLIFIER

The MCP6071/2/4 op amps are well suited for conditioning sensor signals in battery-powered applications. Figure 4-9 shows a two op amp instrumentation amplifier, using the MCP6072, that works well for applications requiring rejection of common mode noise at higher gains. The reference voltage ( $V_{REF}$ ) is supplied by a low impedance source. In single supply applications,  $V_{REF}$  is typically  $V_{DD}/2$ .

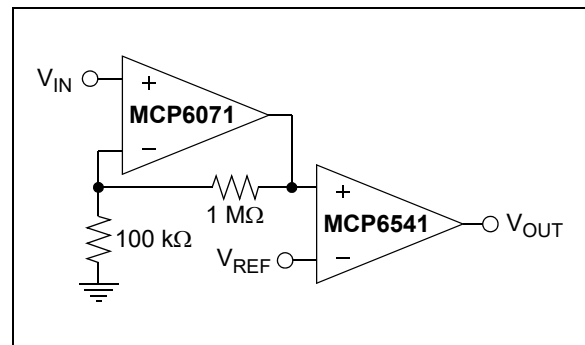


**FIGURE 4-9:** Two Op Amp Instrumentation Amplifier.

To obtain the best CMRR possible, and not limit the performance by the resistor tolerances, set a high gain with the  $R_G$  resistor.

### 4.7.3 PRECISION COMPARATOR

Use high gain before a comparator to improve the latter's input offset performance. Figure 4-10 shows a gain of 11 V/V placed before a comparator. The reference voltage  $V_{REF}$  can be any value between the supply rails.



**FIGURE 4-10:** Precision, Noninverting Comparator.

## 5.0 DESIGN AIDS

Microchip provides the basic design tools needed for the MCP6071/2/4 family of op amps.

### 5.1 SPICE Macro Model

The latest SPICE macro model for the MCP6071/2/4 op amps is available on the Microchip web site at [www.microchip.com](http://www.microchip.com). The model was written and tested in official Orcad (Cadence) owned PSPICE. For the other simulators, it may require translation.

The model covers a wide aspect of the op amp's electrical specifications. Not only does the model cover voltage, current, and resistance of the op amp, but it also covers the temperature and noise effects on the behavior of the op amp. The model has not been verified outside of the specification range listed in the op amp data sheet. The model behaviors under these conditions can not be guaranteed that it will match the actual op amp performance.

Moreover, the model is intended to be an initial design tool. Bench testing is a very important part of any design and cannot be replaced with simulations. Also, simulation results using this macro model need to be validated by comparing them to the data sheet specifications and characteristic curves.

### 5.2 FilterLab® Software

Microchip's FilterLab® software is an innovative software tool that simplifies analog active filter (using op amps) design. Available at no cost from the Microchip web site at [www.microchip.com/filterlab](http://www.microchip.com/filterlab), the FilterLab design tool provides full schematic diagrams of the filter circuit with component values. It also outputs the filter circuit in SPICE format, which can be used with the macro model to simulate actual filter performance.

### 5.3 MAPS (Microchip Advanced Part Selector)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip website at [www.microchip.com/maps](http://www.microchip.com/maps), the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for Data Sheets, purchase, and sampling of Microchip parts.

## 5.4 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at [www.microchip.com/analogtools](http://www.microchip.com/analogtools).

Some boards that are especially useful are:

- MCP6XXX Amplifier Evaluation Board 1
- MCP6XXX Amplifier Evaluation Board 2
- MCP6XXX Amplifier Evaluation Board 3
- MCP6XXX Amplifier Evaluation Board 4
- Active Filter Demo Board Kit
- 5/6-Pin SOT-23 Evaluation Board, P/N VSUPEV2
- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV
- 14-Pin SOIC/TSSOP/DIP Evaluation Board, P/N SOIC14EV

## 5.5 Application Notes

The following Microchip Analog Design Note and Application Notes are available on the Microchip web site at [www.microchip.com/appnotes](http://www.microchip.com/appnotes) and are recommended as supplemental reference resources.

- **ADN003:** "Select the Right Operational Amplifier for your Filtering Circuits", DS21821
- **AN722:** "Operational Amplifier Topologies and DC Specifications", DS00722
- **AN723:** "Operational Amplifier AC Specifications and Applications", DS00723
- **AN884:** "Driving Capacitive Loads With Op Amps", DS00884
- **AN990:** "Analog Sensor Conditioning Circuits – An Overview", DS00990
- **AN1177:** "Op Amp Precision Design: DC Errors", DS01177
- **AN1228:** "Op Amp Precision Design: Random Noise", DS01228
- **AN1332:** "Current Sensing Circuit Concepts and Fundamentals", DS01332

These application notes and others are listed in the design guide:

- "Signal Chain Design Guide", DS21825

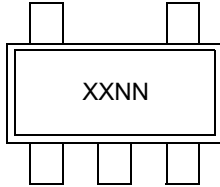
NOTES:

# MCP6071/2/4

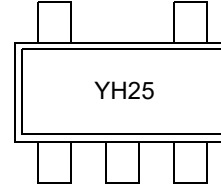
## 6.0 PACKAGING INFORMATION

### 6.1 Package Marking Information

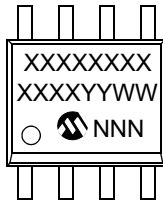
5-Lead SOT-23 (MCP6071)



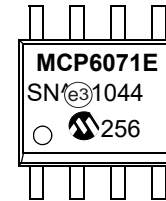
Example:



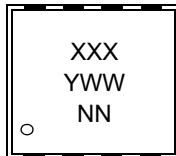
8-Lead SOIC (150 mil) (MCP6071, MCP6072)



Example:

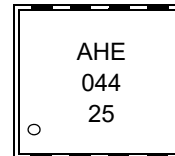


8-Lead 2x3 TDFN (MCP6071, MCP6072)



Device	Marking
MCP6071	AHE
MCP6072	AHF

Example:

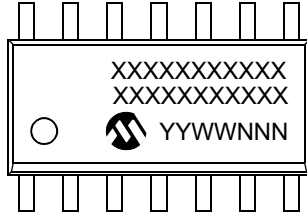


<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

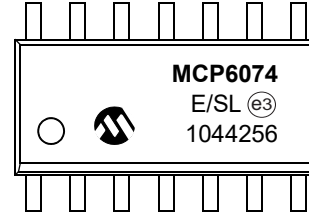
**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

## Package Marking Information (Continuation)

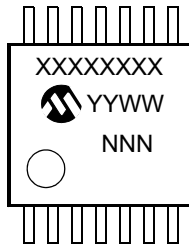
14-Lead SOIC (150 mil) (MCP6074)



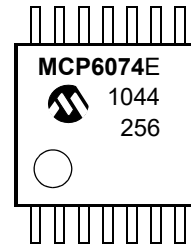
Example:



14-Lead TSSOP (MCP6074)



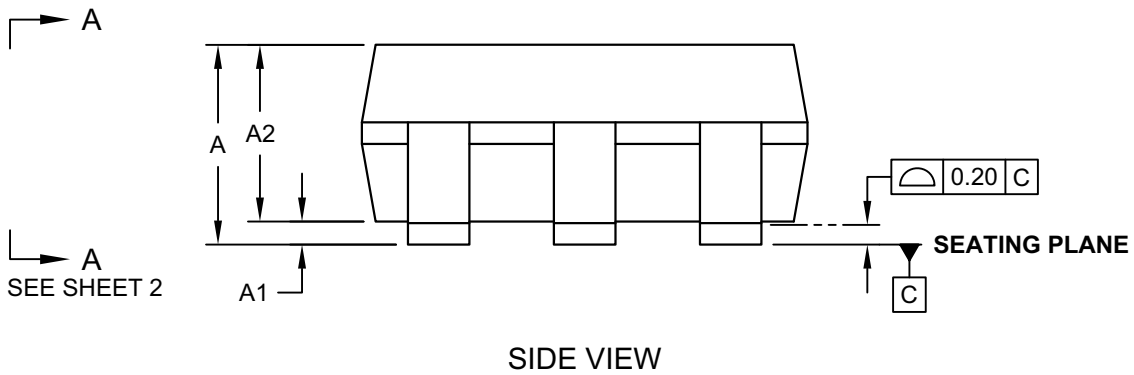
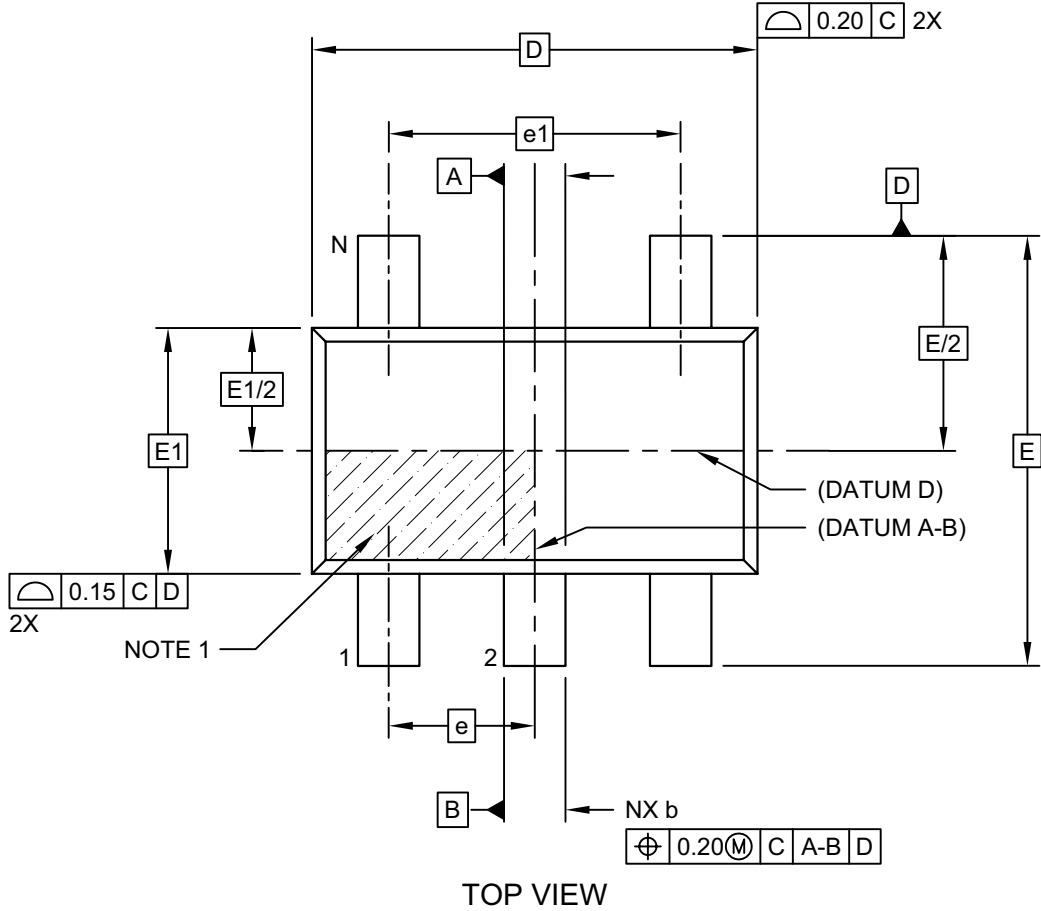
Example:



# MCP6071/2/4

## 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

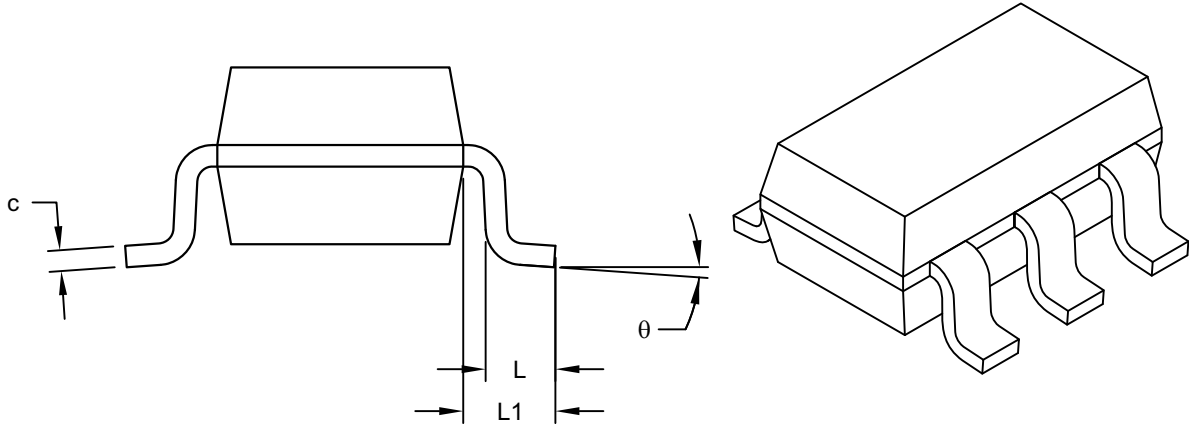
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-091-OT Rev F Sheet 1 of 2

## 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



VIEW A-A  
SHEET 1

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	5		
Pitch	e	0.95 BSC		
Outside lead pitch	e1	1.90 BSC		
Overall Height	A	0.90	-	1.45
Molded Package Thickness	A2	0.89	-	1.30
Standoff	A1	-	-	0.15
Overall Width	E	2.80 BSC		
Molded Package Width	E1	1.60 BSC		
Overall Length	D	2.90 BSC		
Foot Length	L	0.30	-	0.60
Footprint	L1	0.60 REF		
Foot Angle	φ	0°	-	10°
Lead Thickness	c	0.08	-	0.26
Lead Width	b	0.20	-	0.51

**Notes:**

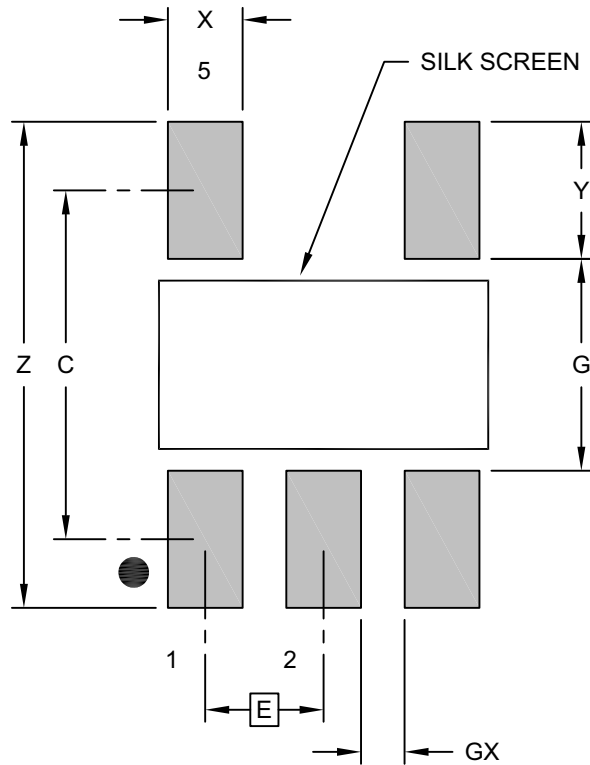
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
- Dimensioning and tolerancing per ASME Y14.5M  
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-091-OT Rev F Sheet 2 of 2

# MCP6071/2/4

## 5-Lead Plastic Small Outline Transistor (OT) [SOT23]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

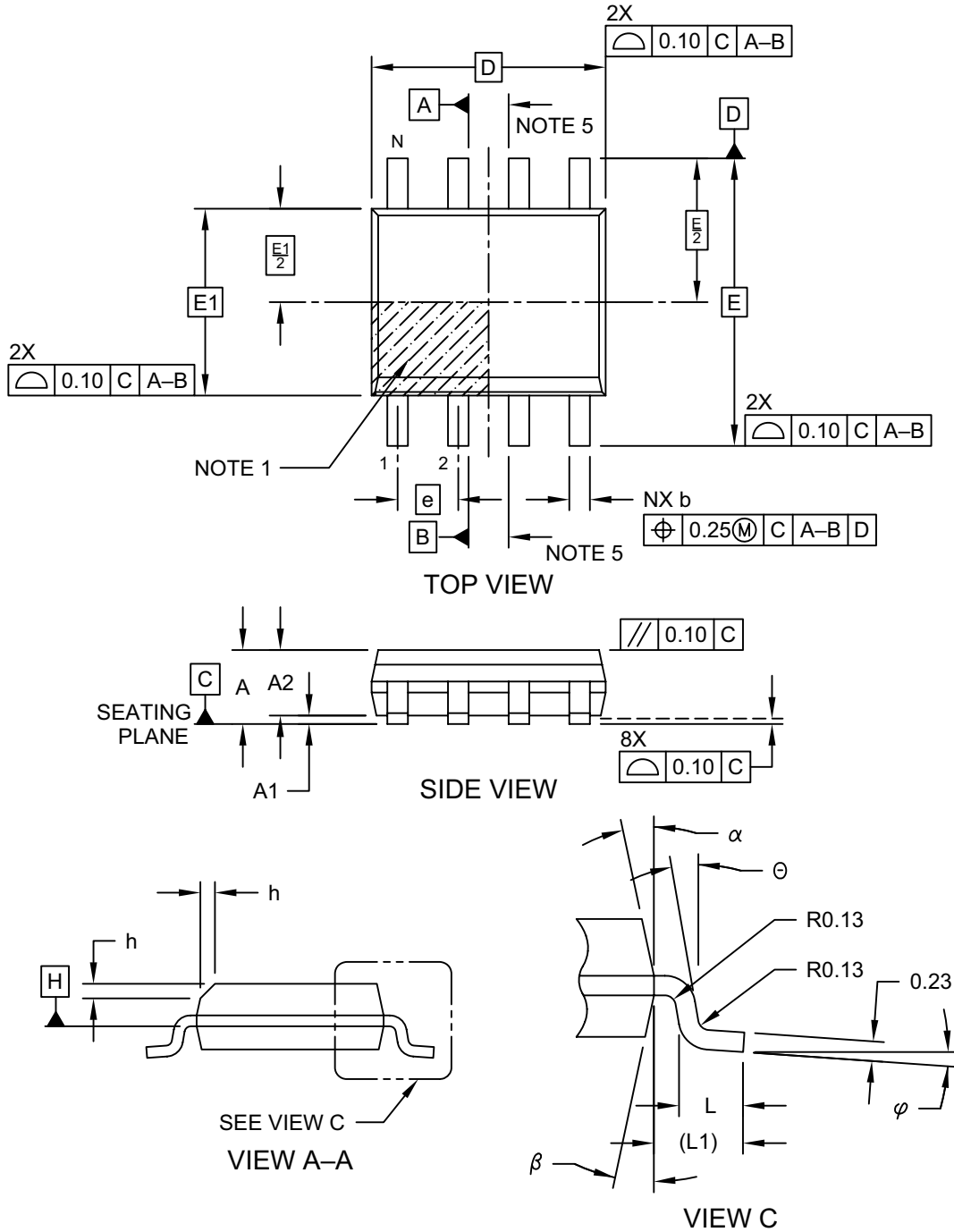
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091-OT Rev F



## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

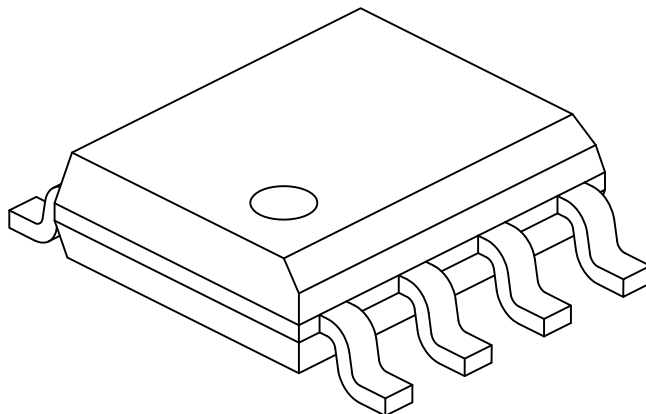


Microchip Technology Drawing No. C04-057-SN Rev F Sheet 1 of 2

# MCP6071/2/4

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Foot Angle	$\varphi$	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	$\alpha$	5°	-	15°
Mold Draft Angle Bottom	$\beta$	5°	-	15°

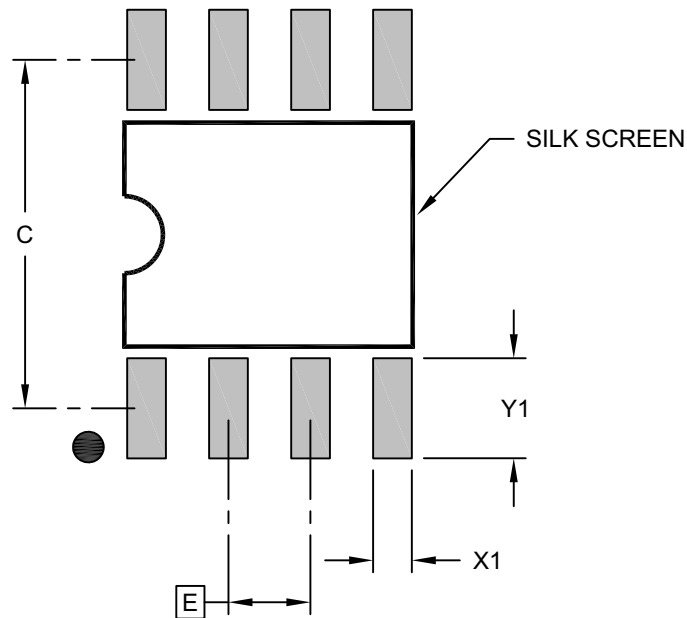
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev F Sheet 2 of 2

## 8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

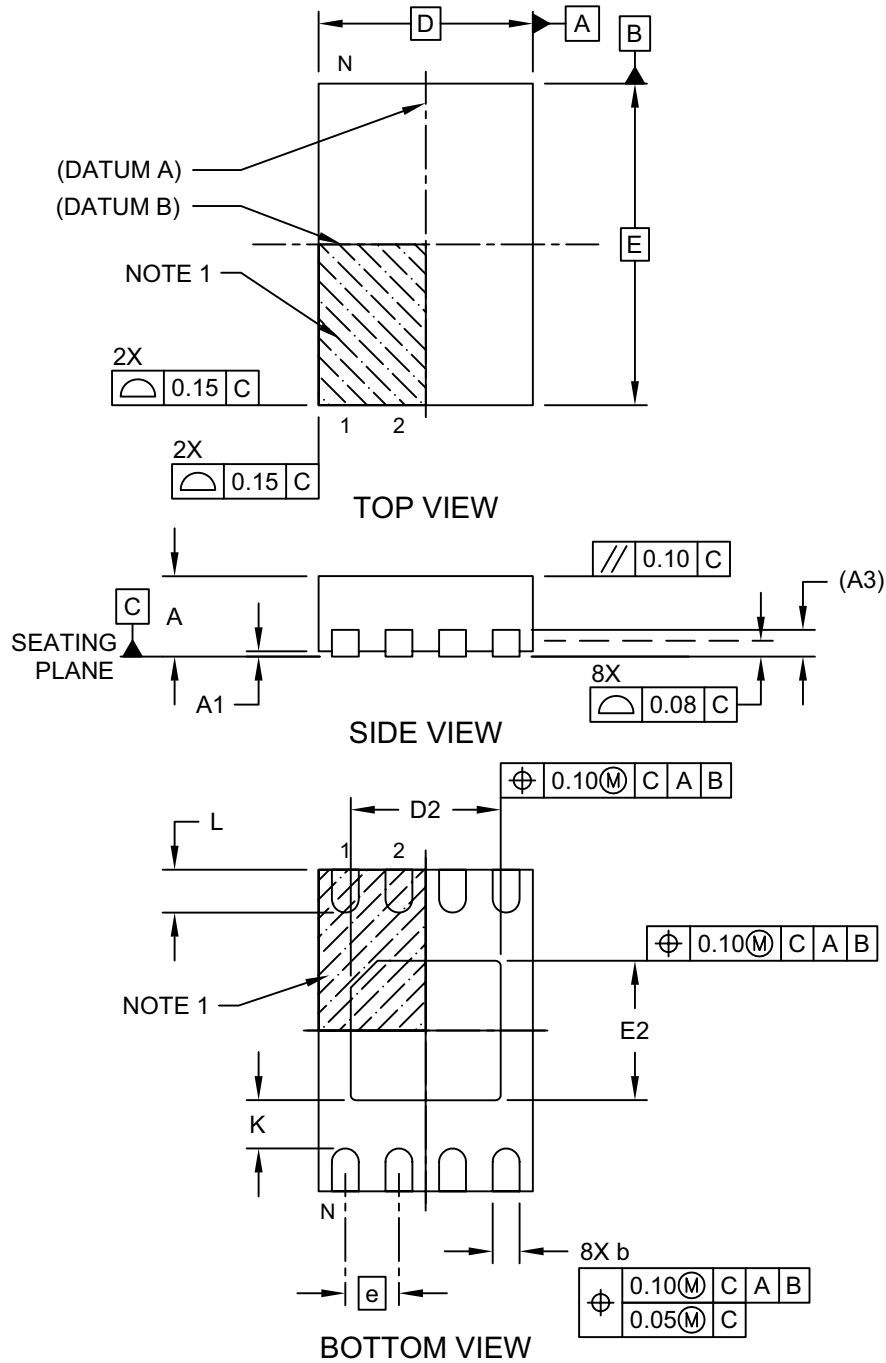
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-SN Rev F

# MCP6071/2/4

## 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

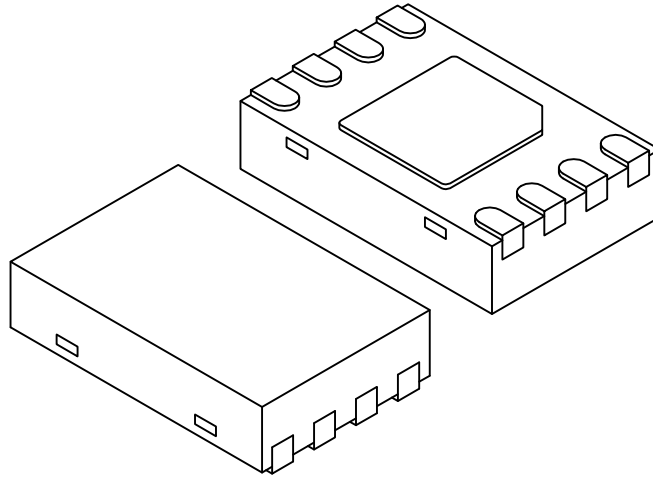
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing No. C04-129-MN Rev E Sheet 1 of 2

## 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	1.35	1.40	1.45
Exposed Pad Width	E2	1.25	1.30	1.35
Contact Width	b	0.20	0.25	0.30
Contact Length	L	0.25	0.30	0.45
Contact-to-Exposed Pad	K	0.20	-	-

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

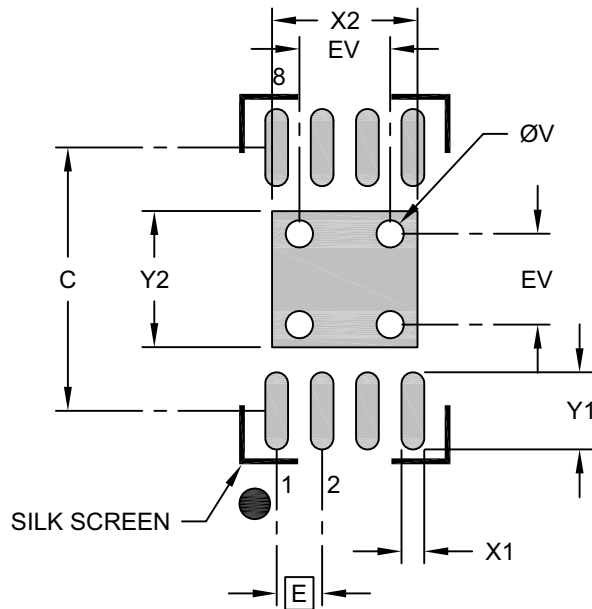
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-129-MN Rev E Sheet 2 of 2

# MCP6071/2/4

## 8-Lead Plastic Dual Flat, No Lead Package (MN) – 2x3x0.8 mm Body [TDFN] With 1.4x1.3 mm Exposed Pad (JEDEC Package type WDFN)

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			1.60
Optional Center Pad Length	Y2			1.50
Contact Pad Spacing	C		2.90	
Contact Pad Width (X8)	X1			0.25
Contact Pad Length (X8)	Y1			0.85
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

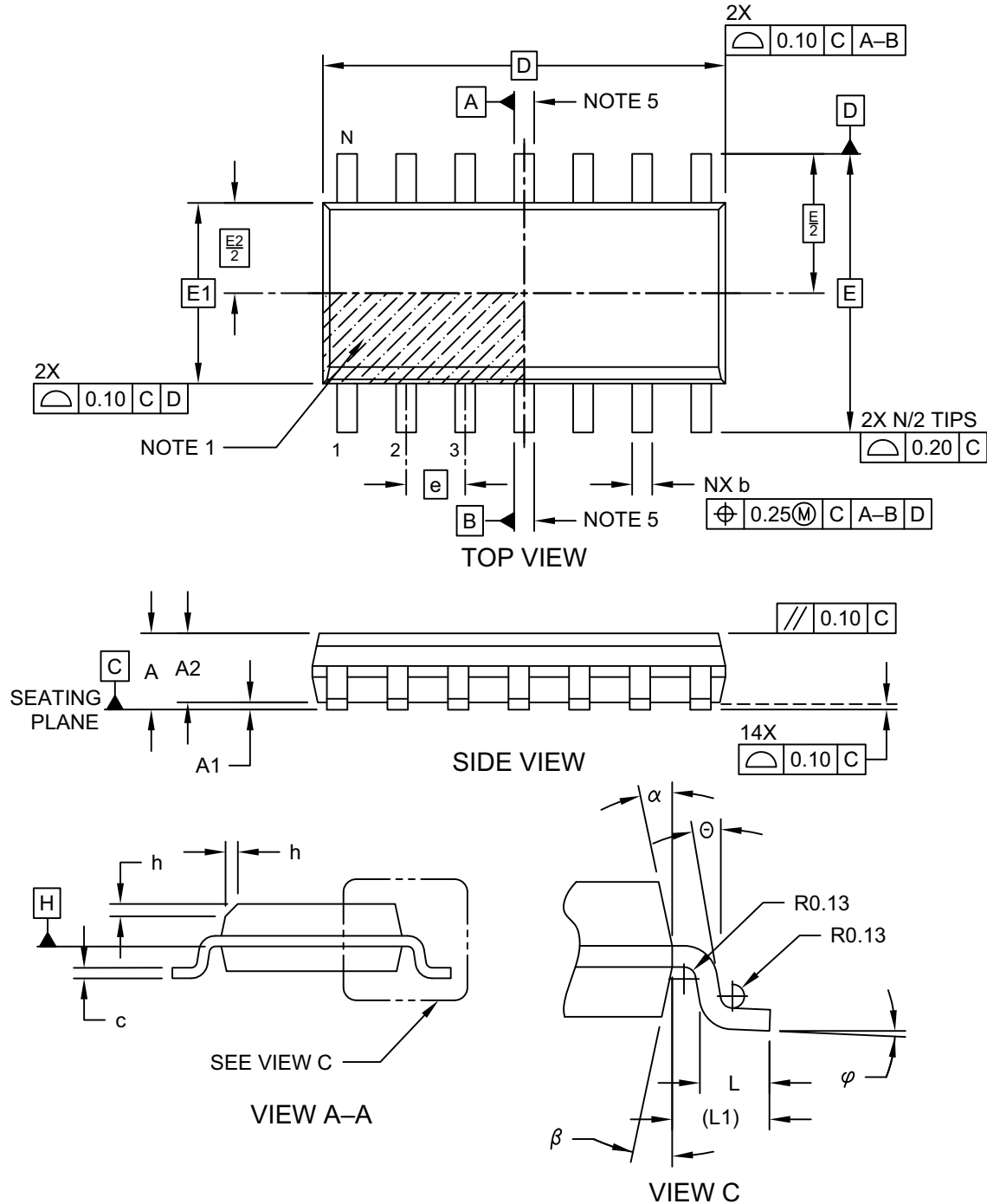
**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing No. C04-129-MN Rev. B

## 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

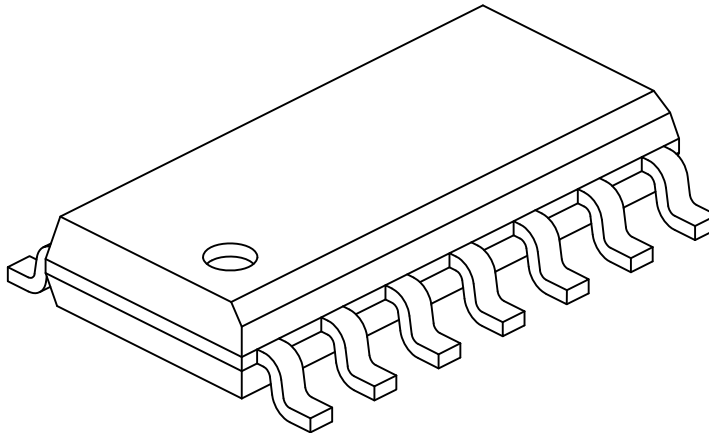


Microchip Technology Drawing No. C04-065-SL Rev D Sheet 1 of 2

# MCP6071/2/4

## 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	14		
Pitch	e	1.27 BSC		
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	8.65 BSC		
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1	1.04 REF		
Lead Angle	∅	0°	-	-
Foot Angle	∅	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

**Notes:**

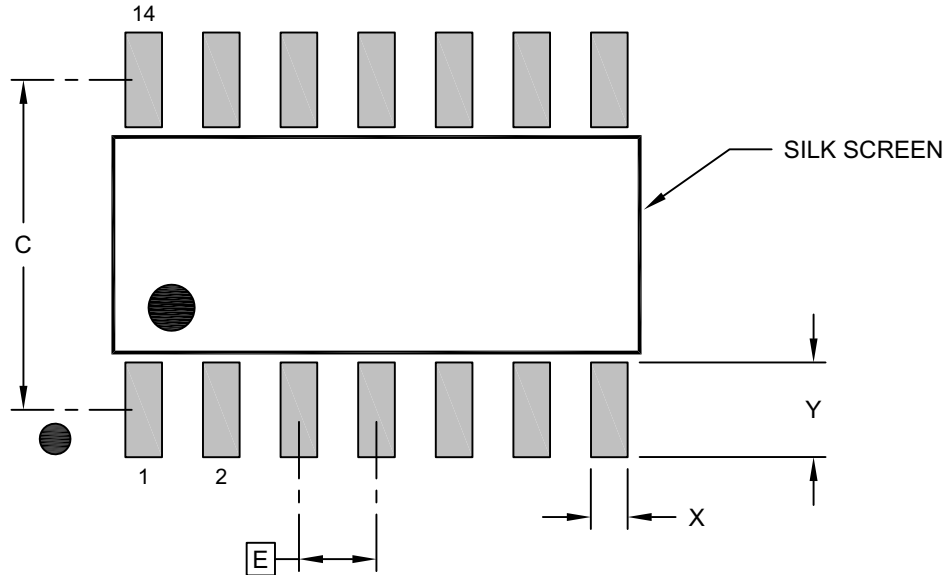
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065-SL Rev D Sheet 2 of 2



## 14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X14)	X			0.60
Contact Pad Length (X14)	Y			1.55

**Notes:**

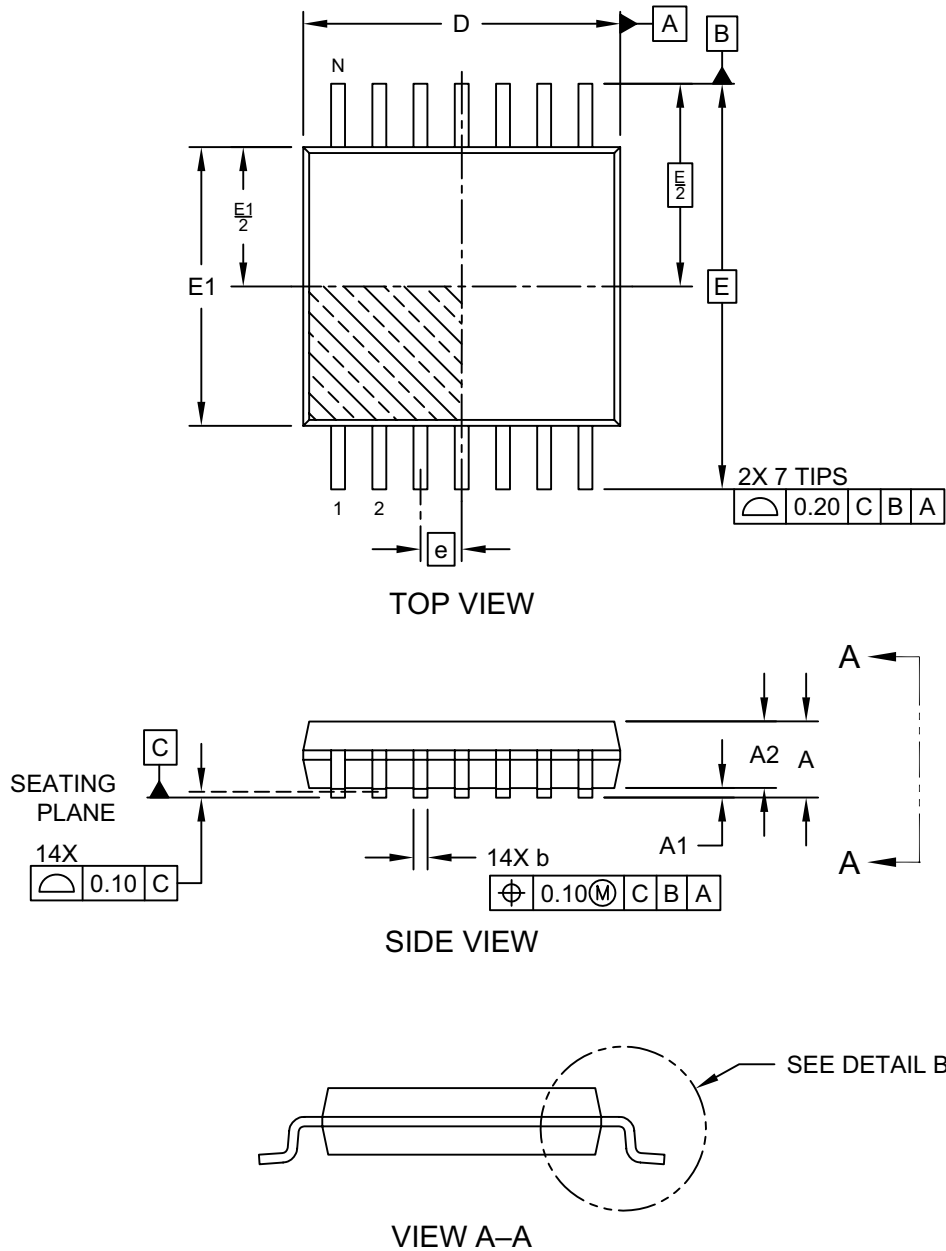
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065-SL Rev D

# MCP6071/2/4

## 14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

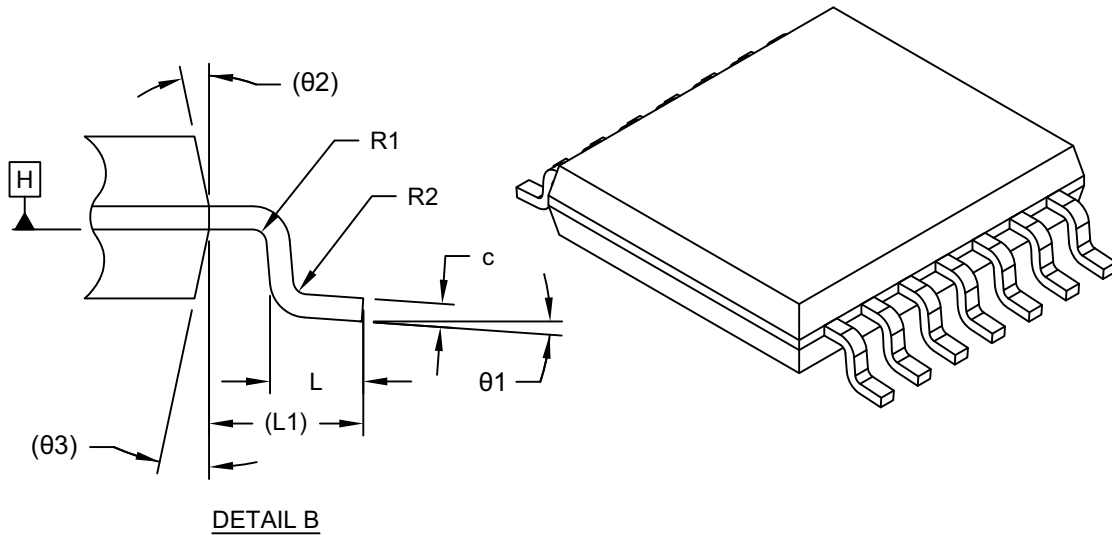
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-087 Rev D Sheet 1 of 2

## 14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Terminals	N	14		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.20
Standoff	A1	0.05	–	0.15
Molded Package Thickness	A2	0.80	1.00	1.05
Overall Length	D	4.90	5.00	5.10
Overall Width	E	6.40 BSC		
Molded Package Width	E1	4.30	4.40	4.50
Terminal Width	b	0.19	–	0.30
Terminal Thickness	c	0.09	–	0.20
Terminal Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Lead Bend Radius	R1	0.09	–	–
Lead Bend Radius	R2	0.09	–	–
Foot Angle	θ1	0°	–	8°
Mold Draft Angle	θ2	–	12° REF	–
Mold Draft Angle	θ3	–	12° REF	–

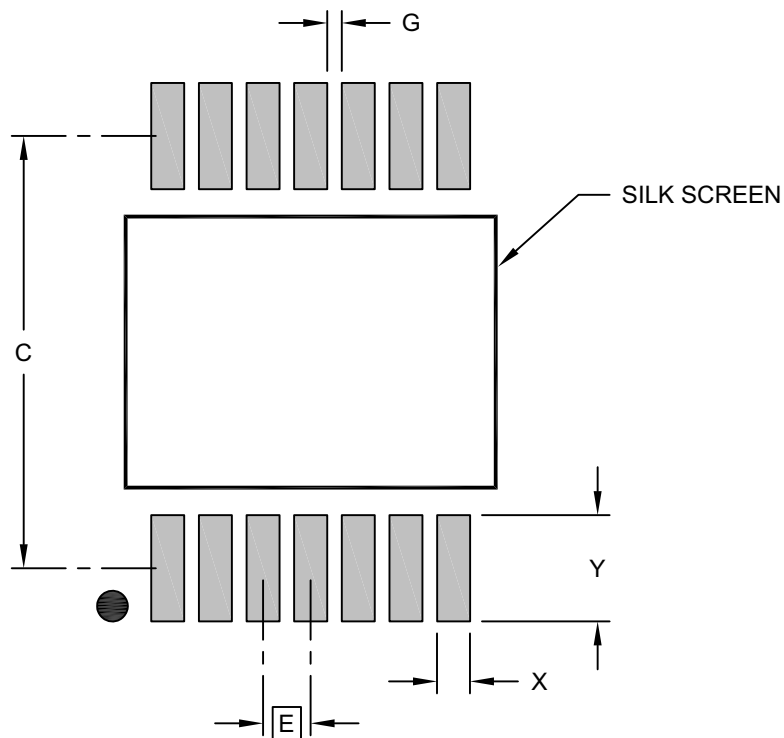
**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensioning and tolerancing per ASME Y14.5M  
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
 REF: Reference Dimension, usually without tolerance, for information purposes only.

# MCP6071/2/4

## 14Lead Thin Shrink Small Outline Package [ST] 4.4 mm Body [TSSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



### RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.90	
Contact Pad Width (Xnn)	X			0.45
Contact Pad Length (Xnn)	Y			1.45
Contact Pad to Contact Pad (Xnn)	G	0.20		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2087 Rev D

## APPENDIX A: REVISION HISTORY

### Revision C (November 2021)

The following is the list of modifications:

- Added Markings table for TDF package option, in [Section 6.1 “Package Marking Information”](#).

### Revision B (December 2010)

The following is the list of modifications:

- Added new SOT-23-5 package type for MCP6071 device.
- Corrected [Figures 2-13, 2-22, 2-23, 2-24, 2-28, 2-29](#) and [2-34](#) in [Section 2.0 “Typical Performance Curves”](#).
- Modified [Table 3-1](#) to show the pin column for MCP6071, SOT-23-5 package.
- Updated [Section 4.1.2 “Input Voltage Limits”](#).
- Added [Section 4.1.3 “Input Current Limits”](#).
- Added new document item in [Section 5.5 “Application Notes”](#).
- Updated the [Product Identification System](#) page.

### Revision A (March 2009)

- Original Release of this Document.

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>-X</u>	<u>/XX</u>	<b>Examples:</b>
Device	Temperature Range	Package	
Device:	MCP6071:	Single Op Amp	a) MCP6071T-E/OT: Tape and Reel, 5LD SOT-23 package
	MCP6071T:	Single Op Amp (Tape and Reel) (SOIC, SOT-23 and 2x3 TDFN)	b) MCP6071-E/SN: 8LD SOIC package
	MCP6072:	Dual Op Amp	c) MCP6071T-E/SN: Tape and Reel, 8LD SOIC package
	MCP6072T:	Dual Op Amp (Tape and Reel) (SOIC and 2x3 TDFN)	d) MCP6071T-E/MNY: Tape and Reel, 8LD 2x3 TDFN package
	MCP6074:	Quad Op Amp	a) MCP6072-E/SN: 8LD SOIC package
	MCP6074T:	Quad Op Amp (Tape and Reel) (SOIC and TSSOP)	b) MCP6072T-E/SN: Tape and Reel, 8LD SOIC package
Temperature Range:	E	= -40°C to +125°C	c) MCP6072T-E/MNY: Tape and Reel, 8LD 2x3 TDFN package
Package:	MNY *	= Plastic Dual Flat, No Lead, (2x3 TDFN) 8-lead	a) MCP6074-E/SL: 14LD SOIC package
	OT	= Plastic Small Outline Transistor (SOT-23), 5-lead	b) MCP6074T-E/SL: Tape and Reel, 14LD SOIC package
	SL	= Plastic SOIC (150 mil Body), 14-lead	c) MCP6074-E/ST: 14LD TSSOP package
	SN	= Plastic SOIC, (150 mil Body), 8-lead	d) MCP6074T-E/ST: Tape and Reel, 14LD TSSOP package
	ST	= Plastic TSSOP (4.4mm Body), 14-lead	
	* Y = Nickel palladium gold manufacturing designator. Only available on the TDFN package.		

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NOTES:



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