NB680A

28V, Low Iq, High-Current, Fixed 3.36V, 8A, Synchronous Buck Converter with 100mA LDO and LP# Vout Scaling

DESCRIPTION

The NB680A is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter with a fixed 3.36V Vout and low-power mode voltage scaling. It offers a very compact solution to achieve an 8A continuous output current and a 10A peak output current over a wide input supply range with excellent load and line regulation.

The NB680A operates at high efficiency over a wide output current load range based on MPS proprietary switching loss reduction technology and internal low Ron power MOSFETs.

Adaptive constant-on-time (COT) control mode provides fast transient response and eases loop stabilization. The DC auto-tune loop provides good load and line regulation.

The NB680A provides a fixed 3.3V LDO, which can be used to power the external peripheries, such as the keyboard controller in laptops.

Also, a 250kHz CLK is available on the NB680A. Its output can be used to drive an external charge pump, generating gate drive voltage for the load switches without reducing the main converter's efficiency.

Full protection features include OC limit, OVP, UVP, and thermal shutdown.

NB680A requires a minimum number of external components and is available in a QFN-12 2mm x 3mm package.

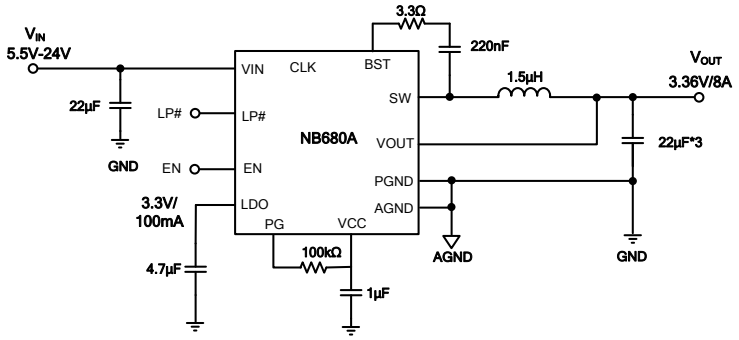
FEATURES

- Wide 5.5V to 28V Operating Input Range
- Fixed 3.36V V_{OUT}(+1.8% of 3.3V)
- LP# Output Voltage Scaling (-3% of 3.3V)
- Ultrasonic Mode
- 100µA Low Quiescent Current
- 8A Continuous and 10A Peak Output Current
- Adaptive COT for Fast Transient
- DC Auto-Tune Loop
- Stable with POSCAP and Ceramic Output Capacitors
- 250 kHz CLK for External Charge Pump
- Built-In 3.3V, 100mA LDO with Switch Over
- 1% Reference Voltage
- Internal Soft Start
- Output Discharge
- 700kHZ Switching Frequency
- OCP, OVP, UVP, and Thermal Shutdown
- Latch-Off Reset via EN or Power Cycle
- QFN-12 2mm x 3mm Package

APPLICATIONS

- Laptop Computers
- Tablet PCs
- Networking Systems
- Servers
- Flat Panel Televisions and Monitors
- Distributed Power Systems

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
NB680AGD	QFN-12 (2mm x 3mm)	*See Below*

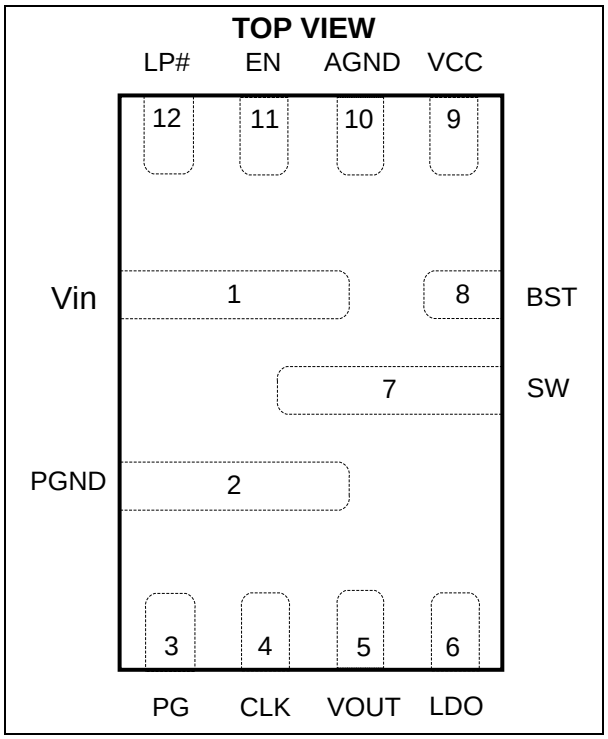
* For Tape & Reel, add suffix –Z (e.g. NB680AGD–Z)

TOP MARKING

APBY
LLL

APB: Product code of NB680AGD
Y: Year code
LLL: Lot number

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 28V
V_{SW} (DC) ..... -1V to 26V
V_{SW} (25ns) ..... -3.6V to 28V
V_{BST} ..... V_{SW} + 4.5V
All other pins ..... -0.3V to +4.5V
Continuous power dissipation (T_A = +25°C) (2)
QFN-12 (2mm x 3mm) 1.8W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply voltage ..... 4.8V to 24V
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-12 (2mm x 3mm) ..... 70 ..... 15 ... °C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will produce an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (quiescent)	I_{IN}	V_{EN} = $V_{LP\#}$ = 3.3V, V_{OUT} = 3.5V		125	145	μA
Supply current (standby)	I_{IN}	V_{EN} = $V_{LP\#}$= 0V, I_{LDO} = 0A		65	85	μA
MOSFET						
High-side switch on resistance	HS_{RDS-ON}			25		mΩ
Low-side switch on resistance	LS_{RDS-ON}			12		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V		0	1	μA
Current Limit						
Low-side valley current limit	I_{LIMIT}		10	11	12	A
Switching Frequency and Timer						
Switching frequency	F_S			700		kHz
Constant on timer	Ton	Vin = 6.4V, $V_{LP\#}$ = 0V	600	710	820	ns
Minimum on time[5]	T_{ON_Min}			32		ns
Minimum off time[5]	T_{OFF_Min}			220		ns
Ultrasonic Mode						
Ultrasonic mode operation period	T_{USM}		20	30	40	μs
Over-Voltage and Under-Voltage Protection						
OVP threshold	V_{OVP}		117%	122%	127%	V_{REF}
UVP-1 threshold	V_{UVP-1}		70%	75%	80%	V_{REF}
UVP-1 foldback timer[5]	T_{UVP-1}			32		μs
UVP-2 threshold	V_{UVP-2}		45%	50%	55%	V_{REF}
Reference and Soft Start						
Vout REF voltage	V_{OUT_REF}	$V_{LP\#}$ = 3.3V	3.32	3.36	3.40	V
		$V_{LP\#}$ = 0V	3.168	3.2	3.234	
Soft-start time	T_{SS}	EN to Vout ready		2	2.5	ms
Enable and UVLO						
Enable rising threshold	V_{EN_H}		1.18	1.28	1.38	V
Enable hysteresis	V_{EN-HYS}			150		mV
EN high limit @ USM	$V_{EN\_H\_USM}$				1.8	V
EN low limit @ Normal	$V_{EN\_L\_Normal}$		2.6			V
Enable input current	I_{EN}	V_{EN} = 2V		4		μA
		V_{EN} = 0V		0		
VIN UVLO rising	VIN_{VTH}			4.4	4.7	V
VIN UVLO hysteresis	VIN_{HYS}			450		mV
LP# Logic						
LP# rising threshold	$V_{LP\#\_H}$		1.18	1.28	1.38	V
LP# hysteresis	$V_{LP\#-HYS}$			150		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
CLK Output						
CLK output high-level voltage	V_{CLKH}	I_{Vclk} = -10mA, $V_{LP\#}$ = 0V	3	3.2	3.4	V
CLK output low-level voltage	V_{CLKL}	I_{Vclk} = 10mA	0	0.05	0.1	V
CLK frequency	F_{CLK}	T_J = 25°C		250		kHz
LDO Regulator						
LDO regulator	V_{LDO}	V_{EN} = 0V,	3.22	3.3	3.38	V
LDO load regulation		V_{EN} = 0V, LDO load = 100mA		2		%
LDO current limit(5)	$I_{LDO\ Limit}$	V_{EN} = 0V, V_{LDO} = 3V		135		mA
Switch Rdson(5)	R_{Switch}	I_{LDO} = 50mA		0.9	1.2	Ω
VCC Regulator						
VCC regulator	V_{CC}		3.5	3.6	3.7	V
VCC load regulation		Icc = 5mA		5		%
Power Good						
PG when FB rising (good)	$PG_{\_Rising(GOOD)}$	VFB rising, percentage of VFB		95		%
PG when FB falling (fault)	$PG_{\_Falling(Fault)}$	VFB falling, percentage of VFB		85		
PG when FB rising (fault)	$PG_{\_Rising(Fault)}$	VFB rising, percentage of VFB		115		
PG when FB falling (good)	$PG_{\_Falling(GOOD)}$	VFB falling, percentage of VFB		105		
Power good low to high delay	PG_{Td}			750		µs
EN low to power good low delay	$PG_{Td\_EN\ low}$				5	µs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3.3V			5	µA
Thermal Protection						
Thermal shutdown(5)	T_{SD}			140		°C
Thermal shutdown hysteresis(5)	T_{SD-HYS}			25		°C

NOTE:

5) Guaranteed by design.

PIN FUNCTIONS

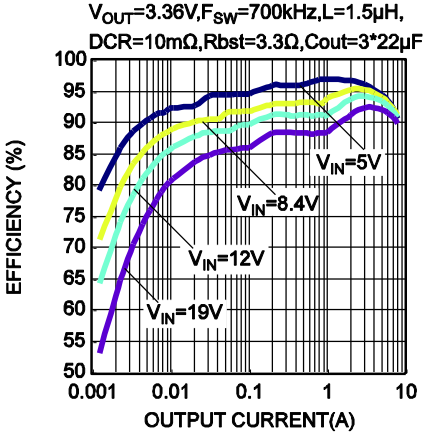
NB680A

PIN #	Name	Description
1	VIN	**Supply voltage.** VIN supplies power for the internal MOSFET and regulator. The NB680A operates from a 4.8V to 24V input rail. An input capacitor is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection. Apply at least two layers for this input trace.
2	PGND	**Power ground.** To make the connection, use wide PCB traces and enough vias to handle the load current.
3	PG	**Power good output.** The output of PG is an open-drain signal. It is high if the output voltage is higher than 95% or lower than 105% of the nominal voltage.
4	CLK	**250kHZ CLK output to drive the external charge pump.** Control by EN also
5	VOUT	**Output voltage of the buck regulator sense.** Connect VOUT to the output capacitor of the regulator directly. VOUT also acts as the input of the internal LDO switch over-power input. Keep the VOUT sensing trace far away from the SW node. Vias should be avoided on the VOUT sensing trace. A >25 mil trace is required.
6	LDO	I**nternal LDO output.** The driver and control circuits are powered from this voltage. Decouple with a minimum 4.7µF ceramic capacitor as close to LDO as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics. Once the PG of the output voltage of the buck regulator is ready, it will switch over the LDO output to reduce power loss.
7	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to the VIN voltage by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW negative during the off-time. The on resistance of the low-side switch and the internal diode fixes the negative voltage. Use wide and short PCB traces to make the connection. Try to minimize the area of the SW pattern.
8	BST	**Bootstrap**. A capacitor connected between SW and BST is required to form a floating supply across the high-side switch driver.
9	VCC	**Internal VCC LDO output.** The driver and control circuits are powered from this voltage. Decouple with a minimum 1µF ceramic capacitor as close to VCC as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
10	AGND	**Signal logic ground.** A Kelvin connection to PGND is required.
11	EN	**BUCK enable**. EN is a digital input that turns the buck regulator on or off. Connect EN with 3V3 through a pull-up resistor or a resistive voltage divider to Vin for automatic start-up. Note that there is a 600kΩ internal pull low resistor. EN threshold also sets mode between USM and normal. When EN is in the range of 1.38V to 1.8V, it enters USM. If EN is in the range of 2.6V to 3.6V, it operates in normal mode.
12	LP#	**Low-power mode control logic.** LP# is pulled high internally. Leave LP# open to enter normal mode with a 3.36V Vout and drive it low to enter low-power mode with lower than a 3.2V Vout.

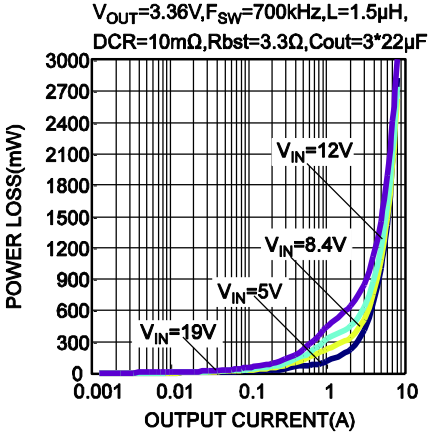
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, LP# = 1, V_{OUT} = 3.36V, L = 1.5µH/10mΩ, f_S = 700kHz, T_J = +25°C, unless otherwise noted.

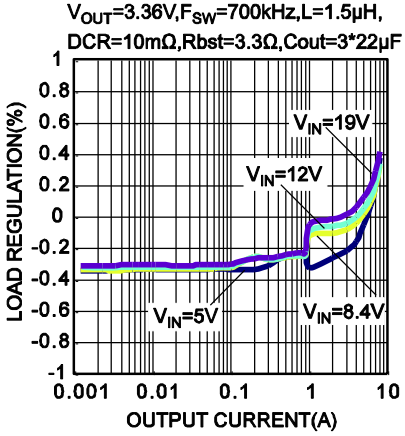
Efficiency vs. Output Current



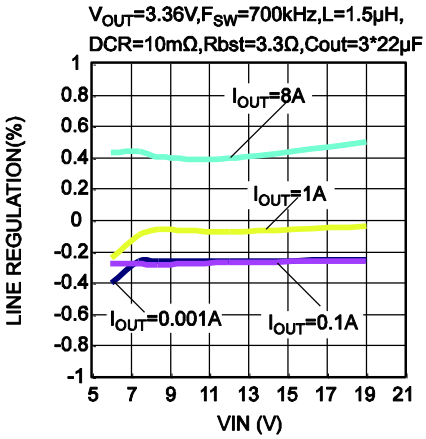
Power Loss vs. Output Current



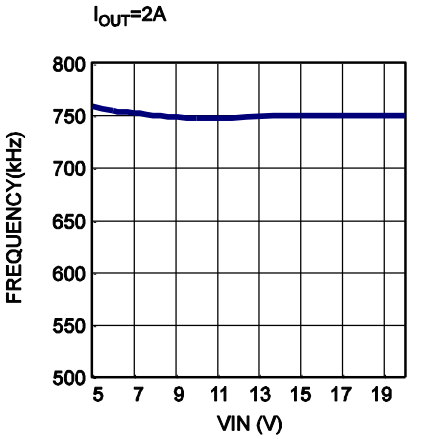
Load Regulation vs. Output Current



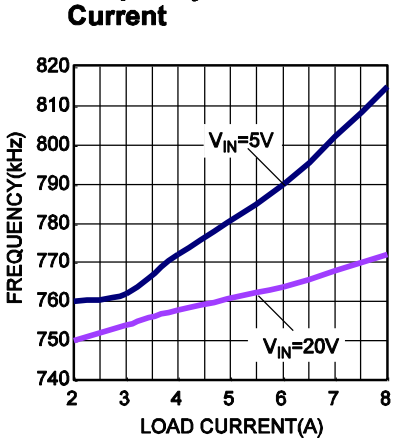
Line Regulation vs. VIN



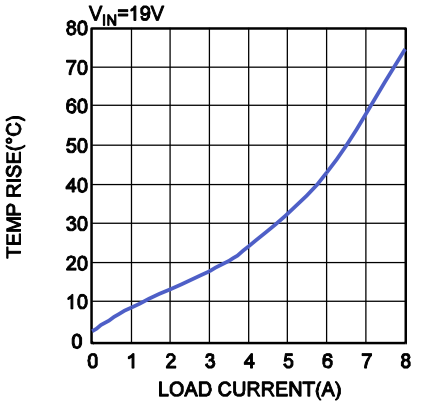
Frequency vs. VIN



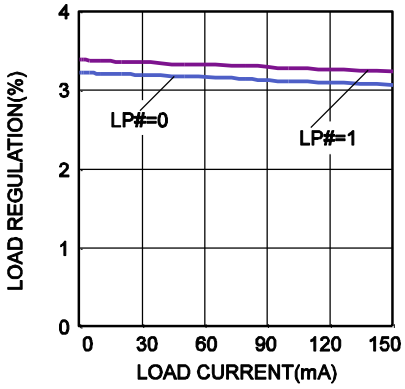
Frequency vs. Load Current



Temp Rise vs. Load Current



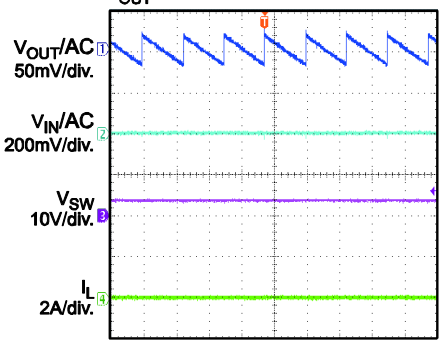
LDO Load Regulation vs. Load Current



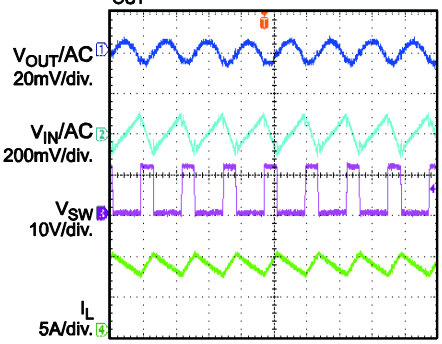
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, LP# = 1, V_{OUT} = 3.36V, L = 1.5µH/10mΩ, f_S = 700kHz, T_J = +25°C, unless otherwise noted.

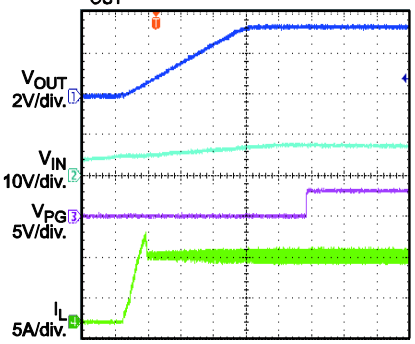
Input/Output Voltage Ripple
I_{OUT}=0A



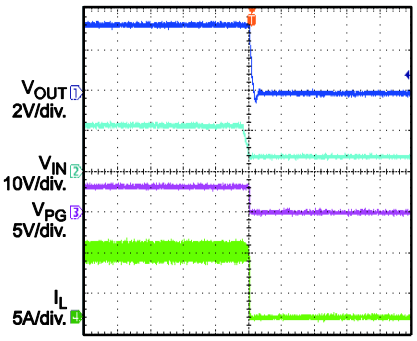
Input/Output Voltage Ripple
I_{OUT}=8A



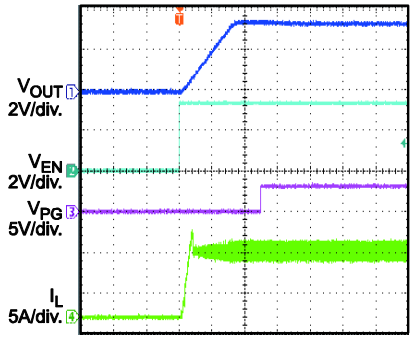
Power Good through VIN Start-Up
I_{OUT}=8A



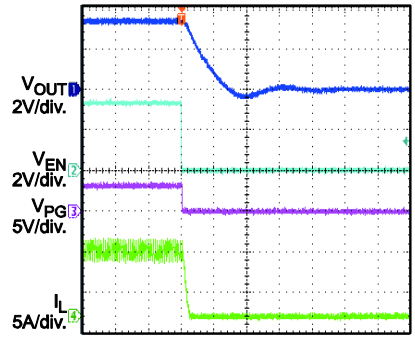
Power Good through VIN Shutdown
I_{OUT}=8A



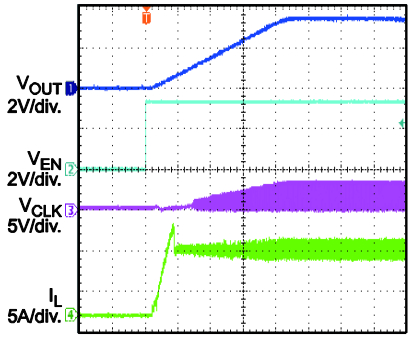
Power Good through EN Start-Up
I_{OUT}=8A



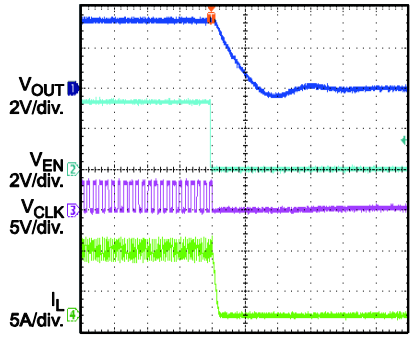
Power Good through EN Shutdown
I_{OUT}=8A



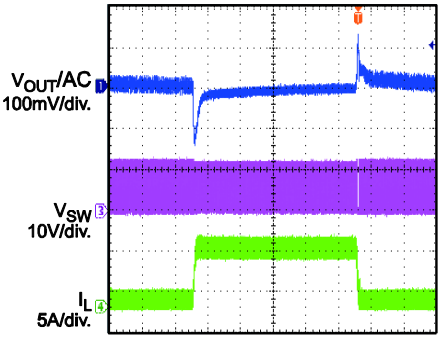
CLK Start-Up through EN
I_{OUT}=8A



CLK Shutdown through EN
I_{OUT}=8A



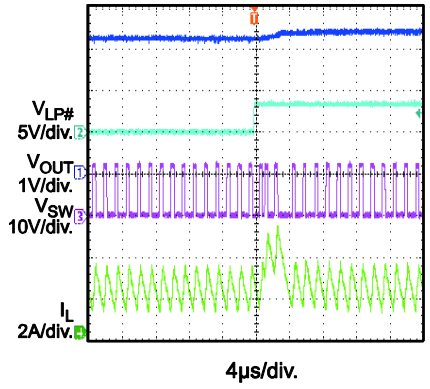
Transient
V_{IN}=12V,L=1.5uH,C_{OUT}=66µF,
I_{OUT}=0.8A-7.2A @1.6A/µs



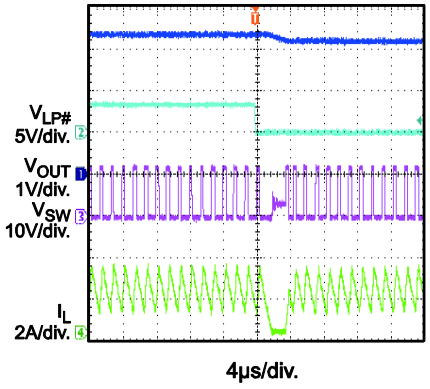
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, LP# = 1, V_{OUT} = 3.36V, L = 1.5µH/10mΩ, f_S = 700kHz, T_J = +25°C, unless otherwise noted.

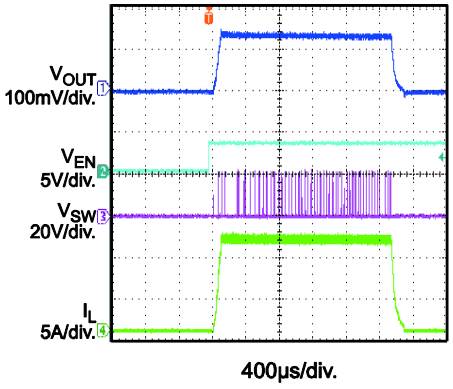
Transient LP# On
V_{OUT}=3.2V->3.36V, I_{OUT}=2A



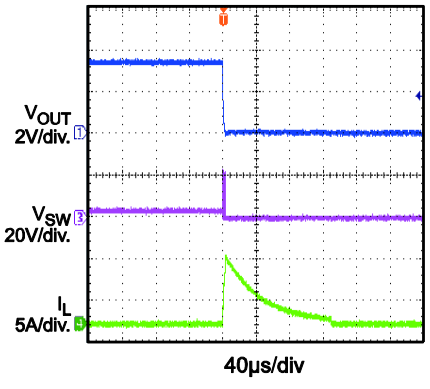
Transient LP# Off
V_{OUT}=3.2V->3.36V, I_{OUT}=2A



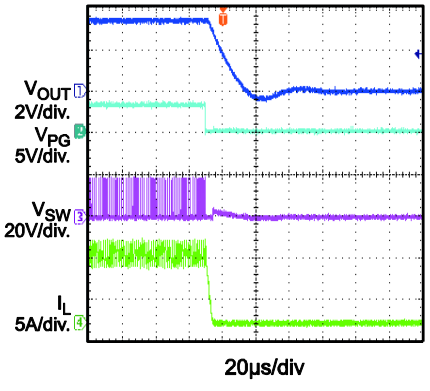
Short-Circuit Protection with EN
V_{IN}=22V



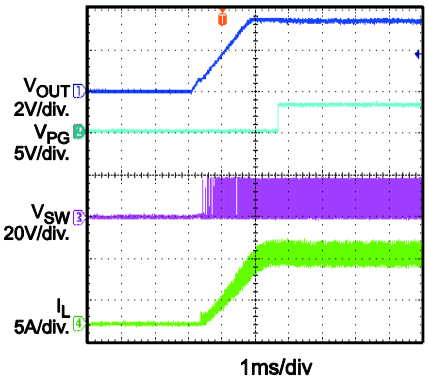
Short-Circuit Protection
V_{IN}=22V



Thermal Shutdown
V_{IN}=19V, I_{OUT}=8A



Thermal Recovery
V_{IN}=19V,I_{OUT}=8A



FUNCTIONAL BLOCK DIAGRAM

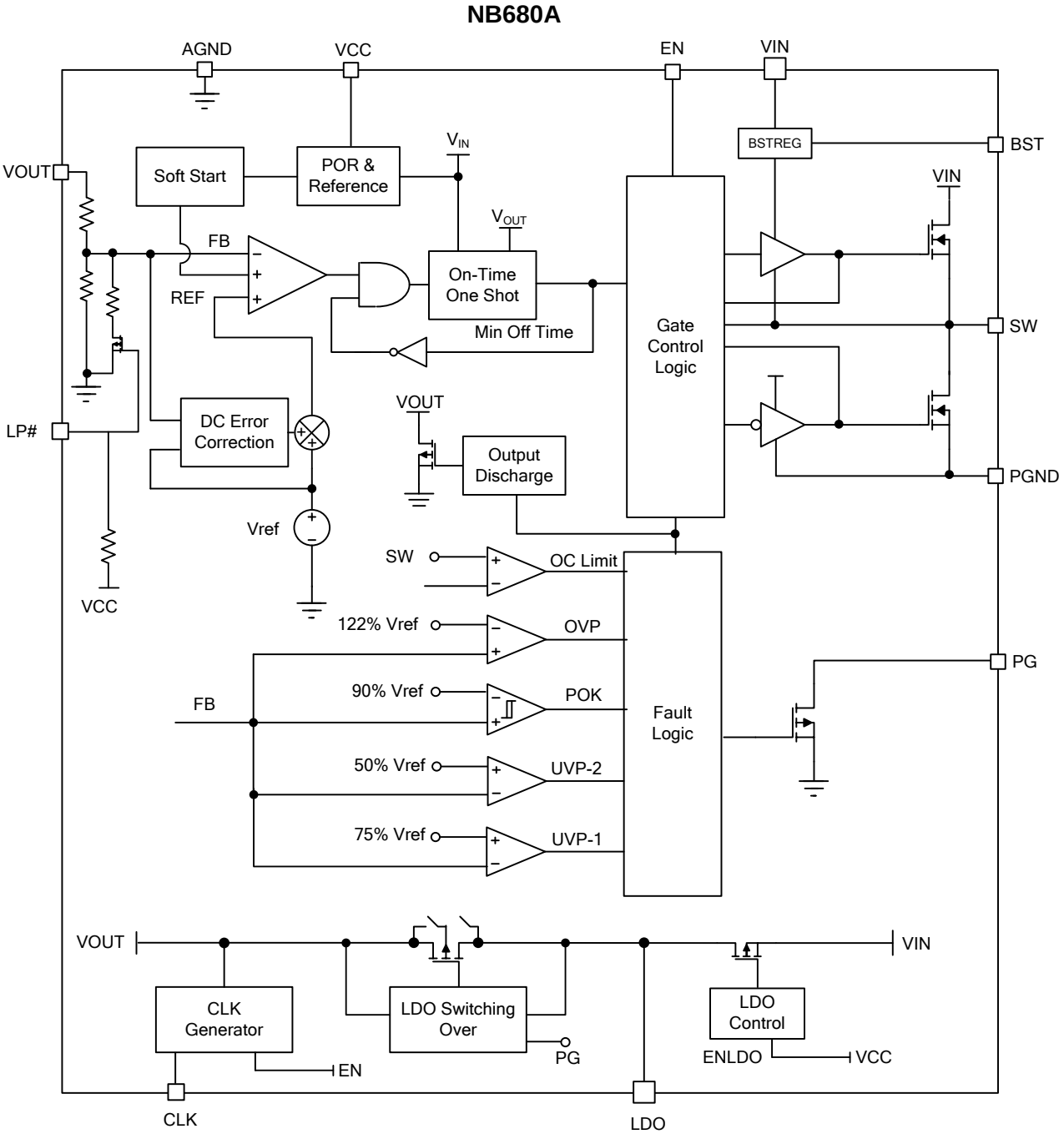


Figure 1: Functional Block Diagram

OPERATION

PWM Operation

The NB680A is a fully integrated, synchronous, rectified, step-down, switch mode converter with a fixed 3.36V output. Constant-on-time (COT) control provides fast transient response and eases loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The on period is determined by the output voltage and the input voltage to make the switching frequency fairly constant over the input voltage range.

After the on period elapses, the HS-FET is turned off or enters an off state. It is turned on again when V_{FB} drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its off state to minimize conduction loss. A dead short occurs between the input and GND if both the HS-FET and the LS-FET are turned on at the same time (shoot-through). In order to avoid shoot-through, a dead time (DT) is generated internally between the HS-FET off and the LS-FET on period or the LS-FET off and the HS-FET on period.

Internal compensation is applied for COT control for stable operation even when ceramic capacitors are used as output capacitors. This internal compensation improves the jitter performance without affecting the line or load regulation.

Heavy-Load Operation (CCM)

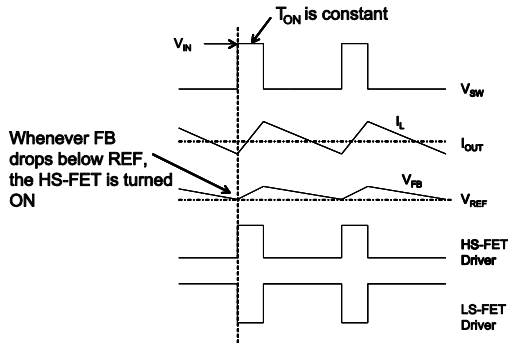


Figure 2: CCM Operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above zero amps (see Figure 2). When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval. When the HS-FET is turned off, the LS-FET is turned on until the next period.

In CCM operation, the switching frequency is fairly constant (PWM mode).

Light-Load Power Save Mode (DCM)

When the load decreases, the inductor current will decrease as well. Once the inductor current reaches zero, the part transitions from CCM to discontinuous conduction mode (DCM).

Discontinuous conduction mode is shown in Figure 3. When V_{FB} is below V_{REF}, the HS-FET is turned on for a fixed interval, which is determined by the one-shot on-timer. See Equation (1). When the HS-FET is turned off, the LS-FET is turned on until the inductor current reaches zero. In DCM operation, the V_{FB} does not reach V_{REF} when the inductor current is approaching zero. The LS-FET driver turns into tri-state (high Z) when the inductor current reaches zero. A current modulator takes over the control of the LS-FET and limits the inductor current to less than -1mA. Hence, the output capacitors discharge slowly to GND through the LS-FET. As a result, the efficiency during a light-load condition is improved greatly. The HS-FET is not turned on as frequently during a light-load condition as it is during a heavy-load condition (skip mode).

At a light-load or no-load condition, the output drops very slowly, and the NB680A reduces the switching frequency naturally, achieving high efficiency at light load.

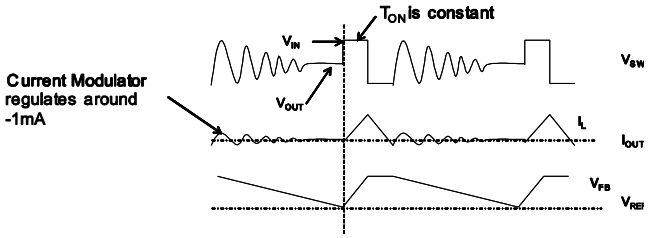


Figure 3—DCM Operation

As the output current increases from the light-load condition, the time period within which the current modulator regulates becomes shorter. The HS-FET is turned on more frequently. Hence, the switching frequency increases accordingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

The device enters PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

DC Auto-Tune Loop

NB680A applies a DC auto-tune loop to balance the DC error between V_{FB} and V_{REF} by adjusting the comparator input REF to make V_{FB} always follow V_{REF}. This loop is quite small, so it improves the load and line regulation without affecting the transient performance. The relationship between V_{FB}, V_{REF}, and REF is shown in Figure 4.

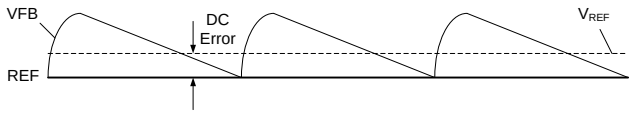


Figure 4: DC Auto-Tune Loop Operation

Ultrasonic Mode (USM)

Ultrasonic mode (USM) is designed to keep the switching frequency above an audible frequency area during light-load or no-load conditions. Once the part detects both the HS-FET and the LS-FET are off (for about 32µs), it decreases the Ton so as to keep Vout under regulation with optimal efficiency. If the load continues to reduce, then the part discharges the Vout to make sure the FB is smaller than 102% of the internal reference. The HS-FET will turn on again once the internal FB reaches the V_{REF} and then stops switching.

USM is selected by the EN voltage level. When EN is in the range of 1.38V to 1.8V, it enters USM. If EN is in the range of 2.6V to 3.6V, it is in normal mode.

Configuring the EN Control

The NB680A has EN pins to control the on/off of the internal regulators and CLK.

For the NB680A, the 3V3 LDO is always on when Vin passes UVLO. EN is used to control both the buck regulator and the CLK (see Table 1).

Table 1 : EN Control

State	EN	VCC	VOUT	CLK	LDO
S0	1	ON	ON	ON	ON
S3/S5	0	ON	OFF	OFF	ON

For automatic start-up, EN can be pulled up to the input voltage through a resistive voltage divider. Refer to the “UVLO Protection” section for more details.

Configuring the LP# Control

The NB680A implements a voltage scaling function on low-power mode by controlling LP# (see Table 3).

Table 3 : LP# Control

State	LP#	VOUT(V)
S0	1	3.36
S3/S5	0	3.2

Soft Start (SS)

The NB680A employs a soft-start (SS) mechanism to ensure smooth output during power-up. When EN goes high, the internal reference voltage ramps up gradually; hence, the output voltage ramps up smoothly as well. Once the reference voltage reaches the target value, the soft start finishes, and it enters steady-state operation.

If the output is pre-biased to a certain voltage during start-up, the IC will disable the switching of both the high-side and the low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the internal FB node.

3.3V Linear Regulator

There is a built-in 100mA standby linear regulator with a fixed output at 3.3V, controlled by VIN UVLO. Once Vin passes its UVLO, it is turned on; the 3.3V LDO is not controlled by EN or LP#. This LDO is intended mainly for an auxiliary 3.3V supply for the notebook system in standby mode.

Add a ceramic capacitor with a value between 4.7μF and 22μF close to the LDO pins to stabilize the LDOs.

LDO Switch Over

When the output voltage becomes higher than 3.15V, and the power good (PG) is OK, the internal LDO regulator is shut off, and the LDO output is connected to VOUT by the internal switch-over MOSFET. This helps reduce the power loss from the LDO.

CLK for Charge Pump

The 250kHz CLK signal drives an external charge pump circuit to generate approximately 10V-12V DC voltage. The CLK voltage becomes available once Vin is higher than the UVLO threshold, and EN is pulled high (see Figure 5).

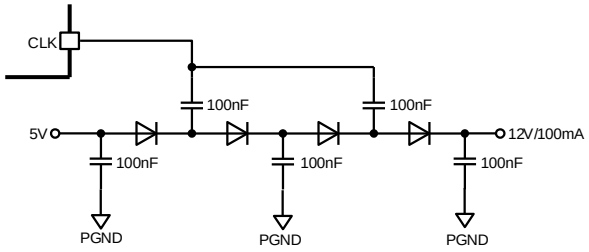


Figure 5: Charge Pump Circuit

Power Good (PG)

The NB680A has power-good (PG) output used to indicate whether the output voltage of the buck regulator is ready. PG is the open drain of a MOSFET. It should be connected to V_{CC} or other voltage source through a resistor (e.g.,100k). After the input voltage is applied, the MOSFET is turned on, so PG is pulled to GND before SS is ready. Once the FB voltage rises to 95% of the REF voltage, PG is pulled high after 750μs.

When the FB voltage drops to 85% of the REF voltage, PG is pulled low.

Over-Current Protection (OCP)

NB680A has cycle-by-cycle over-current limiting control. The current-limit circuit employs a "valley" current-sensing algorithm. The part uses the Rds(on) of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle.

The trip level is fixed internally. The inductor current is monitored by the voltage between GND and SW. GND is used as the positive current sensing node, so GND should be connected to the source terminal of the bottom MOSFET.

Since the comparison is done during the HS-FET off and the LS-ET on state, the OC trip level sets the valley level of the inductor current. Thus, the load current at an over-current threshold (I_{OC}) can be calculated with Equation (2):

$$I_{OC} = I\_limit + \frac{\Delta I_{inductor}}{2} \quad (2)$$

In an over-current condition, the current to the load exceeds the current to the output capacitor; thus the output voltage tends to fall off. Eventually, it ends up crossing the under-voltage protection threshold and shuts down. Fault latching can be re-set by EN going low or the power cycling of VIN.

Over/Under-Voltage Protection (OVP/UVP)

The NB680A monitors the output voltage to detect over and under voltage. Once the feedback voltage becomes higher than 122% of the target voltage, the OVP comparator output goes high, and the circuit latches as the HS-FET driver turns off, and the LS-FET driver turns on, acting as an -2A current source.

To protect the part from damage, there is an absolute OVP on VOUT, usually set at 6.2V. Once the Vout > 6.2V, the controller turns off both the HS-FET and the LS-FET. This protection is not latched off; it will keep switching once the Vout returns to its normal value.

When the feedback voltage drops below 75% of V_{REF} but remains higher than 50% of V_{REF}, the UVP-1 comparator output goes high. The part is latched if the FB voltage remains in this range for about 32μs (latching the HS-FET off and the LS-FET on). The LS-FET remains on until the inductor current reaches zero. During this period, the valley current limit helps control the inductor current.

When the feedback voltage drops below 50% of V_{REF}, the UVP-2 comparator output goes high. The part latches off directly after the comparator and logic delay (latching the HS-FET off and the LS-FET on). The LS-FET remains on until the inductor current reaches zero. Fault latching can be re-set by EN going low or the power cycling of VIN.

UVLO Protection

The part starts up only when the Vin voltage is higher than the UVLO rising threshold voltage. The part shuts down when VIN is lower than the Vin falling threshold. The UVLO protection is non-latch off. Fault latching can be re-set by EN going low or the power cycling of VIN.

If an application requires a higher under-voltage lockout (UVLO), use EN to adjust the input voltage UVLO by using two external resistors (see Figure 6). Note that there is a 600kΩ internal pull low resistor on the EN Pin. The Calculation of the two resistors needs to consider this resistor.

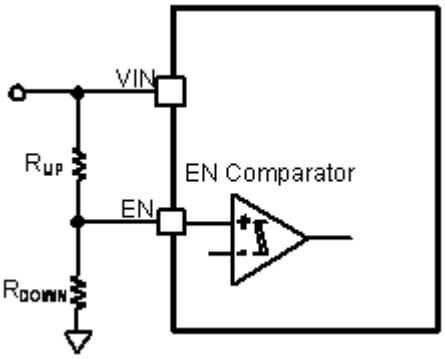


Figure 6: Adjustable UVLO

To avoid too much sink current on EN when Rdown is not applied, the EN resistor (Rup) is usually in the range of 1M-2MΩ. A typical pull-up resistor is 2MΩ.

Thermal Shutdown

Thermal shutdown is employed in the NB680A. The junction temperature of the IC is monitored internally. If the junction temperature exceeds the threshold value (140ºC, typically), the converter shuts off. This is a non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to about 115ºC, it initiates a SS.

Output Discharge

NB680A discharges the output when EN is low, or the controller is turned off by the protection functions UVP, OCP, OVP, UVLO, and thermal shutdown. The part discharges outputs using an internal 6Ω MOSFET from Vout Pin, so it is suggest that the Vout trace need to be over 20mil.

APPLICATION INFORMATION

Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated using Equation (3) and Equation (4):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (3)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (4)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated using Equation (5) and Equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (6)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated using Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (7)$$

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated using Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{\ 2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (8)$$

When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (9)$$

The maximum output capacitor limitation should be considered in design application. For a small soft-start time period (if the output capacitor value is too high), the output voltage cannot reach the design value during the soft-start time, causing it to fail to regulate. The maximum output capacitor value (C_{o_max}) can be limited approximately using Equation (10):

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (10)$$

Where I_{LIM_AVG} is the average start-up current during the soft-start period, and T_{ss} is the soft-start time.

Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor results in less ripple current, resulting in a lower output ripple voltage. However, a larger value inductor has a larger physical footprint, a higher series resistance, and/or a lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 50% of the maximum output current, with the peak inductor current below the maximum switch current limit. The inductance value can be calculated using Equation (11):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current (including short current), so it is recommended to choose Isat > 11A.

PCB Layout Guidelines

Efficient PCB layout is critical for optimum IC performance. For best results, refer to Figure 7 and follow the guidelines below:

1. Place the high current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Place the input capacitors as close to IN and GND as possible.
3. Place the decoupling capacitor as close to VCC and GND as possible. Keep the switching node (SW) short and away from the feedback network.
4. Keep the BST voltage path as short as possible with a > 25 mil trace.
5. Keep the IN and GND pads connected with a large copper plane to achieve better thermal performance. Add several vias with a 10mil drill/18mil copper width close to the IN and GND pads to help thermal dissipation.
6. Keep the Vout sense trace over 20mil
7. A 4-layer layout is strongly recommended to achieve better thermal performance.

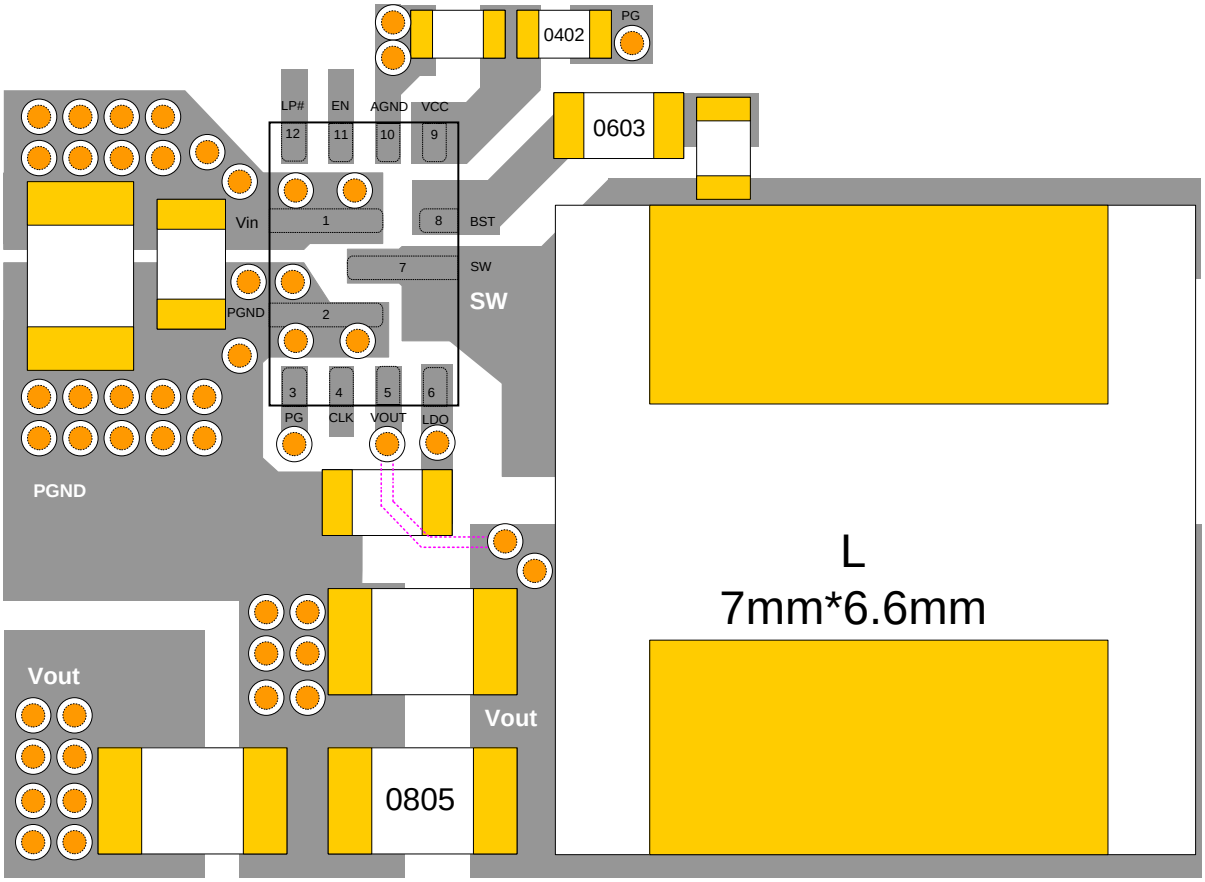


Figure 7: Recommended PCB Layout

TYPICAL APPLICATION

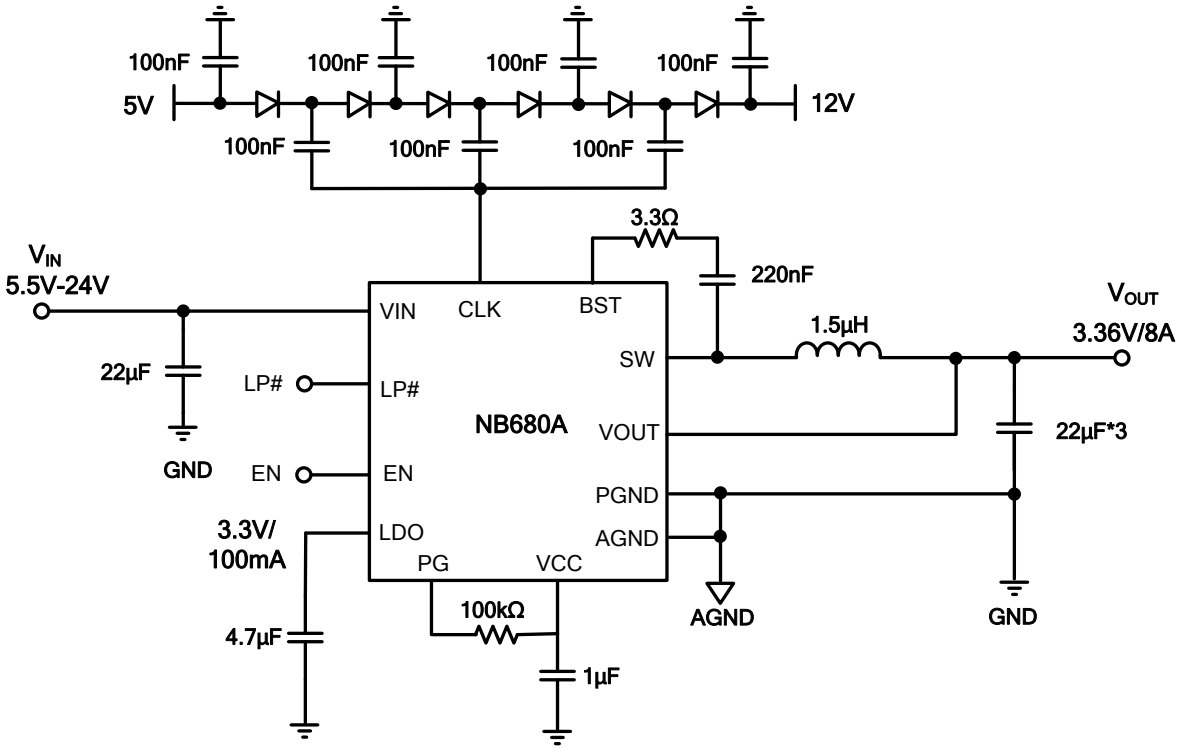
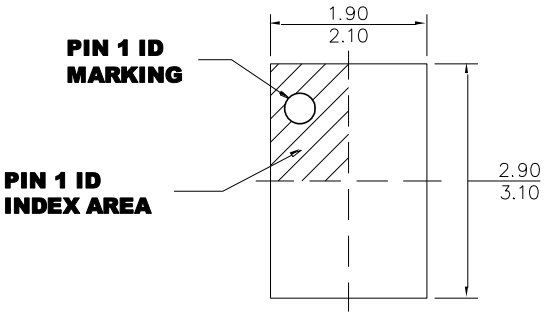


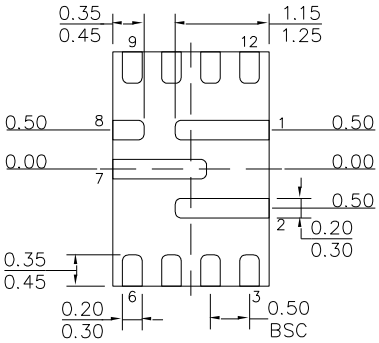
Figure 8: Typical Application Schematic with Ceramic Output Capacitors

PACKAGE INFORMATION

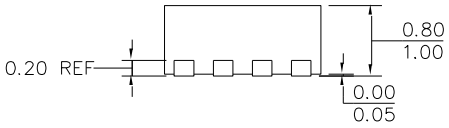
QFN-12 (2mm x 3mm)



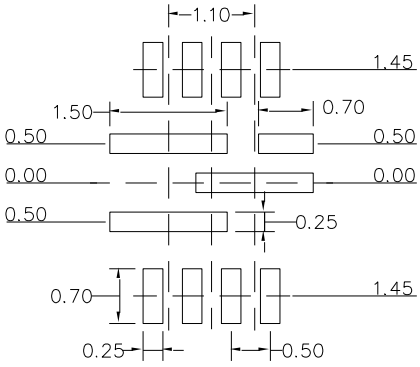
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.