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December 2014

FCPF400N60 N-Channel SuperFET[®] II MOSFET 600 V, 10 A, 400 m Ω

Features

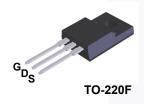
- 650 V @ T_{.1} = 150°C
- Typ. $R_{DS(on)}$ = 350 m Ω
- Ultra Low Gate Charge (Typ. Q_g = 28 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 90 pF)
- · 100% Avalanche Tested
- · RoHS Compliant

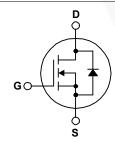
Applications

- · LCD / LED / PDP TV Lighting
- · Solar Inverter
- AC-DC Power Supply

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter		FCPF400N60	Unit
V_{DSS}	Drain to Source Voltage			600	V
V	Coto to Source Valtage	- DC		±20	V
V _{GSS} Gate to Source Volta	Gate to Source Voltage	- AC	(f > 1 Hz)	±30	v
. \	Drain Current	- Continuous (T _C = 25°C)	/	10*	Α
I _D Drain Current		- Continuous (T _C = 100°C)		6.3*	
I _{DM}	Drain Current	- Pulsed	(Note 1)	30*	Α
E _{AS}	Single Pulsed Avalanche En	ergy	(Note 2)	211.6	mJ
I _{AR}	Avalanche Current		(Note 1)	2.3	Α
E _{AR}	Repetitive Avalanche Energy	/	(Note 1)	1.06	mJ
dv/dt	MOSFET dv/dt			100	V/ns
αν/αι	Peak Diode Recovery dv/dt		(Note 3)	20	V/IIS
D	Dower Discipation	(T _C = 25°C)		31	W
P_{D}	Power Dissipation - Derate Above 25°C			0.25	W/°C
T _J , T _{STG}	Operating and Storage Temp	perature Range		-55 to +150	°C
TL	Maximum Lead Temperature	e for Soldering, 1/8" from Case for 5 S	Seconds	300	°C

^{*}Drain current limited by maximum junction temperature.

Thermal Characteristics

Symbol	Parameter FCPF400N60			
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	4.0	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	C/VV	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCPF400N60	FCPF400N60	TO-220F	Tube	N/A	N/A	50 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Chara	cteristics					
D\/	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 25^{\circ}\text{C}$	600	-	-	V
BV _{DSS} Dr	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 10 \text{ mA}, T_J = 150^{\circ}\text{C}$	650	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	0.67	-	V/°C
BV _{DS}	Drain-Source Avalanche Breakdown Voltage	V _{GS} = 0 V, I _D = 10 A	-	700	-	V
1	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	-	-	1	
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 480 \text{ V}, T_{C} = 125^{\circ}\text{C}$	-	0.97	-	μА
I _{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2.5	-	3.5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$	-	0.35	0.40	Ω
9 _{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 5 \text{ A}$	_	11	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V = 25 V V = 0 V	- \	1180	1580	pF
Coss	Output Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		860	1144	pF
C _{rss}	Reverse Transfer Capacitance			43	54	pF
Coss	Output Capacitance	V _{DS} = 380 V, V _{GS} = 0 V, f = 1 MHz	-	22	-	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 480 V, V _{GS} = 0 V	-	90	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V _{DS} = 380 V, I _D = 5 A,	-	28	38	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	10	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	- /	1	-	Ω

Switching Characteristics

t _{d(on)}	Turn-On Delay Time			13	37	ns
t _r	Turn-On Rise Time	$V_{DD} = 380 \text{ V}, I_D = 5 \text{ A},$	/ -	7	24	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_G = 4.7 \Omega$	-	43	95	ns
t _f	Turn-Off Fall Time	(Note 4)	-	6	21	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current			-	10	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-		30	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 5 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 5 A,	-	240	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	2.7	_	μС

Notes

- ${\it 1. Repetitive\ rating: pulse-width\ limited\ by\ maximum\ junction\ temperature.}$
- 2. I $_{AS}$ = 2.3 A, V $_{DD}$ = 50 V, R $_{G}$ = 25 Ω , starting T $_{J}$ = 25°C.
- 3. I $_{SD} \leq$ 5 A, di/dt \leq 200 A/ μ s, V $_{DD} \leq$ BV $_{DSS}$, starting T $_{J}$ = 25°C.
- 4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

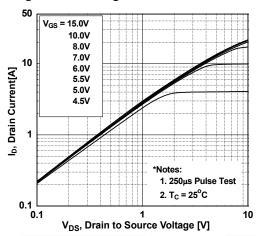


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

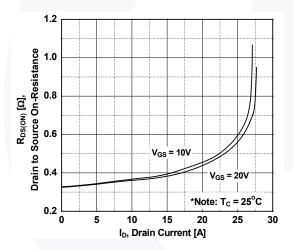


Figure 5. Capacitance Characteristics

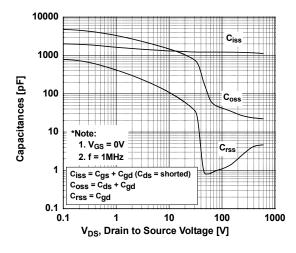


Figure 2. Transfer Characteristics

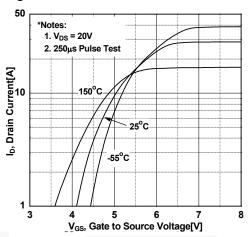


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

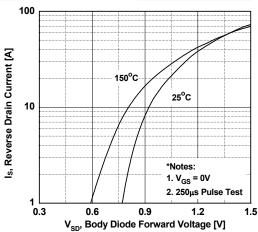
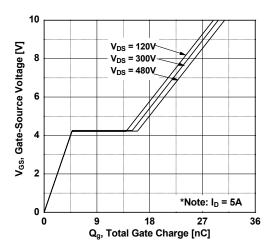


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

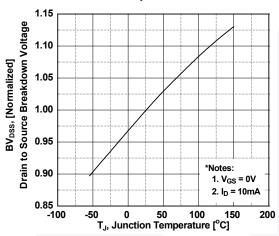


Figure 9. Maximum Safe Operating Area

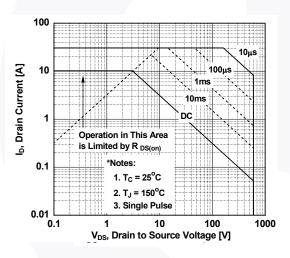


Figure 11. Eoss vs. Drain to Source Voltage

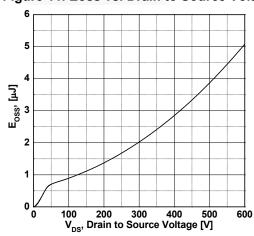


Figure 8. On-Resistance Variation vs. Temperature

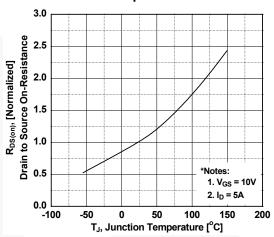
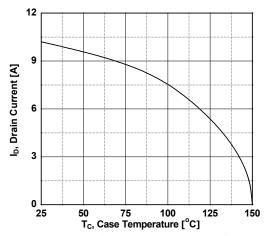
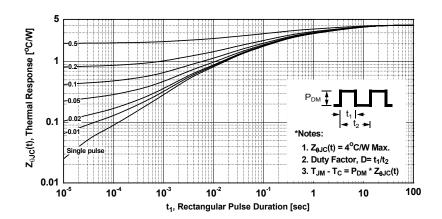


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



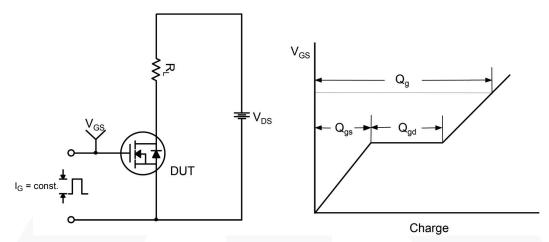


Figure 13. Gate Charge Test Circuit & Waveform

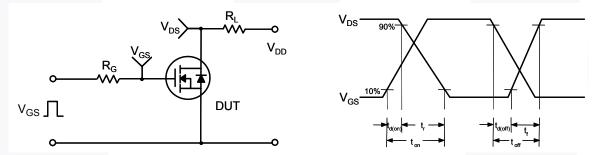


Figure 14. Resistive Switching Test Circuit & Waveforms

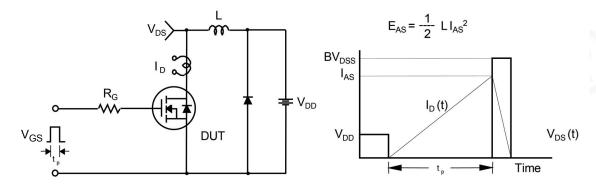


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

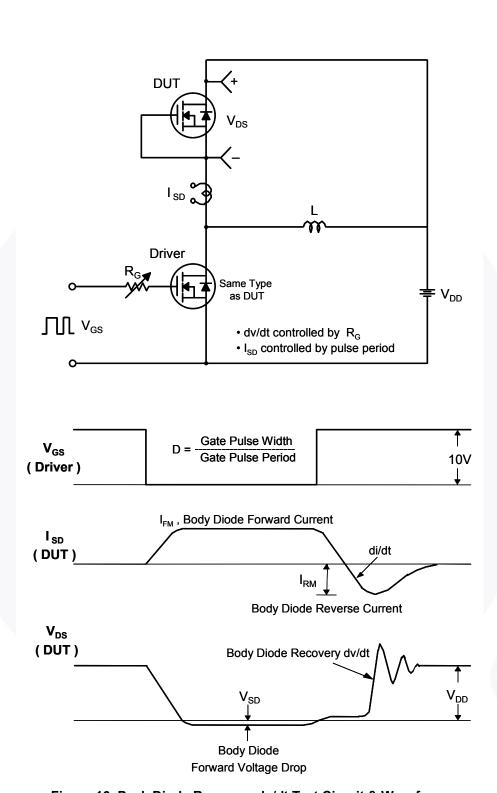


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

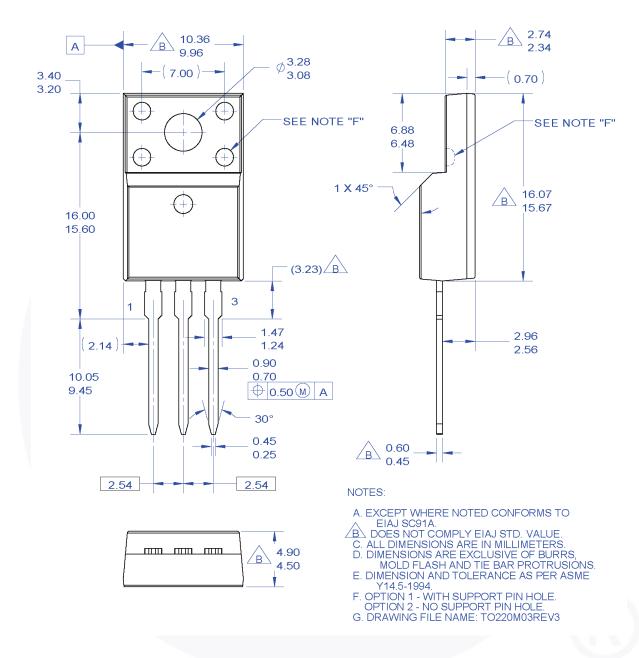


Figure 17. TO220, Molded, 3-Lead, Full Pack, EIAJ SC91, Straight Lead

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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