



SNx4LVC573A Octal Transparent D-Type Latches With 3-State Outputs

1 Features

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.9 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- I_{off} Supports Live Insertion, Partial Power Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- PC, Notebook
- Network Switch
- Health & Fitness/Wearables
- Telecom Infrastructure
- Electronic Point of Sales

3 Description

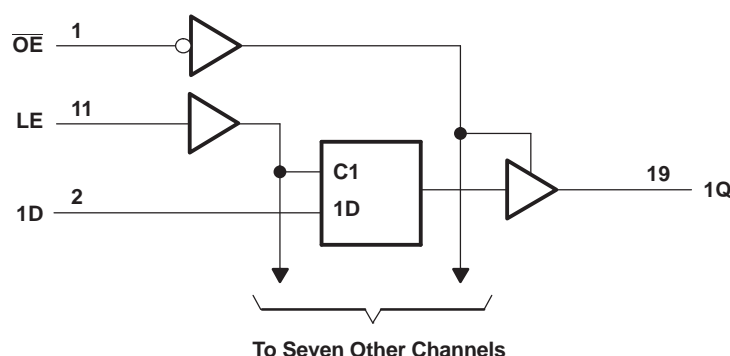
The SN54LVC573A octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC573A octal transparent D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation. These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|------------|-----------------|
| SN74LVC573A | PDIP (20) | 25.40 x 6.35 mm |
| | VQGN (20) | 4.50 x 3.50 mm |
| | SOIC (20) | 12.80 x 7.50 mm |
| | SSOP (20) | 7.20 x 5.30 mm |
| | TVSOP (20) | 5.00 x 4.40 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



Pin numbers shown are for the DB, DGV, DW, FK, J, N, NS, PW, RGY, and W packages.



Table of Contents

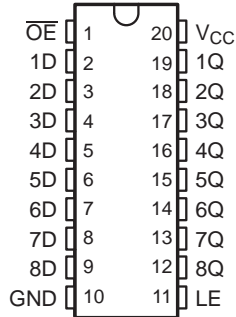
| | | | |
|--|----------|--|-----------|
| 1 Features | 1 | 9 Detailed Description | 9 |
| 2 Applications | 1 | 9.1 Overview | 9 |
| 3 Description | 1 | 9.2 Functional Block Diagram | 9 |
| 4 Simplified Schematic | 1 | 9.3 Feature Description | 9 |
| 5 Revision History | 2 | 9.4 Device Functional Modes | 9 |
| 6 Pin Configuration and Functions | 3 | 10 Applications and Implementation | 10 |
| 7 Specifications | 4 | 10.1 Application Information | 10 |
| 7.1 Absolute Maximum Ratings | 4 | 10.2 Typical Application | 10 |
| 7.2 Handling Ratings | 4 | 11 Power Supply Recommendations | 11 |
| 7.3 Recommended Operating Conditions | 5 | 12 Layout | 11 |
| 7.4 Thermal Information | 5 | 12.1 Layout Guidelines | 11 |
| 7.5 Electrical Characteristics | 6 | 12.2 Layout Example | 11 |
| 7.6 Timing Requirements, SN54LVC573A | 6 | 13 Device and Documentation Support | 12 |
| 7.7 Timing Requirements, SN74LVC573A | 6 | 13.1 Related Links | 12 |
| 7.8 Switching Characteristics, SN54LVC573A | 7 | 13.2 Trademarks | 12 |
| 7.9 Switching Characteristics, SN74LVC573A | 7 | 13.3 Electrostatic Discharge Caution | 12 |
| 7.10 Operating Characteristics | 7 | 13.4 Glossary | 12 |
| 7.11 Typical Characteristics | 7 | 14 Mechanical, Packaging, and Orderable Information | 12 |
| 8 Parameter Measurement Information | 8 | | |

5 Revision History

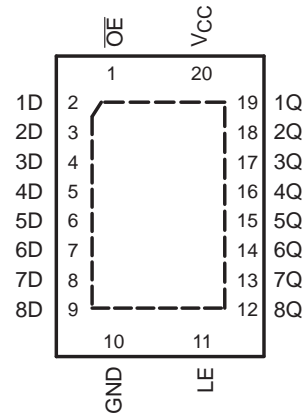
| Changes from Revision R (September 2005) to Revision S | Page |
|--|------|
| • Removed Ordering Information table. | 1 |
| • Updated device temperature ratings. | 4 |
| • Added Handling Ratings. | 4 |
| • Added Typical Characteristics. | 7 |
| • Added Detailed Description section. | 9 |
| • Added Applications and Implemetation section. | 10 |
| • Added Power Supply Recommendations section. | 11 |
| • Added Layout section. | 11 |

6 Pin Configuration and Functions

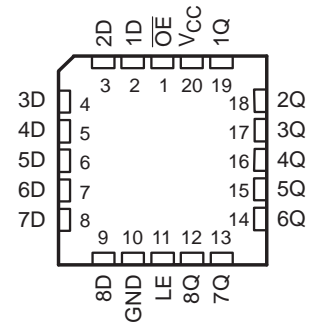
SN54LVC573A . . . J OR W PACKAGE
SN74LVC573A . . . DB, DGV, DW, N,
NS, OR PW PACKAGE
(TOP VIEW)



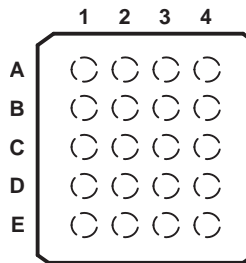
SN74LVC573A . . . RGY PACKAGE
(TOP VIEW)



SN54LVC573A . . . FK PACKAGE
(TOP VIEW)



GQN OR ZQN PACKAGE
(TOP VIEW)



Pin Functions

| NAME | PIN | | | DESCRIPTION |
|-----------------|-----------------------------|---|-------------|--------------|
| | SN54LVC573A J, W, AND FK | SN74LVC573A DB, DGV, DW, N, NS, PW, AND RGY | GQN AND ZQN | |
| \overline{OE} | 1 | 1 | A2 | Enable Pin |
| 1D | 2 | 2 | A1 | Input 1 |
| 2D | 3 | 3 | B3 | Input 2 |
| 3D | 4 | 4 | B1 | Input 3 |
| 4D | 5 | 5 | C2 | Input 4 |
| 5D | 6 | 6 | C1 | Input 5 |
| 6D | 7 | 7 | D3 | Input 6 |
| 7D | 8 | 8 | D1 | Input 7 |
| 8D | 9 | 9 | E2 | Input 8 |
| GND | 10 | 10 | E1 | Ground Pin |
| LE | 11 | 11 | E3 | Latch Enable |
| 8Q | 12 | 12 | E4 | Output 8 |
| 7Q | 13 | 13 | D2 | Output 7 |
| 6Q | 14 | 14 | D4 | Output 6 |
| 5Q | 15 | 15 | C3 | Output 5 |
| 4Q | 16 | 16 | C4 | Output 4 |
| 3Q | 17 | 17 | B2 | Output 3 |
| 2Q | 18 | 18 | B4 | Output 2 |
| 1Q | 19 | 19 | A4 | Output 1 |
| V_{CC} | 20 | 20 | A3 | Power Pin |

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|-----------------|---|-----------------------------------|------|-----------------------|------|
| V _{CC} | Supply voltage | | –0.5 | 6.5 | V |
| V _I | Input voltage range ⁽²⁾ | | –0.5 | 6.5 | V |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | | –0.5 | 6.5 | V |
| V _O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | | –0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | | –50 | mA |
| I _{OK} | Output clamp current | V _O < 0 | | –50 | mA |
| I _O | Continuous output current | | | ±50 | mA |
| | Continuous current through V _{CC} or GND | | | ±100 | mA |
| θ _{JA} | Package thermal impedance | DB package ⁽⁴⁾ | | 70 | °C/W |
| | | DGV package ⁽⁴⁾ | | 92 | |
| | | DW package ⁽⁴⁾ | | 58 | |
| | | GQN or ZQN package ⁽⁴⁾ | | 78 | |
| | | N package ⁽⁴⁾ | | 69 | |
| | | NS package ⁽⁴⁾ | | 60 | |
| | | PW package ⁽⁴⁾ | | 83 | |
| | | RGY package ⁽⁵⁾ | | 37 | |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

7.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|--------------------|---------------------------|--|-----|------|------|
| T _{stg} | Storage temperature range | | –65 | 150 | °C |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | 0 | 2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | 0 | 1000 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as 500 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as 250 V may actually have higher performance.

7.3 Recommended Operating Conditions⁽¹⁾

| | | | SN54LVC573A | | SN74LVC573A | | UNIT |
|-----------------|------------------------------------|------------------------------------|-------------|-----------------|------------------------|-----------------|------|
| | | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | Operating | 2 | 3.6 | 1.65 | 3.6 | V |
| | | Data retention only | 1.5 | | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 1.65 V to 1.95 V | | | 0.65 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | | | 1.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | 2 | | 2 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 1.65 V to 1.95 V | | | 0.35 × V _{CC} | | V |
| | | V _{CC} = 2.3 V to 2.7 V | | | 0.7 | | |
| | | V _{CC} = 2.7 V to 3.6 V | | 0.8 | 0.8 | | |
| V _I | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| V _O | Output voltage | High or low state | 0 | V _{CC} | 0 | V _{CC} | V |
| | | 3-state | 0 | 5.5 | 0 | 5.5 | |
| I _{OH} | High-level output current | V _{CC} = 1.65 V | | | | –4 | mA |
| | | V _{CC} = 2.3 V | | | | –8 | |
| | | V _{CC} = 2.7 V | | –12 | | –12 | |
| | | V _{CC} = 3 V | | –24 | | –24 | |
| I _{OL} | Low-level output current | V _{CC} = 1.65 V | | | | 4 | mA |
| | | V _{CC} = 2.3 V | | | | 8 | |
| | | V _{CC} = 2.7 V | | 12 | | 12 | |
| | | V _{CC} = 3 V | | 24 | | 24 | |
| Δt/Δv | Input transition rise or fall rate | | | 6 | | 6 | ns/V |
| T _A | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74LVC573A | UNIT |
|-------------------------------|--|-------------|------|
| | | PW | |
| | | 20 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 102.5 | °C/W |
| R _{θJCTop} | Junction-to-case (top) thermal resistance | 35.9 | |
| R _{θJB} | Junction-to-board thermal resistance | 53.5 | |
| Ψ _{JT} | Junction-to-top characterization parameter | 2.2 | |
| Ψ _{JB} | Junction-to-board characterization parameter | 52.9 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

SN54LVC573A, SN74LVC573A

SCAS300S –JANUARY 1993–REVISED MAY 2014

www.ti.com

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CC} | SN54LVC573A | | SN74LVC573A | | UNIT |
|--------------------------|---|-----|-----------------|-----------------------|------------------------|-----------------------|------------------------|------|
| | | | | MIN | TYP ⁽¹⁾ MAX | MIN | TYP ⁽¹⁾ MAX | |
| V _{OH} | I _{OH} = −100 μA | | 1.65 V to 3.6 V | V _{CC} − 0.2 | | V _{CC} − 0.2 | | V |
| | | | 2.7 V to 3.6 V | | | | | |
| | I _{OH} = −4 mA | | 1.65 V | 1.2 | | | | |
| | I _{OH} = −8 mA | | 2.3 V | 1.7 | | | | |
| | I _{OH} = −12 mA | | 2.7 V | 2.2 | | | | |
| | | | 3 V | 2.4 | | | | |
| I _{OH} = −24 mA | | 3 V | 2.2 | | | | | |
| V _{OL} | I _{OL} = 100 μA | | 1.65 V to 3.6 V | 0.2 | | 0.2 | | V |
| | | | 2.7 V to 3.6 V | | | | | |
| | I _{OL} = 4 mA | | 1.65 V | 0.45 | | | | |
| | I _{OL} = 8 mA | | 2.3 V | 0.7 | | | | |
| | I _{OL} = 12 mA | | 2.7 V | 0.4 | | | | |
| | I _{OL} = 24 mA | | 3 V | 0.55 | | | | |
| I _I | V _I = 0 to 5.5 V | | 3.6 V | ±5 | | ±5 | | μA |
| I _{off} | V _I or V _O = 5.5 V | | 0 | | | ±10 | | μA |
| I _{OZ} | V _O = 0 to 5.5 V | | 3.6 V | ±15 | | ±10 | | μA |
| I _{CC} | V _I = V _{CC} or GND | | 3.6 V | 10 | | 10 | | μA |
| | 3.6 V ≤ V _I ≤ 5.5 V ⁽²⁾ | | | 10 | | 10 | | |
| ΔI _{CC} | One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND | | 2.7 V to 3.6 V | 500 | | 500 | | μA |
| C _i | V _I = V _{CC} or GND | | 3.3 V | 4 | | 4 | | pF |
| C _o | V _O = V _{CC} or GND | | 3.3 V | 5.5 | | 5.5 | | pF |

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

(2) This applies in the disabled state only.

7.6 Timing Requirements, SN54LVC573A

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| | | SN54LVC573A | | | | UNIT |
|-----------------|-----------------------------|-------------------------|-----|------------------------------------|-----|------|
| | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | |
| | | MIN | MAX | MIN | MAX | |
| t _w | Pulse duration, LE high | 3.3 | | 3.3 | | ns |
| t _{su} | Setup time, data before LE↓ | 2 | | 2 | | ns |
| t _h | Hold time, data after LE↓ | 2.5 | | 2.5 | | ns |

7.7 Timing Requirements, SN74LVC573A

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

| | | SN74LVC573A | | | | | | | | UNIT |
|-----------------|-----------------------------|-------------------------------------|-----|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|------|
| | | V _{CC} = 1.8 V ± 0.15 V | | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t _w | Pulse duration, LE high | 9 | | 4 | | 3.3 | | 3.3 | | ns |
| t _{su} | Setup time, data before LE↓ | 6 | | 4 | | 2 | | 2 | | ns |
| t _h | Hold time, data after LE↓ | 4 | | 2 | | 1.5 | | 1.5 | | ns |

7.8 Switching Characteristics, SN54LVC573A

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVC573A | | | | UNIT |
|------------------|-----------------|----------------|-------------------------|-----|------------------------------------|-----|------|
| | | | V _{CC} = 2.7 V | | V _{CC} = 3.3 V ± 0.3 V | | |
| | | | MIN | MAX | MIN | MAX | |
| t _{pd} | D | Q | 7.7 | | 1 | 6.9 | ns |
| | LE | | 8.4 | | 1 | 7.7 | |
| t _{en} | \overline{OE} | Q | 8.5 | | 1 | 7.5 | ns |
| t _{dis} | \overline{OE} | Q | 7 | | 0.5 | 6.7 | ns |

7.9 Switching Characteristics, SN74LVC573A

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

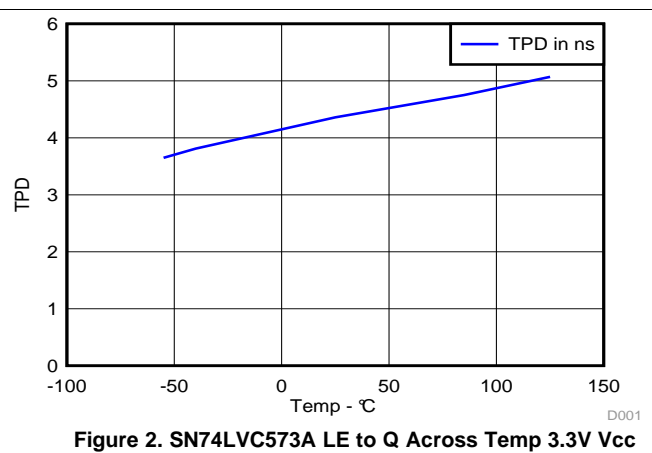
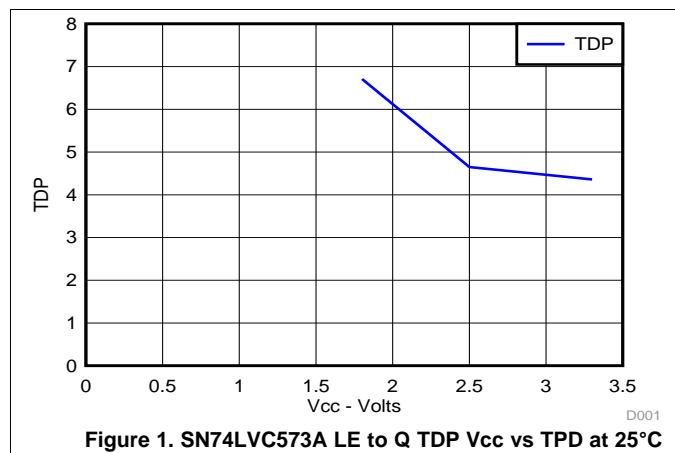
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN74LVC573A | | | | | | | | UNIT |
|-------------|-----------------|----------------|--|------|---|------|-------------------------|-----|---|-----|------|
| | | | $V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$ | | $V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{pd} | D | Q | 1 | 19.1 | 1 | 9.6 | 1 | 7.7 | 1.5 | 6.9 | ns |
| | LE | | 1 | 22.8 | 1 | 10.5 | 1 | 8.4 | 2 | 7.7 | |
| t_{en} | \overline{OE} | Q | 1 | 20 | 1 | 10.5 | 1 | 8.5 | 1.5 | 7.5 | ns |
| t_{dis} | \overline{OE} | Q | 1 | 19.3 | 1 | 7.8 | 1 | 7 | 1.6 | 6.5 | ns |
| $t_{sk(o)}$ | | | | | | | | | 1 | | ns |

7.10 Operating Characteristics

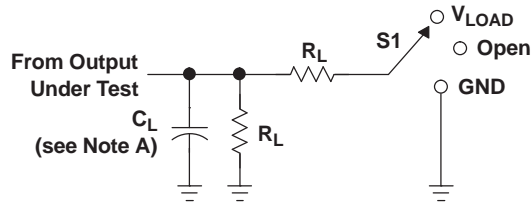
$T_A = 25^\circ\text{C}$

| PARAMETER | | | TEST CONDITIONS | V _{CC} = 1.8 V | V _{CC} = 2.5 V | V _{CC} = 3.3 V | UNIT |
|-----------------|---|---------------------|--------------------|-------------------------|-------------------------|-------------------------|------|
| | | | | TYP | TYP | TYP | |
| C _{pd} | Power dissipation capacitance per latch | Outputs enabled | f = 10 MHz | 61 | 56 | 37 | pF |
| | | Outputs disabled | | 3 | 3 | 4 | |

7.11 Typical Characteristics

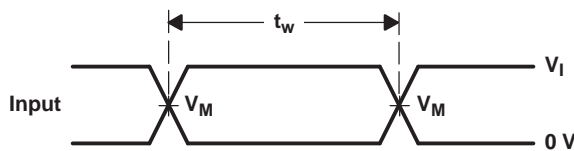
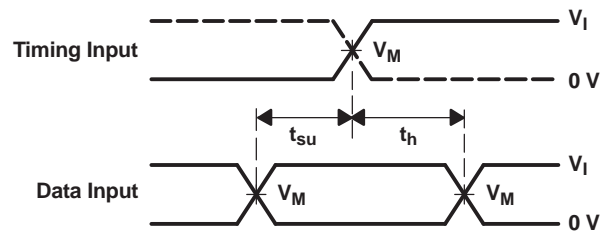
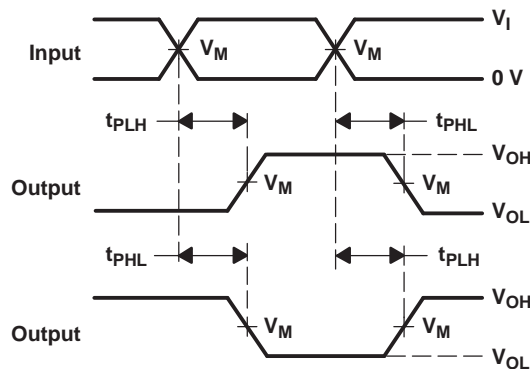
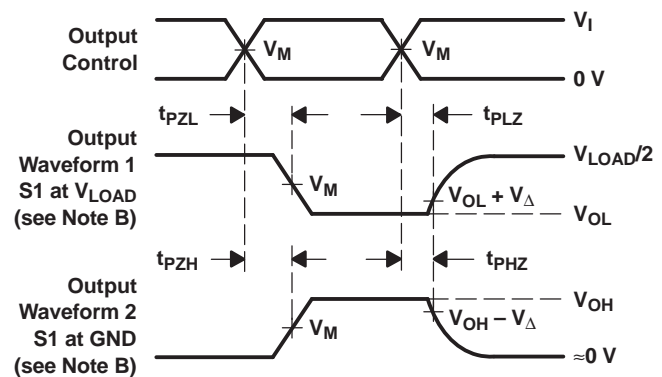


8 Parameter Measurement Information


LOAD CIRCUIT

| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| $1.8\text{ V} \pm 0.15\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | V_{CC} | $\leq 2\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 Ω | 0.15 V |
| 2.7 V | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 2.7 V | $\leq 2.5\text{ ns}$ | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |


**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

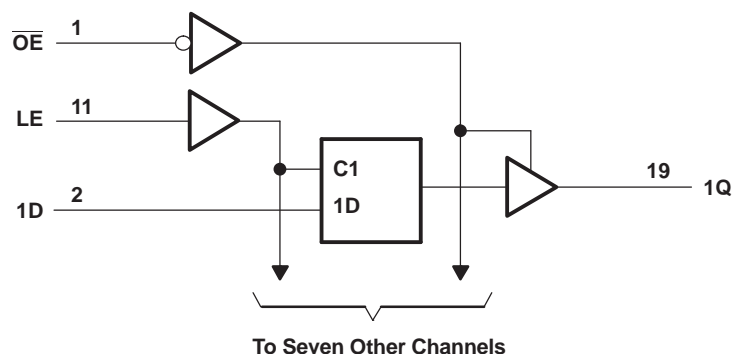
Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN54LVC573A octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation, and the SN74LVC573A octal transparent D-type latch is designed for 1.65-V to 3.6-V V_{CC} operation. These devices feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers. While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels at the D inputs. A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components. \overline{OE} does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state. These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

9.2 Functional Block Diagram



Pin numbers shown are for the DB, DGV, DW, FK, J, N, NS, PW, RGY, and W packages.

9.3 Feature Description

- Wide operating voltage range
 - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
 - Inputs accept voltages to 5.5 V
- I_{off} Feature
 - Allows voltages on the inputs and outputs when V_{CC} is 0 V

9.4 Device Functional Modes

**Function Table
(Each Latch)**

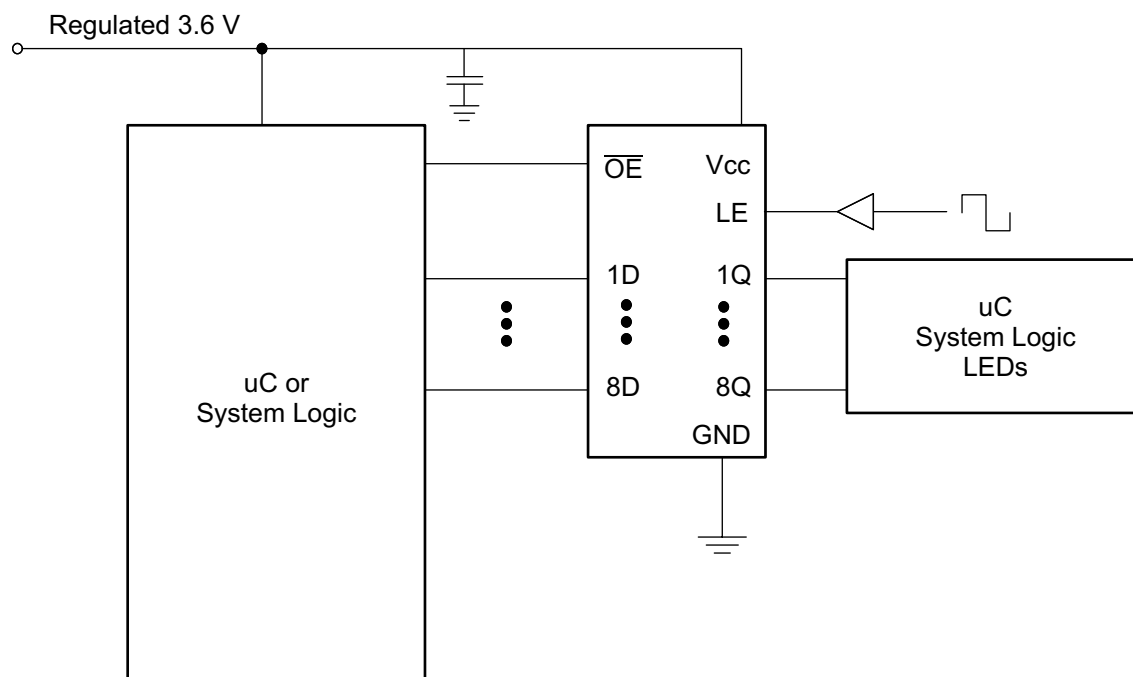
| INPUTS | | | OUTPUT Q |
|-----------------|----|---|-------------|
| \overline{OE} | LE | D | |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

10 Applications and Implementation

10.1 Application Information

The SN74LVC573A is a high drive CMOS device that can be used for a multitude of bus interface type applications where the data needs to be retained or latched . It can produce 24 mA of drive current at 3.3 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to V_{CC} .

10.2 Typical Application



10.2.1 Design Requirements

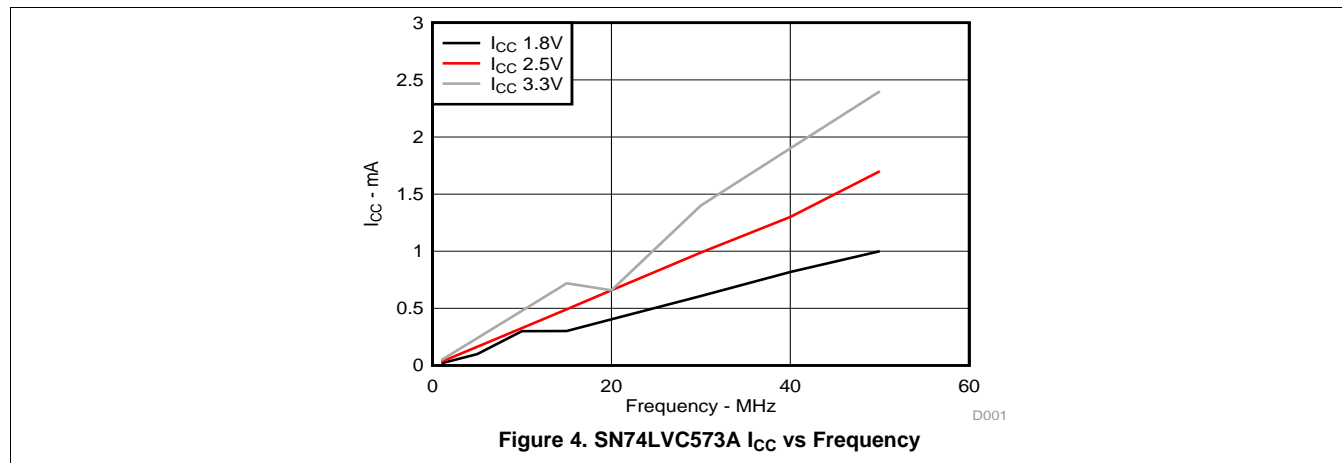
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

1. Recommended Input conditions
 - Rise time and fall time specifications. See $(\Delta t/\Delta V)$ in [Recommended Operating Conditions](#) table.
 - Specified high and low levels. See $(V_{IH}$ and $V_{IL})$ in [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid V_{CC} .
2. Recommend output conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

10.2.3 Application Curves



11 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the [Recommended Operating Conditions](#) table.

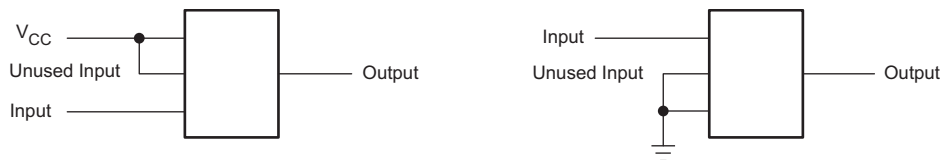
Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF capacitor is recommended. If there are multiple VCC pins, then a 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally OK to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs so they also cannot float when disabled.

12.2 Layout Example



13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54LVC573A | Click here | Click here | Click here | Click here | Click here |
| SN74LVC573A | Click here | Click here | Click here | Click here | Click here |

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|---|-------------------------|
| 5962-9757501Q2A | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962- 9757501Q2A SNJ54LVC 573AFK | Samples |
| 5962-9757501QRA | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9757501QR A SNJ54LVC573AJ | Samples |
| 5962-9757501QSA | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9757501QS A SNJ54LVC573AW | Samples |
| SN74LVC573ADBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A | Samples |
| SN74LVC573ADGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A | Samples |
| SN74LVC573ADW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC573A | Samples |
| SN74LVC573ADWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC573A | Samples |
| SN74LVC573ADWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC573A | Samples |
| SN74LVC573AN | ACTIVE | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | -40 to 125 | SN74LVC573AN | Samples |
| SN74LVC573ANSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC573A | Samples |
| SN74LVC573ANSRE4 | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC573A | Samples |
| SN74LVC573APW | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A | Samples |
| SN74LVC573APWG4 | ACTIVE | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A | Samples |
| SN74LVC573APWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 125 | LC573A | Samples |
| SN74LVC573APWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A | Samples |
| SN74LVC573APWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A | Samples |
| SN74LVC573APWT | ACTIVE | TSSOP | PW | 20 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LC573A | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|--------------------|------|----------------|---------------------|--------------------------------------|----------------------|--------------|---|-------------------------|
| SN74LVC573ARGYR | ACTIVE | VQFN | RGY | 20 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | LC573A | Samples |
| SNJ54LVC573AFK | ACTIVE | LCCC | FK | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962- 9757501Q2A SNJ54LVC 573AFK | Samples |
| SNJ54LVC573AJ | ACTIVE | CDIP | J | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9757501QR A SNJ54LVC573AJ | Samples |
| SNJ54LVC573AW | ACTIVE | CFP | W | 20 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9757501QS A SNJ54LVC573AW | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LVC573A, SN74LVC573A :

- Catalog : [SN74LVC573A](#)
- Automotive : [SN74LVC573A-Q1](#), [SN74LVC573A-Q1](#)
- Enhanced Product : [SN74LVC573A-EP](#), [SN74LVC573A-EP](#)
- Military : [SN54LVC573A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC573ADBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LVC573ADGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC573ADWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74LVC573ANSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74LVC573APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVC573APWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74LVC573APWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74LVC573APWT | TSSOP | PW | 20 | 250 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74LVC573ARGYR | VQFN | RGY | 20 | 3000 | 330.0 | 12.4 | 3.8 | 4.8 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC573ADBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC573ADGVR | TVSOP | DGV | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC573ADWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVC573ANSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74LVC573APWR | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| SN74LVC573APWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC573APWRG4 | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC573APWT | TSSOP | PW | 20 | 250 | 356.0 | 356.0 | 35.0 |
| SN74LVC573ARGYR | VQFN | RGY | 20 | 3000 | 356.0 | 356.0 | 35.0 |

TUBE



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9757501Q2A | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| 5962-9757501QSA | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |
| SN74LVC573ADW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN74LVC573AN | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74LVC573APW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SN74LVC573APWG4 | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |
| SNJ54LVC573AFK | FK | LCCC | 20 | 1 | 506.98 | 12.06 | 2030 | NA |
| SNJ54LVC573AW | W | CFP | 20 | 1 | 506.98 | 26.16 | 6220 | NA |

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|---------------------|------------------|------------------|------------------|------------------|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | AA | BB | AC | AD |



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

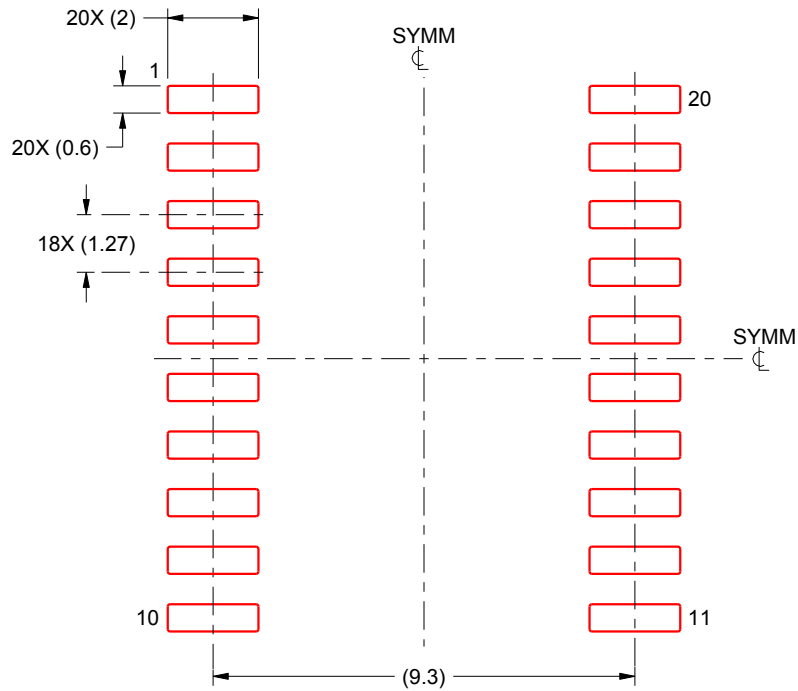
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



| NO. OF TERMINALS ** | A | | B | |
|---------------------------|------------------|------------------|------------------|------------------|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

EXAMPLE BOARD LAYOUT

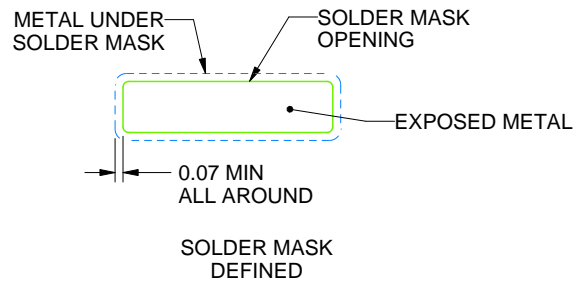
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| PINS ** DIM | 14 | 16 | 18 | 20 |
|----------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

RGY 20

VQFN - 1 mm max height

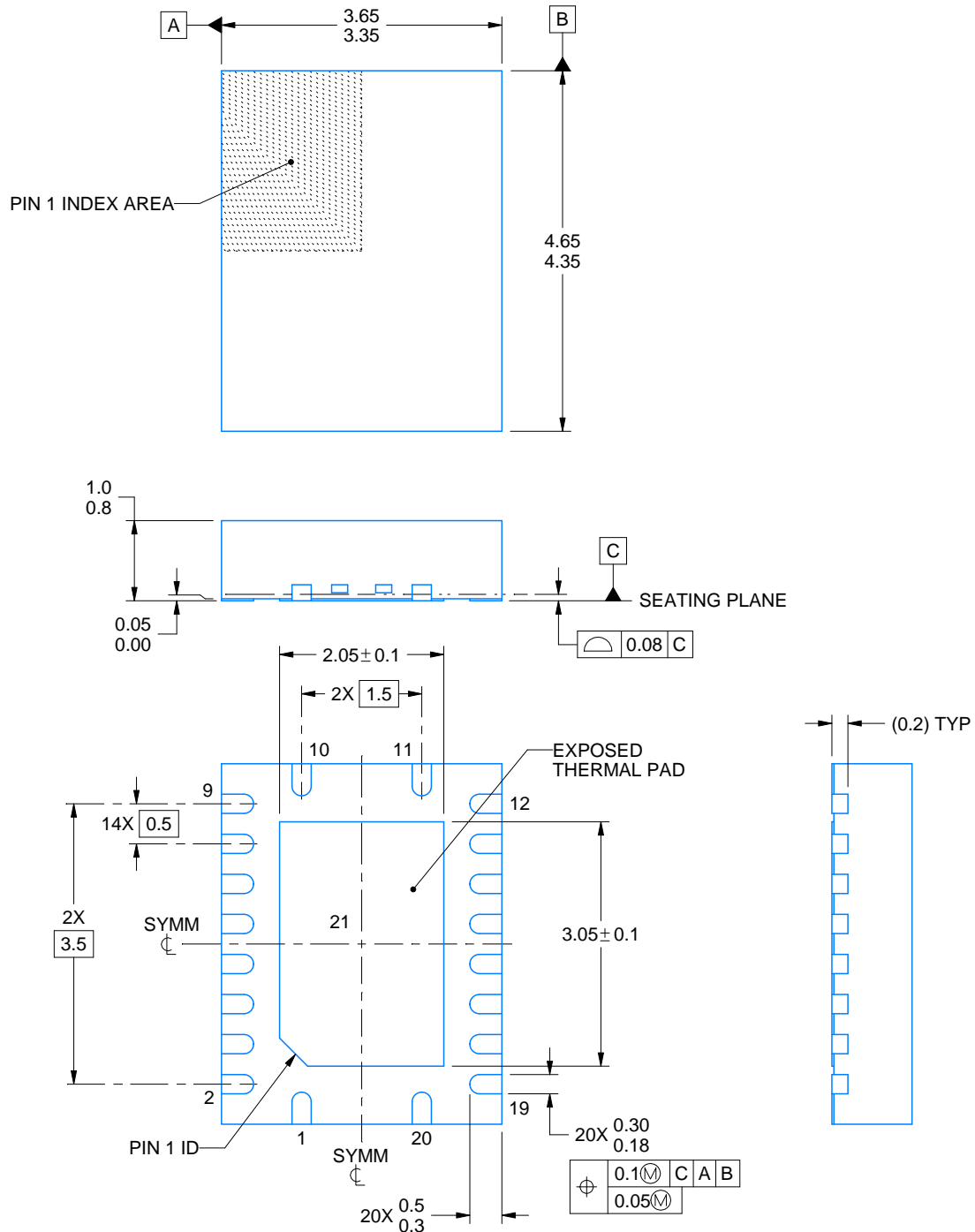
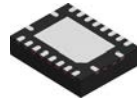
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

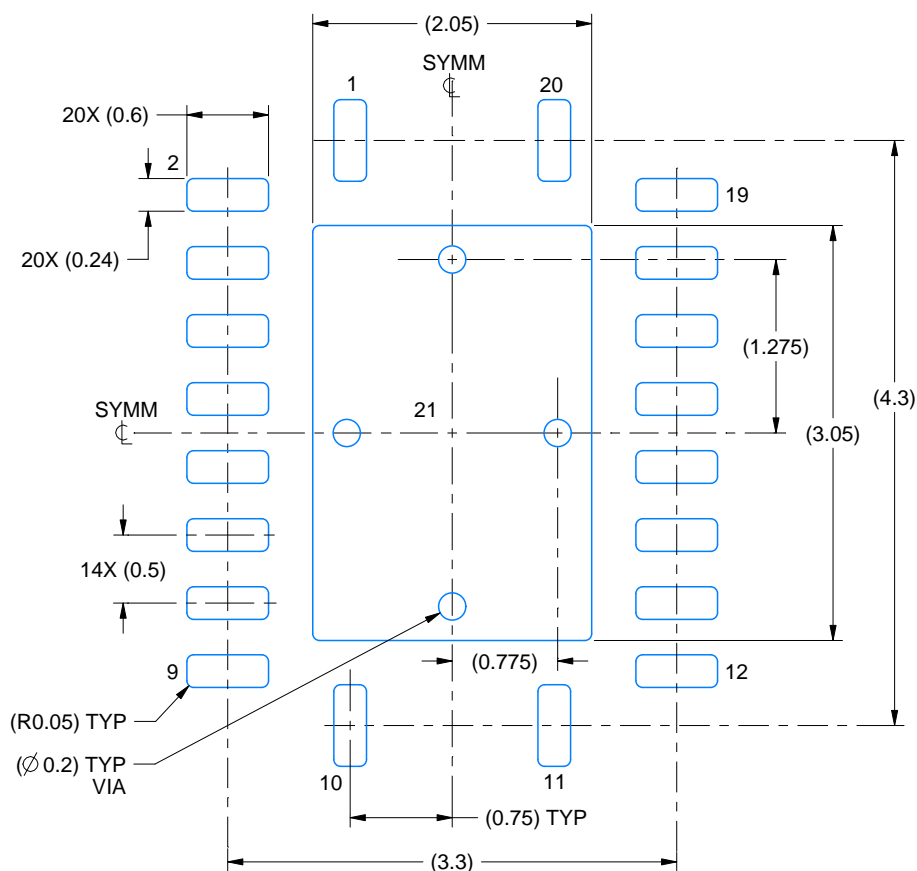
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

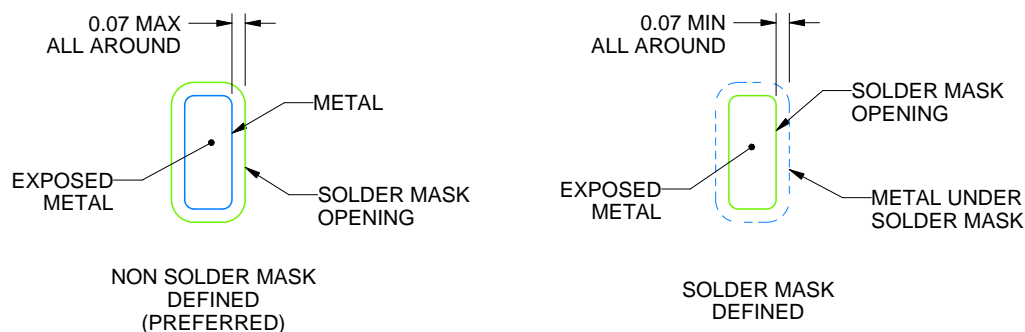
RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

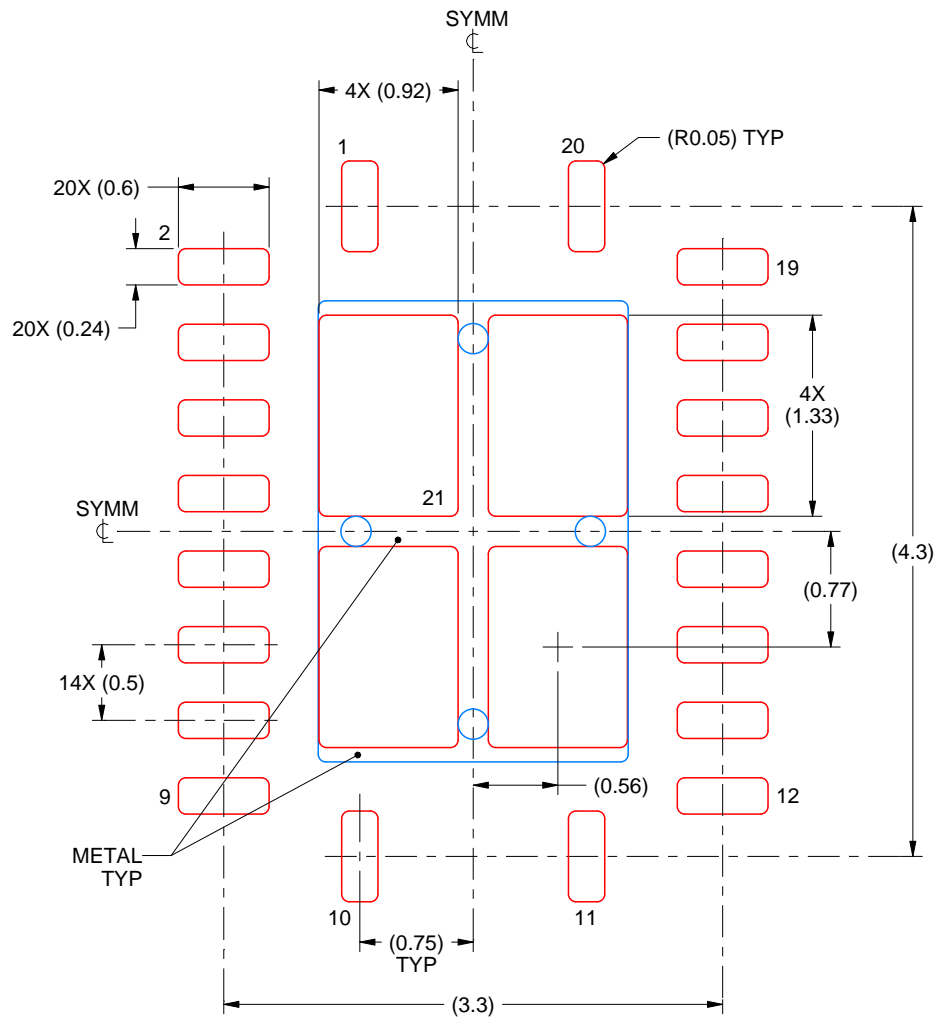
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
 78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated