DRV8313 2.5-A Triple 1/2-H Bridge Driver

1 Features

- Triple 1/2-H Bridge Driver IC
  - 3-Phase brushless DC Motors
  - Solenoid and Brushed DC Motors
- High Current-Drive Capability: 2.5-A Peak
- Low MOSFET ON-Resistance
- Independent 1/2-H-Bridge Control
- Uncommitted Comparator Can Be Used for Current Limit or Other Functions
- Built-In 3.3-V 10-mA LDO Regulator
- 8-V to 60-V Operating Supply-Voltage Range
- Sleep Mode for Standby Operation
- Small Package and Footprint
  - 28-Pin HTSSOP (PowerPAD™ Package)
  - 36-Pin VQFN

2 Applications

- Camera Gimbals
- HVAC Motors
- Office Automation Machines
- Factory Automation and Robotics

3 Description

The DRV8313 provides three individually controllable half-H-bridge drivers. The device is intended to drive a three-phase brushless-DC motor, although it can also be used to drive solenoids or other loads. Each output driver channel consists of N-channel power MOSFETs configured in a 1/2-H-bridge configuration. Each 1/2-H-bridge driver has a dedicated ground terminal, which allows independent external current sensing.

An uncommitted comparator is integrated into the DRV8313, which allows for the construction of current-limit circuitry or other functions.

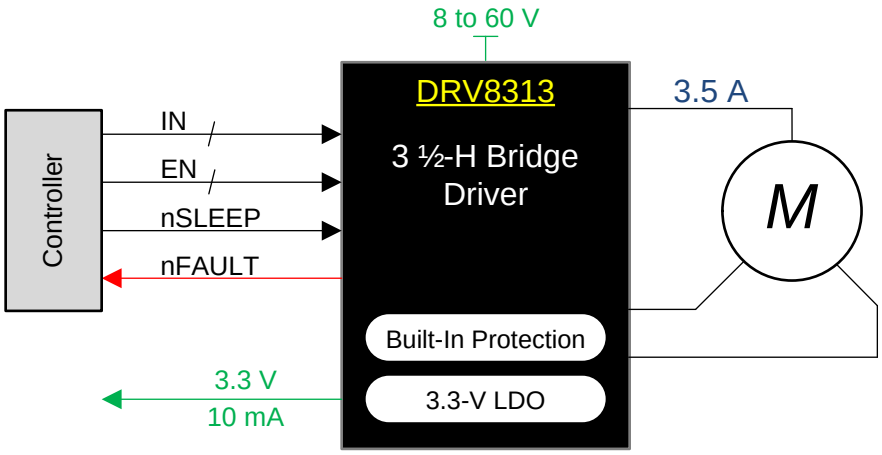
Internal protection functions are provided for undervoltage, charge pump faults, overcurrent, short circuits, and overtemperature. Fault conditions are indicated by the nFAULT pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8313	HTSSOP (28)	9.70 mm × 4.40 mm
	VQFN (36)	6.00 mm × 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (November 2015) to Revision D — **Page**

- Changed pin 18 of the VQFN (RHH) package from GND to RSVD ... 4

Changes from Revision B (January 2015) to Revision C — **Page**

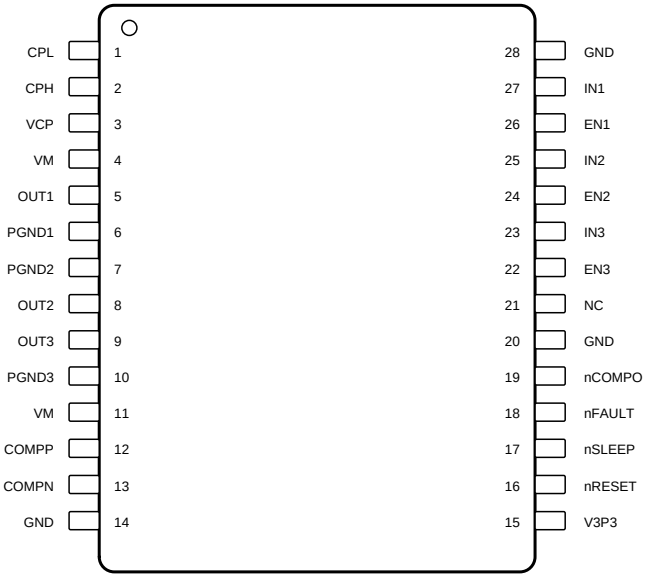
- Added a new package to the Device Information table ... 1
- Added a new VQFN package for the device ... 3
- Corrected a numbering error on one of the ground pins in the Pin Functions table ... 3

Changes from Revision A (November 2012) to Revision B — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 4

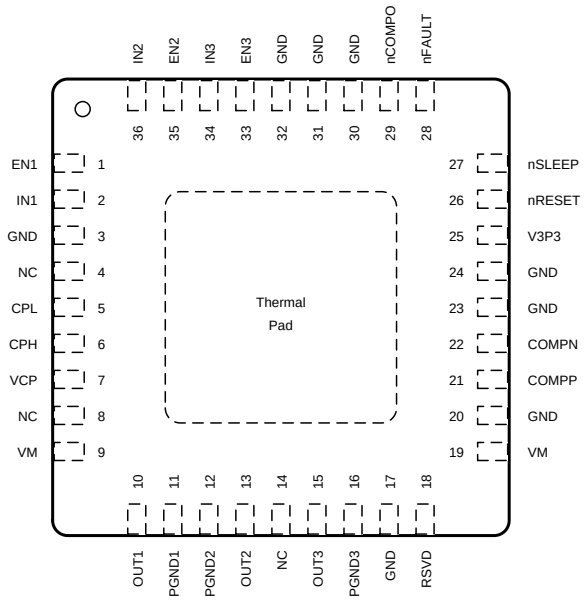
5 Pin Configuration and Functions

PWP Package
28-Pin HTSSOP With PowerPAD Package
Top View



NC - No internal connection

RHH Package
36-Pin VQFN With Exposed Thermal Pad
Top View



Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	PWP	RHH		
COMPN	13	22	I	Comparator negative input. Uncommitted comparator input
COMPP	12	21	I	Comparator positive input. Uncommitted comparator input
CPL	1	5	PWR	Charge pump. Connect a VM-rated, 0.01-µF ceramic capacitor between CPH and CPL.
CPH	2	6	PWR	Charge pump. Connect a VM-rated, 0.01-µF ceramic capacitor between CPH and CPL.
EN1	26	1	I	Channel enable. Logic high enables the 1/2-H bridge channel; internal pulldown
EN2	24	35	I	Channel enable. Logic high enables the 1/2-H bridge channel; internal pulldown
EN3	22	33	I	Channel enable. Logic high enables the 1/2-H bridge channel; internal pulldown
GND	14, 20, 28	3, 17, 20, 23, 24, 30, 31, 32,	PWR	Device ground. Connect to system ground
IN1	27	2	I	Channel input. Logic high pulls 1/2-H bridge high, logic low pulls 1/2-H bridge low; no effect when ENx is low; internal pulldown input.
IN2	25	36	I	Channel input. Logic high pulls 1/2-H bridge high, logic low pulls 1/2-H bridge low; no effect when ENx is low; internal pulldown input.
IN3	23	34	I	Channel input. Logic high pulls 1/2-H bridge high, logic low pulls 1/2-H bridge low; no effect when ENx is low; internal pulldown input.
NC	21	4, 8, 14	NC	No internal connection. Recommended net given in block diagram (if any)
nCOMPO	19	29	OD	Comparator output. Uncommitted comparator output; open drain requires an external pullup.
nFAULT	18	28	OD	Fault indication pin. Pulled logic-low with fault condition; open-drain output requires an external pullup.
nRESET	16	26	I	Reset input. Active-low reset input initializes internal logic, clears faults, and disables the outputs, internal pulldown

(1) I = input, O = output, OD = open-drain output, PWR = power, NC = no connect

Pin Functions (continued)

PIN			TYPE(1)	DESCRIPTION
NAME	NO.			
	PWP	RHH		
nSLEEP	17	27	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown
OUT1	5	10	O	Half-H bridge output, connect to the load
OUT2	8	13	O	Half-H bridge output, connect to the load
OUT3	9	15	O	Half-H bridge output, connect to the load
PGND1	6	11	PWR	Low-side FET source. Connect to GND or to low-side current-sense resistors
PGND2	7	12	PWR	Low-side FET source. Connect to GND or to low-side current-sense resistors
PGND3	10	16	PWR	Low-side FET source. Connect to GND or to low-side current-sense resistors
RSVD	—	18	—	Reserved. Leave this pin disconnected.
V3P3	15	25	PWR	Internal regulator. Internal supply voltage; bypass to GND with a 6.3-V, 0.47-µF ceramic capacitor; up to 10-mA external load
VCP	3	7	PWR	Charge pump. Connect a 16-V, 0.1-µF ceramic capacitor to VM
VM	4, 11	9, 19	PWR	Power supply. Connect to motor supply voltage; bypass to GND with two 0.1-µF capacitors (for each pin) plus one bulk capacitor rated for VM
Thermal pad			PWR	Must be connected to ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Power-supply voltage (VM)	–0.3	65	V
Power supply voltage ramp rate (VM)	0	2	V/µs
Charge pump voltage (VCP, CPH)	–0.3	VM + 12	V
Charge pump negative switching pin (CPL)	–0.3	VM	V
Internal regulator current output (V3P3)	0	10	mA
Internal regulator voltage (V3P3)	–0.3	3.8	V
Control pin voltage (nRESET, nSLEEP, nFAULT, nCOMPO, ENx, INx)	–0.5	7	V
Comparator input-voltage (COMPP, COMPN)	–0.5	7	V
Open drain output current (nFAULT, nCOMPO)	0	10	mA
Continuous phase node pin voltage (OUTx)	–0.7	VM + 0.7	V
Continuous 1/2-H-bridge source voltage (PGNDx)	–600	600	mV
Peak output current (OUTx)	Internally limited		A
Operating junction temperature T_J	–40	150	°C
Storage temperature T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VM	Motor power-supply voltage(1)	8	60	V
V_{IN}	Digital pin voltage	0	5.5	V
f_{PWM}	Applied PWM signal on ENx, INx	0	250	kHz
V_{GNDX}	PGNDx pin voltage	–500	500	mV
I_{V3P3}	V3P3 load current	0	10(2)	mA
T_A	Operating ambient temperature	–40	125	°C

(1) Both VM pins must be connected to the same supply voltage.
(2) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC (1)		DRV8313		UNIT
		PWP (HTSSOP)	RHH (VQFN)	
		28 PINS	36 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.6	31.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.9	17.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.6	5.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.5	5.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.4	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V, f_{PWM} < 50 kHz		1	5	mA
I_{VMQ}	VM sleep-mode supply current	V_M = 24 V		500	800	µA
INTERNAL REGULATOR (V3P3)						
V_{3P3}	V3P3 voltage	I_{OUT} = 0 to 10 mA	3.1	3.3	3.52	V
LOGIC-LEVEL INPUTS (nSLEEP, ENx, INx)						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2.2		5.25	V
V_{HYS}	Input hysteresis		50		600	mV
I_{IL}	Input low current	VIN = 0	–5		5	µA
I_{IH}	Input high current	VIN = 3.3 V			100	µA
R_{PD}	Pulldown resistance			100		kΩ
OPEN-DRAIN OUTPUTS (nFAULT and nCOMPO)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
COMPARATOR (COMPP, COMPN, nCOMPO)						
V_{CM}	Common-mode input-voltage range		0		5	V
V_{IO}	Input offset voltage		–7		7	mV
I_{IB}	Input bias current		–300		300	nA
t_R	Response time	100-mV step with 10-mV overdrive			2	µs
H-BRIDGE FETs						
$r_{DS(on)}$	High-side FET ON-resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.24		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C(1)		0.29	0.39	
	Low-side FET ON-resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.24		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C(1)		0.29	0.39	
I_{OFF}	Off-state leakage current		–2		2	µA
PROTECTION CIRCUITS						
V_{UVLO}	VM undervoltage lockout voltage	V_M rising		6.3	8	V
I_{OCP}	Overcurrent protection trip level		3	5		A
t_{OCP}	Overcurrent protection deglitch time			5		µs
T_{TSD}(1)	Thermal shutdown temperature	Die temperature	150	160	180	°C
T_{HYS}(1)	Thermal shutdown hysteresis	Die temperature		35		°C

(1) Specification based on design and characterization data

6.6 Switching Characteristics

T_A = 25°C, V_M = 24 V, R_L = 20 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Delay time, ENx high to OUTx high	INx = 1	130		330	ns
t_2	Delay time, ENx low to OUTx low	INx = 1	275		475	ns
t_3	Delay time, ENx high to OUTx low	INx = 0	100		300	ns
t_4	Delay time, ENx low to OUTx high	INx = 0	200		400	ns
t_5	Delay time, INx high to OUTx high	ENx = 1	300		500	ns
t_6	Delay time, INx low to OUTx low	ENx = 1	275		475	ns
t_r	Output rise time, resistive load to GND		30		150	ns
t_f	Output fall time, resistive load to GND		30		150	ns
t_{DEAD} (1)	Output dead time			90		ns

(1) Specified by design and characterization data

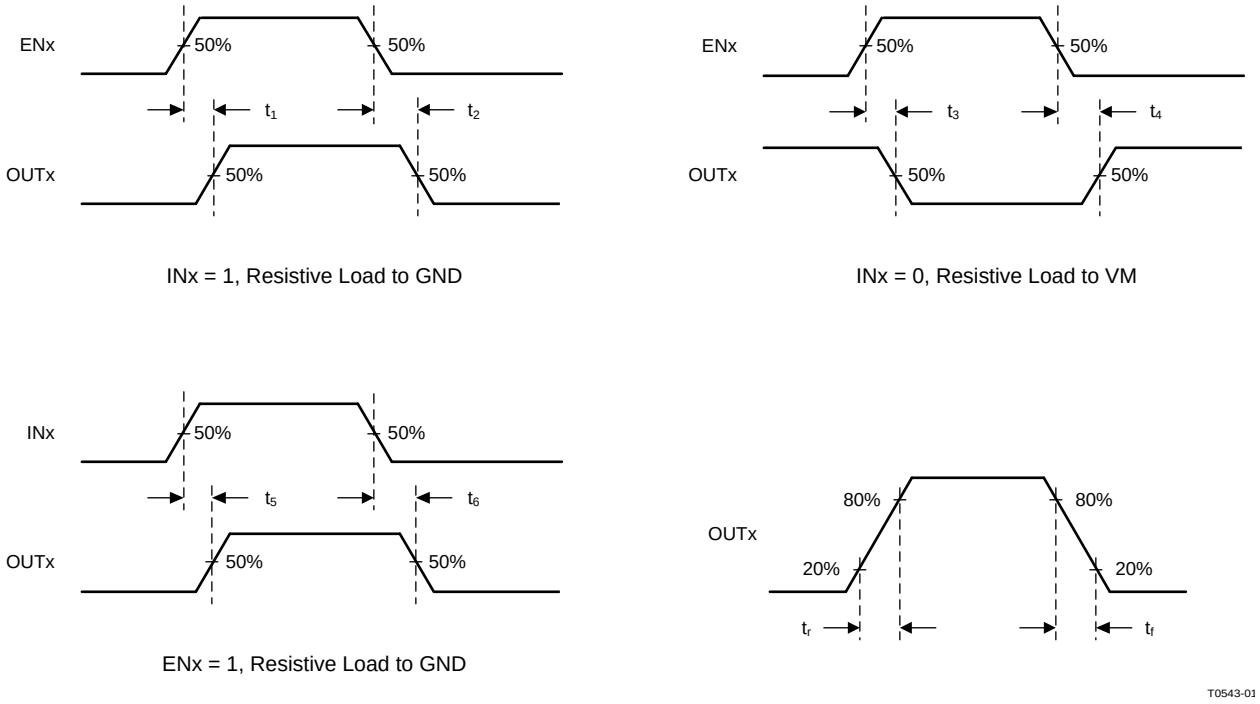


Figure 1. DRV8313 Switching Characteristics

6.7 Typical Characteristics

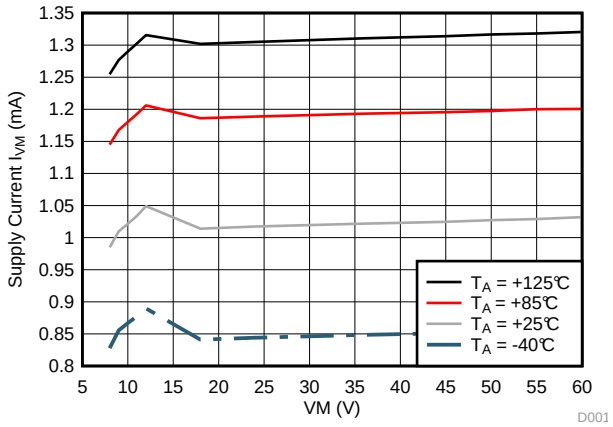


Figure 2. Supply Current vs Supply Voltage

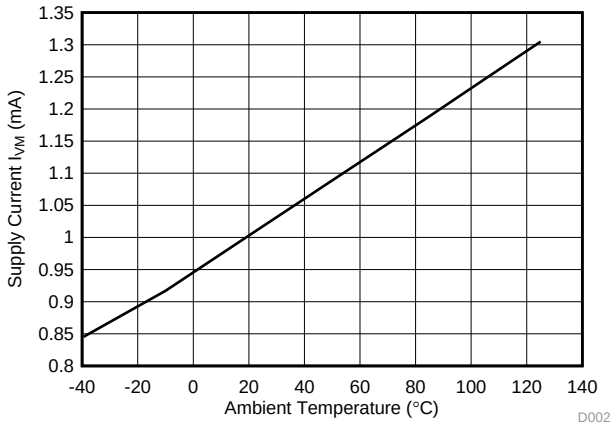


Figure 3. Supply Current vs Temperature at VM = 24 V

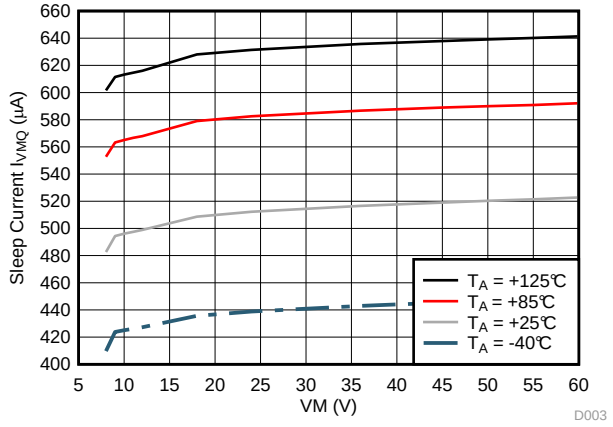


Figure 4. Sleep Current vs Supply Voltage

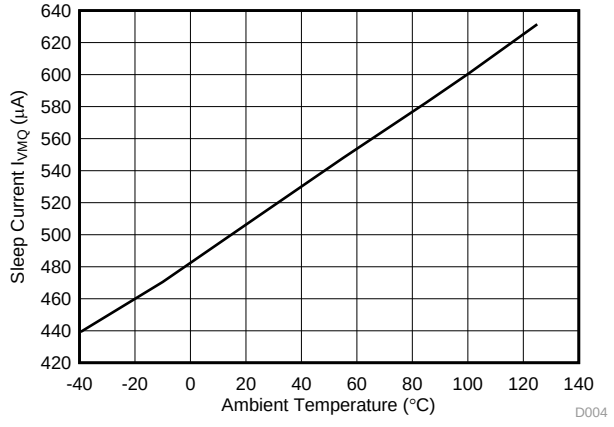


Figure 5. Sleep Current vs Temperature at VM = 24 V

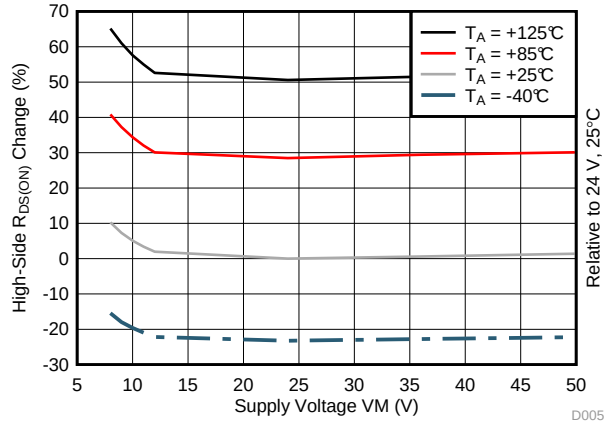


Figure 6. High-Side $R_{DS(on)}$ vs Supply Voltage (Normalized to 24 V, 25°C)

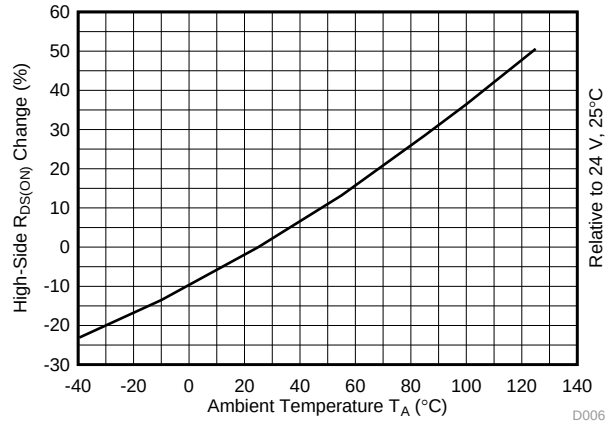


Figure 7. High-Side $R_{DS(on)}$ vs Temperature at VM = 24 V (Normalized to 25°C)

Typical Characteristics (continued)

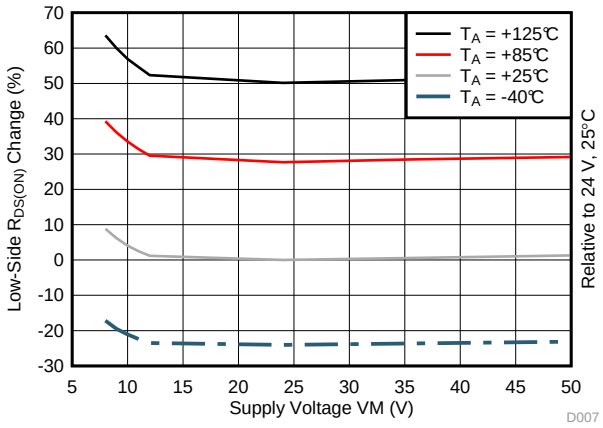


Figure 8. Low-Side $R_{DS(on)}$ vs Supply Voltage (Normalized to 24 V, 25°C)

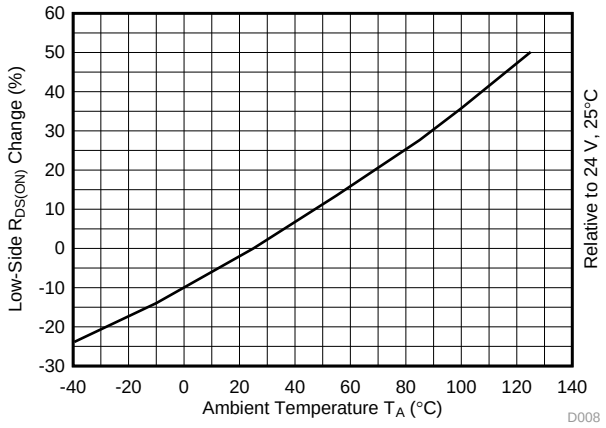


Figure 9. Low-Side $R_{DS(on)}$ vs Temperature at VM = 24 V (Normalized to 25°C)

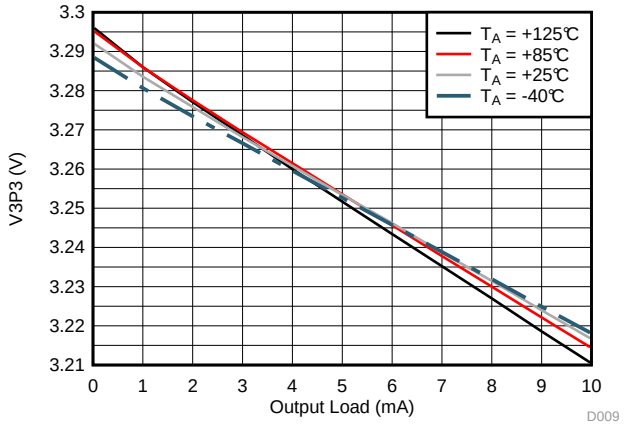


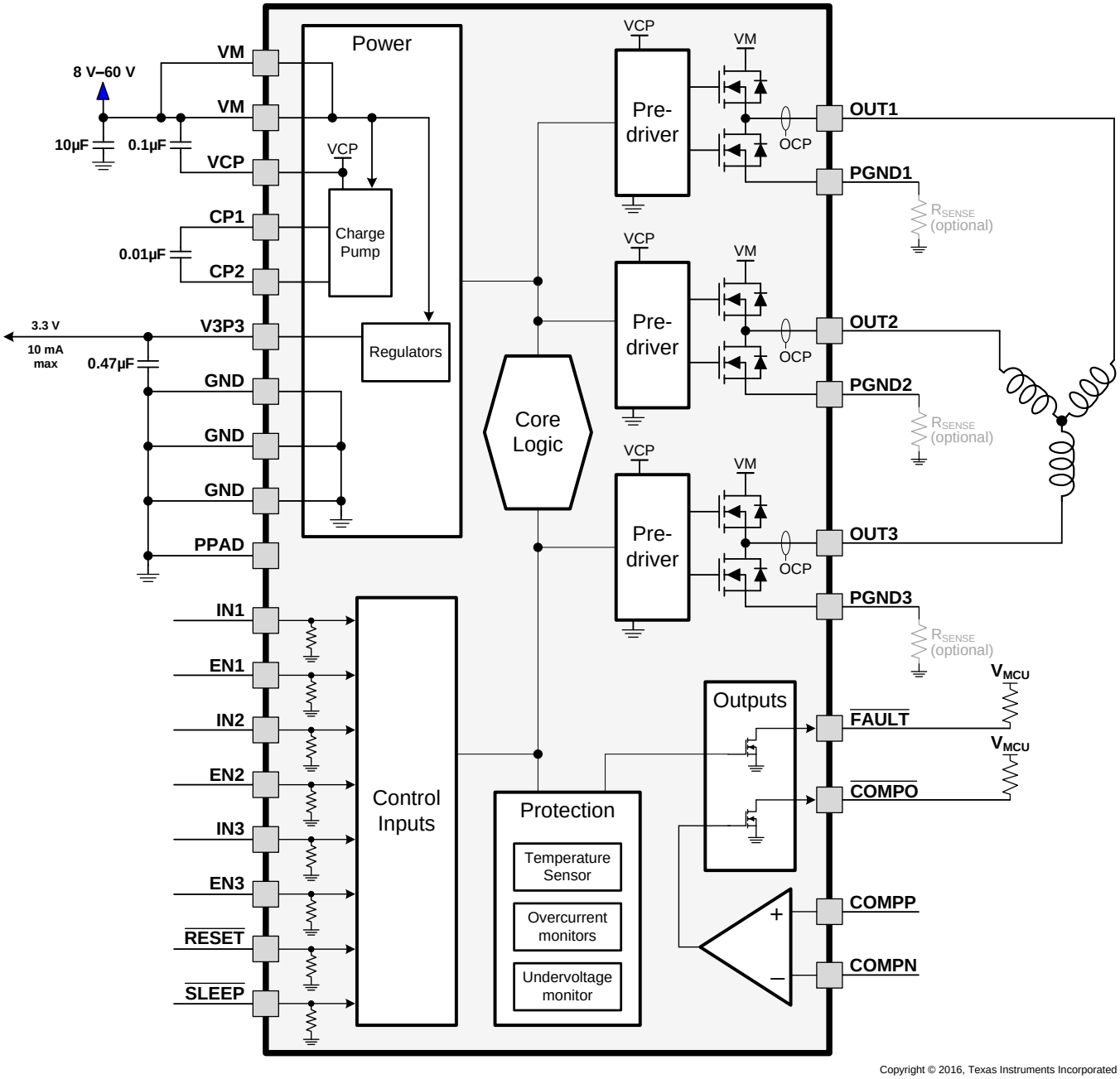
Figure 10. V3P3 Regulator vs Load at VM = 24 V

7 Detailed Description

7.1 Overview

The DRV8313 integrates three independent 2.5-A half-H bridges, protection circuits, sleep mode, fault reporting, and a comparator. The single power supply supports a wide 8-V to 60-V range, making it well-suited for motor drive applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Stage

The DRV8313 contains three half-H-bridge drivers. The source terminals of the low-side FETs of all three half-H-bridges terminate at separate pins (PGND1, PGND2, and PGND3) to allow the use of a low-side current-sense resistor on each output, if desired. The user can also connect all three together to a single low-side sense resistor, or can connect them directly to ground if current sensing is unneeded.

If using a low-side sense resistor, ensure that the voltage on the PGND1, PGND2, or PGND3 pin does not exceed ±500 mV.

The device has two VM motor power-supply pins. Connect both VM pins together to the motor-supply voltage.

7.3.2 Bridge Control

The INx input pins directly control the state (high or low) of the OUTx outputs; the ENx input pins enable or disable the OUTx driver. Table 1 shows the logic:

Table 1. Logic States

INx	ENx	OUTx
X	0	Z
0	1	L
1	1	H

7.3.3 Charge Pump

Because the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to enhance the high-side FETs fully. The DRV8313 integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors for operation. See the block diagram and pin descriptions for details on these capacitors (value, connection, and so forth).

The charge pump shuts down when nSLEEP is low.

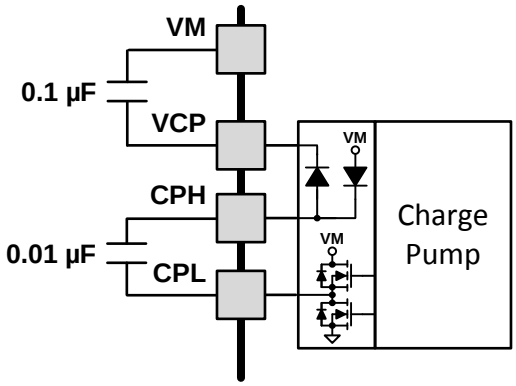


Figure 11. DRV8313 Charge Pump

7.3.4 Comparator

The DRV8313 includes an uncommitted comparator, which can find use as a current-limit comparator or for other purposes.

Figure 12 shows connections to use the comparator to sense current for implementing a current limit. Current from all three low-side FETs is sensed using a single low-side sense resistor. The voltage across the sense resistor is compared with a reference, and when the sensed voltage exceeds the reference, a current-limit condition is signaled to the controller. The V3P3 internal voltage regulator can be used to set the reference voltage of the comparator.

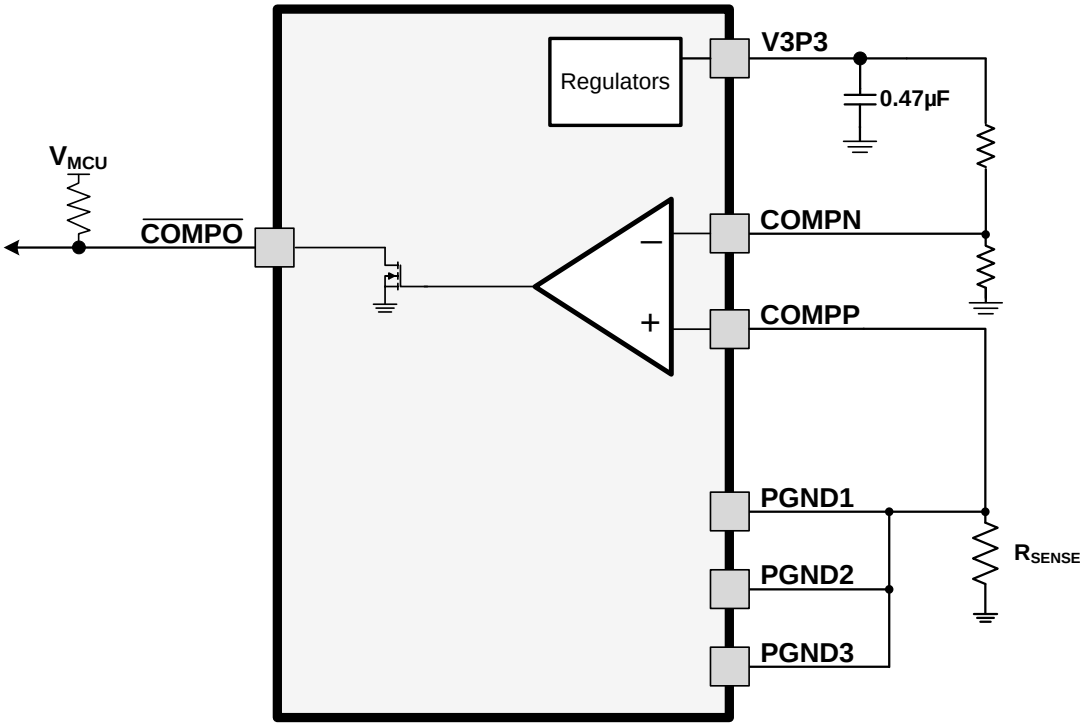


Figure 12. Comparator As Current Monitor

7.3.5 Protection Circuits

The DRV8313 has full protection against undervoltage, overcurrent, and overtemperature events.

7.3.5.1 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage threshold voltage (V_{UVLO}), all FETs in the H-bridge will be disabled, the charge pump will be disabled, the internal logic is reset, and the nFAULT pin will be driven low. Operation will resume when VM rises above the UVLO threshold. The nFAULT pin will be released after operation has resumed.

7.3.5.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume. The nFAULT pin will be released after operation has resumed.

7.3.5.3 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{OCP}, the device disables the channel experiencing the overcurrent and drives the nFAULT pin low. The driver remains off until either assertion of nRESET or the cycling of VM power.

Overcurrent conditions on both high- and low-side devices, that is, a short to ground, supply, or across the motor winding, all result in an overcurrent shutdown.

Table 2. Fault Condition Summary

FAULT	CONDITION	ERROR REPORT	H-BRIDGE	CHARGE PUMP	V3P3	RECOVERY
VM undervoltage (UVLO)	$VM < V_{UVLO}$ (max 8 V)	nFAULT	Disabled	Disabled	Operating	$VM > V_{UVLO}$ (max 8 V)
Thermal Shutdown (TSD)	$T_J > T_{TSD}$ (min 150°C)	nFAULT	Disabled	Operating	Operating	$T_J < T_{TSD} - T_{HYS}$ (T_{HYS} typ 35°C)
Overcurrent (OCP)	$I_{OUT} > I_{OCP}$ (min 3 A)	nFAULT	Disabled	Operating	Operating	nRESET

7.4 Device Functional Modes

The DRV8313 is active unless the nSLEEP pin is brought logic low. In sleep mode the charge pump is disabled, the output FETs are disabled Hi-Z, and the V3P3 regulator is disabled. The DRV313 is brought out of sleep mode automatically if nSLEEP is brought logic high.

7.4.1 nRESET and nSLEEP Operation

The nRESET pin, when driven low, resets any faults. It also disables the output drivers while it is active. The device ignores all inputs while nRESET is active. Note that there is an internal power-up-reset circuit, so that driving nRESET at power up is not required.

Driving nSLEEP low puts the device into a low-power sleep state. Entering this state disables the output drivers, stops the gate-drive charge pump, resets all internal logic (including faults), and stops all internal clocks. In this state, the device ignores all inputs until nSLEEP returns inactive-high. When returning from sleep mode, some time (approximately 1 ms) must pass before the motor driver becomes fully operational. The V3P3 regulator remains operational in sleep mode.

Table 3. Functional Modes Summary

FAULT	CONDITION	H-BRIDGE	CHARGE PUMP	V3P3
Operating	8 V < VM < 60 V nSLEEP pin = 1	Operating	Operating	Operating
Sleep mode	8 V < VM < 60 V nSLEEP pin = 0	Disabled	Disabled	Disabled
Fault encountered	VM undervoltage (UVLO)	Disabled	Disabled	Operating
	Overcurrent (OCP)	Disabled	Operating	Operating
	Thermal shutdown (TSD)	Disabled	Operating	Operating

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8313 can be used to drive Brushless-DC motors, Brushed-DC motors, and solenoid loads. The following design procedure can be used to configure the DRV8313.

8.2 Typical Applications

8.2.1 Three-Phase Brushless-DC Motor Control

In this application, the DRV8313 is used to drive a Brushless-DC motor

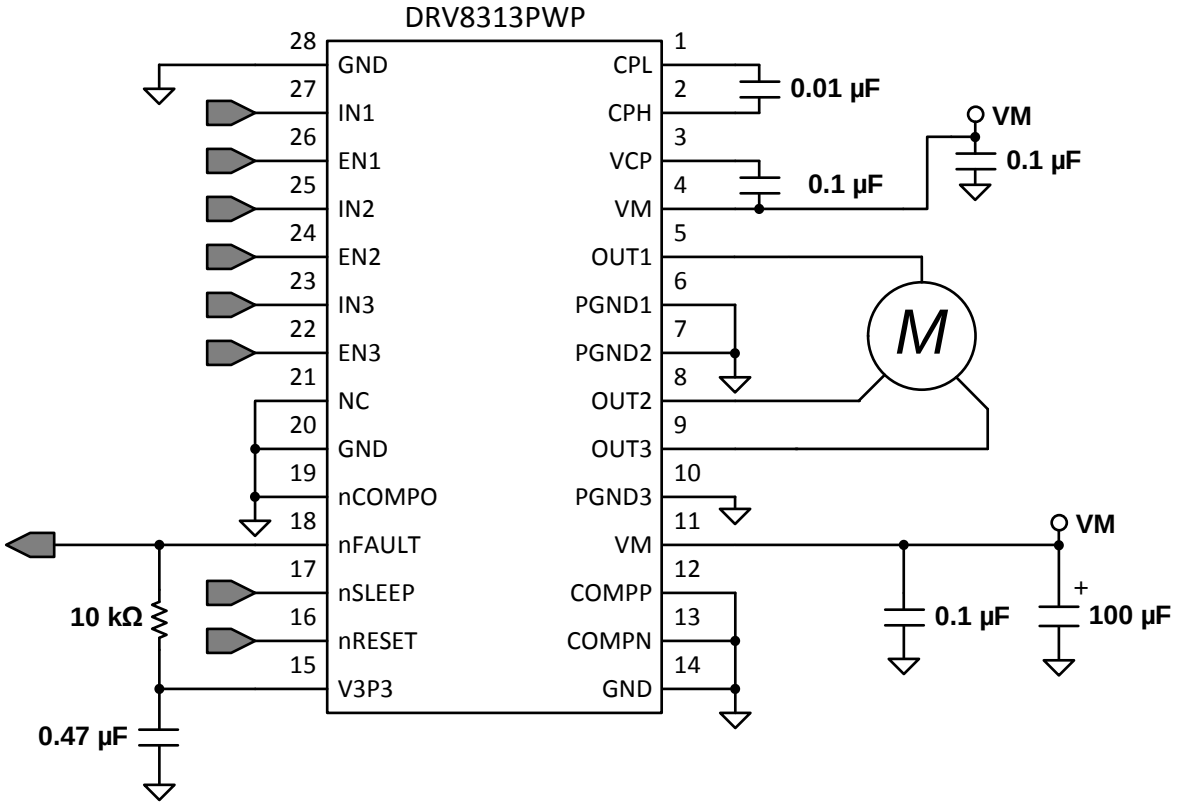


Figure 13. BLDC Driver Application Schematic

Typical Applications (continued)

8.2.1.1 Design Requirements

Table 4 gives design input parameters for system design.

Table 4. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Typical supply voltage	VM	18 V
Maximum voltage	VM_{MAX}	36 V
Target rms current	I_{RMS}	1.2 A
Motor winding resistance	M_R	0.5 Ω
Motor winding inductance	M_L	0.28 mH
Motor poles	M_P	16 poles
Motor rated RPM	M_{RPM}	4000 RPM
PWM frequency	f_{PWM}	25 kHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Motor Voltage

Brushless-DC motors are typically rated for a certain voltage (for example 12 V and 24 V). Operating a motor at a higher voltage corresponds to a lower drive current to obtain the same motor power. A higher operating voltage also corresponds to a higher obtainable rpm. DRV8313 allows for the use of higher operaing voltage because of a maximum VM rating of 60 V.

Operating at lower voltages generally allows for more accurate control of phase currents. The DRV8313 functions down to a supply of 8 V.

8.2.1.2.2 Motor Commutation

The DRV8313 can drive both trapezoidal (120°) and sinusiodal (180°) commutation due to independent control of each of the three 1/2-H bridges.

Both synchronous and asynchronous rectification are supported. Synchronous rectification is achieved by applying a pulse-width-modulated (PWM) input signal to the INx pins while driving. The user can also implement asynchronous rectification by applying the PWM signal to the ENx inputs.

Table 5. Trapezoidal (120°) Commutation States

State	OUT1 (Phase U)			OUT2 (Phase V)			OUT3 (Phase W)		
	IN1	EN1	OUT1	IN2	EN2	OUT2	IN3	EN3	OUT3
1	X	0	Z	1	1	H	0	1	L
2	1	1	H	X	0	Z	0	1	L
3	1	1	H	0	1	L	X	0	Z
4	X	0	Z	0	1	L	1	1	H
5	0	1	L	X	0	Z	1	1	H
6	0	1	L	1	1	H	X	0	Z
Brake	0	1	L	0	1	L	0	1	L
Coast	X	0	Z	X	0	Z	X	0	Z

8.2.1.3 Application Curve

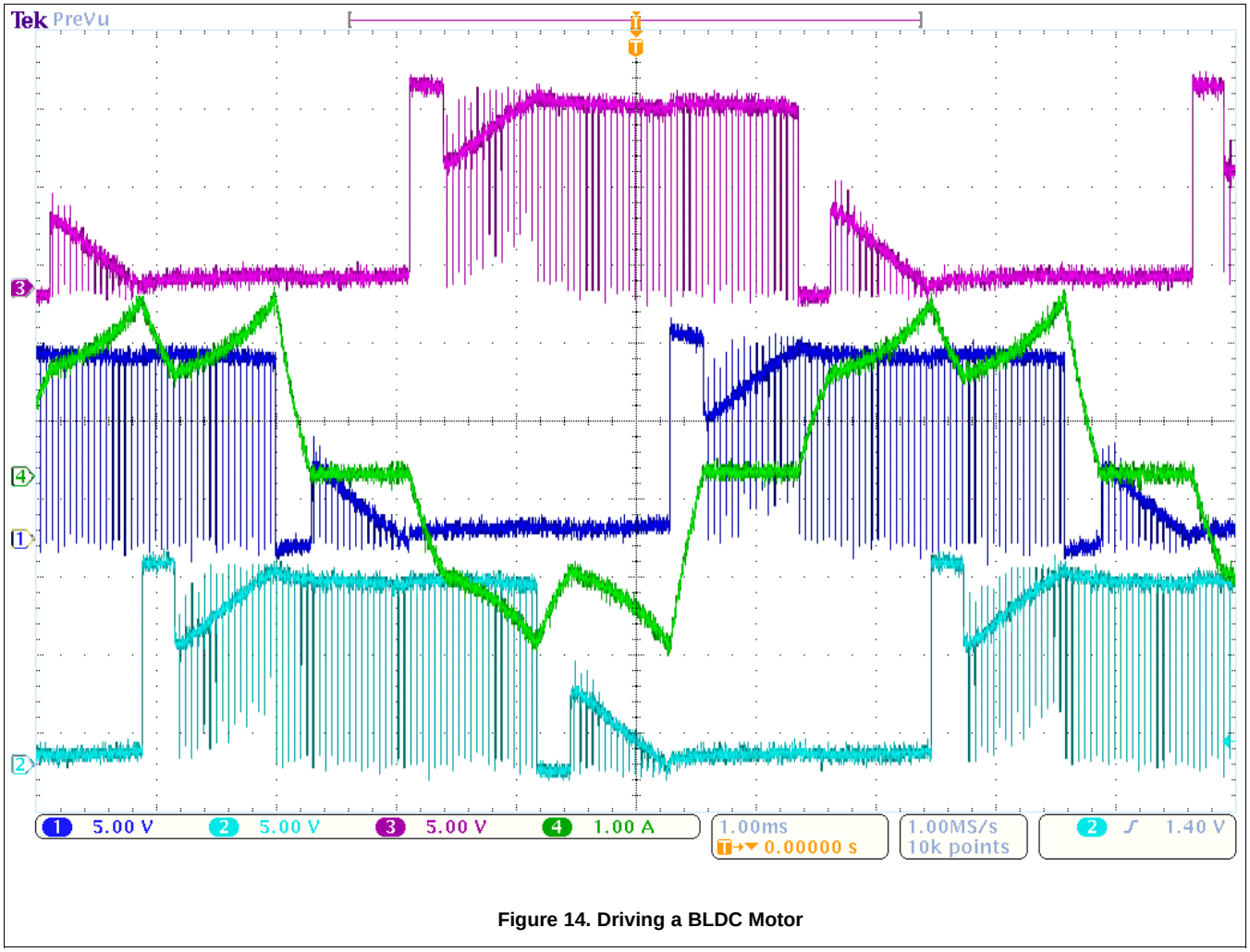


Figure 14. Driving a BLDC Motor

8.2.2 Three-Phase Brushless-DC Motor Control With Current Monitor

In this application, the DRV8313 is used to drive a brushless-DC motor and the uncommitted comparator is used to monitor the motor current

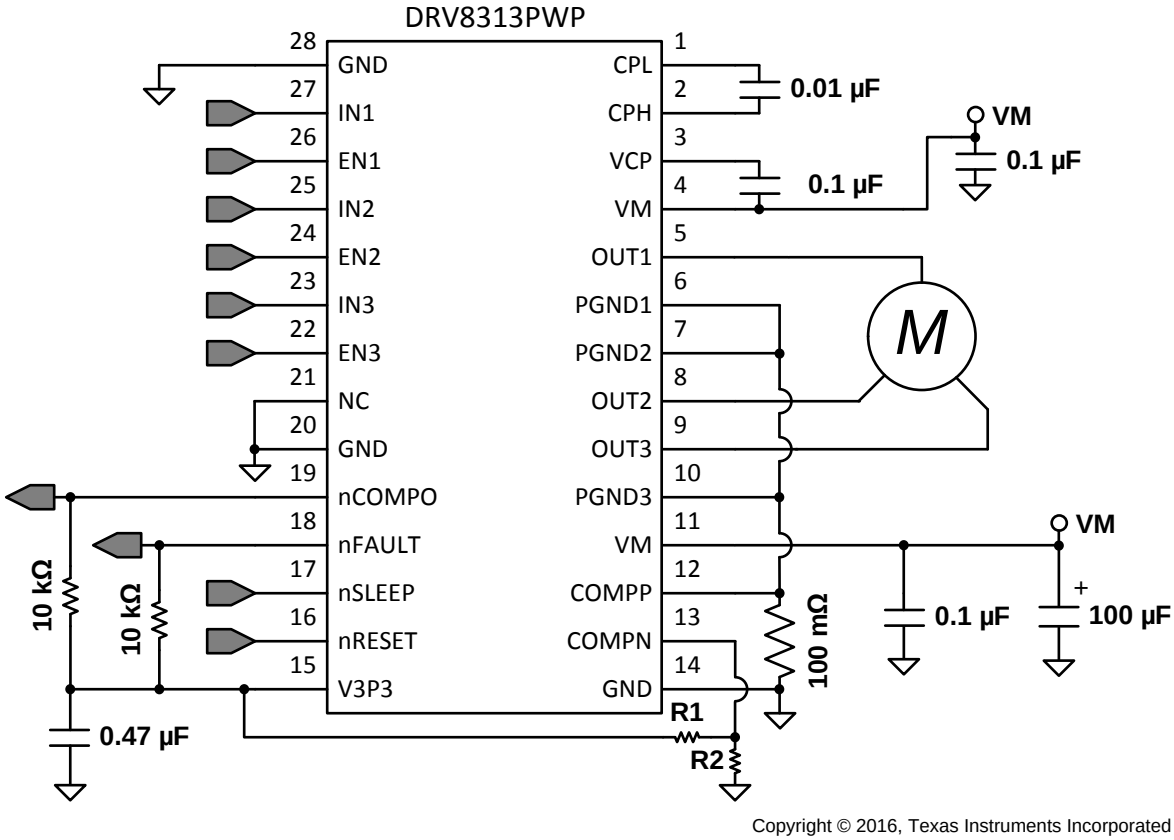


Figure 15. Uncommitted Comparator Used As a Current Monitor

8.2.2.1 Design Requirements

Table 6 gives design input parameters for system design.

Table 6. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Trip current	I_{TRIP}	2.5 A

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Trip Current

The uncommitted comparator is configured such that the negative input COMPN is connected to the PGNDx pins. A sense resistor is placed from the PGNDx/COMPN pins to GND.

The voltage on the COMPP pin will set the current monitor trip threshold. In this case, the the nCOMPO pin will change state when COMPP and COMPN have the same potential.

$$I_{TRIP}\ (A) = \frac{COMPN\ (V)}{R_{SENSE}\ (\Omega)} \quad (1)$$

Example: If the desired trip current is 2.5 A

Set R_{SENSE} = 200 mΩ

COMPN would have to be 0.5 V.

Create a resistor divider from V3P3 (3.3 V) to set COMPN ≈ 0.5 V.

Set R2 = 10 kΩ, set R1 = 56 kΩ

8.2.2.2.2 Sense Resistor

For optimal performance, the sense resistor must have the following characteristics:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{rms}^{2} \times R$. For example, if the rms motor current is 1 A and a 200-mΩ sense resistor is used, the resistor will dissipate $1\ A^2 \times 0.2\ \Omega = 0.2$ W. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. Measuring the actual sense-resistor temperature in a final system, along with the power MOSFETs, is always best because these are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, using multiple standard resistors in parallel, between the sense node and ground is a common practice. This configuration distributes the current and heat dissipation.

8.2.3 Brushed-DC and Solenoid Load

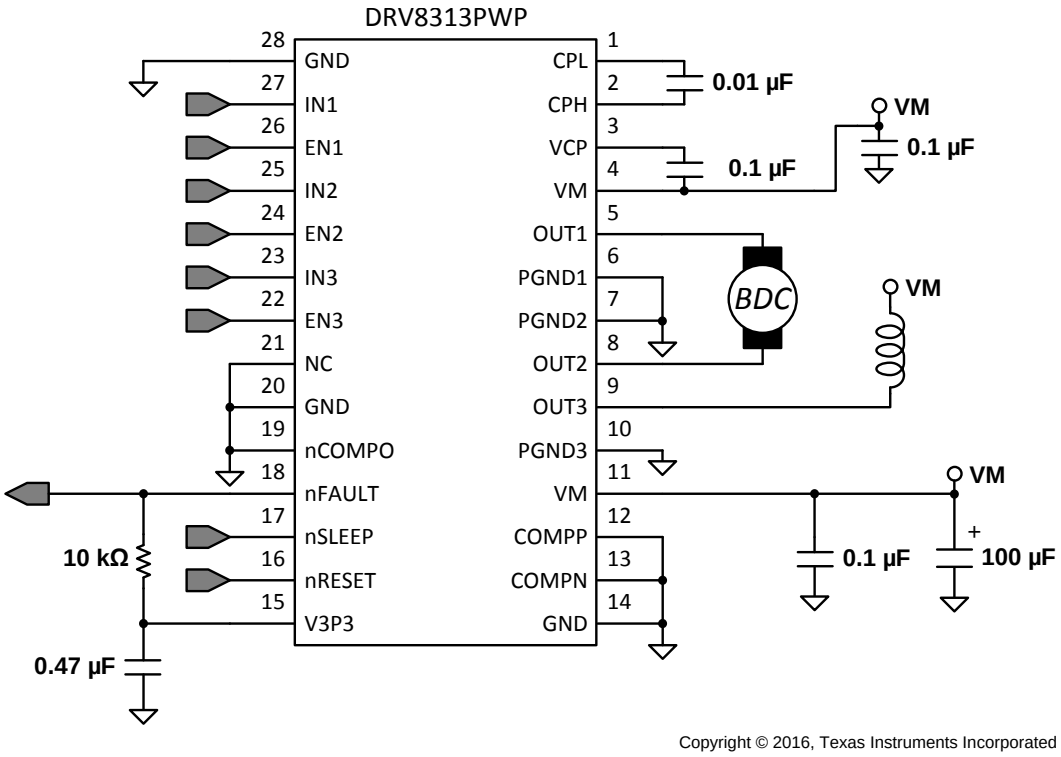


Figure 16. Brushed-DC and Solenoid Schematic

8.2.3.1 Design Requirements

Table 7 gives design input parameters for system design.

Table 7. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Brushed motor rms current	$I_{RMS, BDC}$	1.0 A
Brushed motor peak current	$I_{PEAK, BDC}$	2.0 A
Solenoid rms current	$I_{RMS, SOL}$	0.5 A
Solenoid peak current	$I_{PEAK, SOL}$	1.0 A

8.2.3.1.1 Detailed Design Procedure

Table 8. Brushed-DC Control

Function	IN1	EN1	IN2	EN2	OUT1	OUT2
Forward	1	1	0	1	H	L
Reverse	0	1	1	1	L	H
Brake (low-side slow decay)	0	1	0	1	L	L
High-side slow decay	1	1	1	1	H	H
Coast	X	0	X	0	Z	Z

Table 9. Solenoid Control (High-Side Load)

Function	IN3	EN3	OUT3
Coast / Off	X	0	Z
On	0	1	L
Brake	1	1	H

8.2.4 Three Solenoid Loads

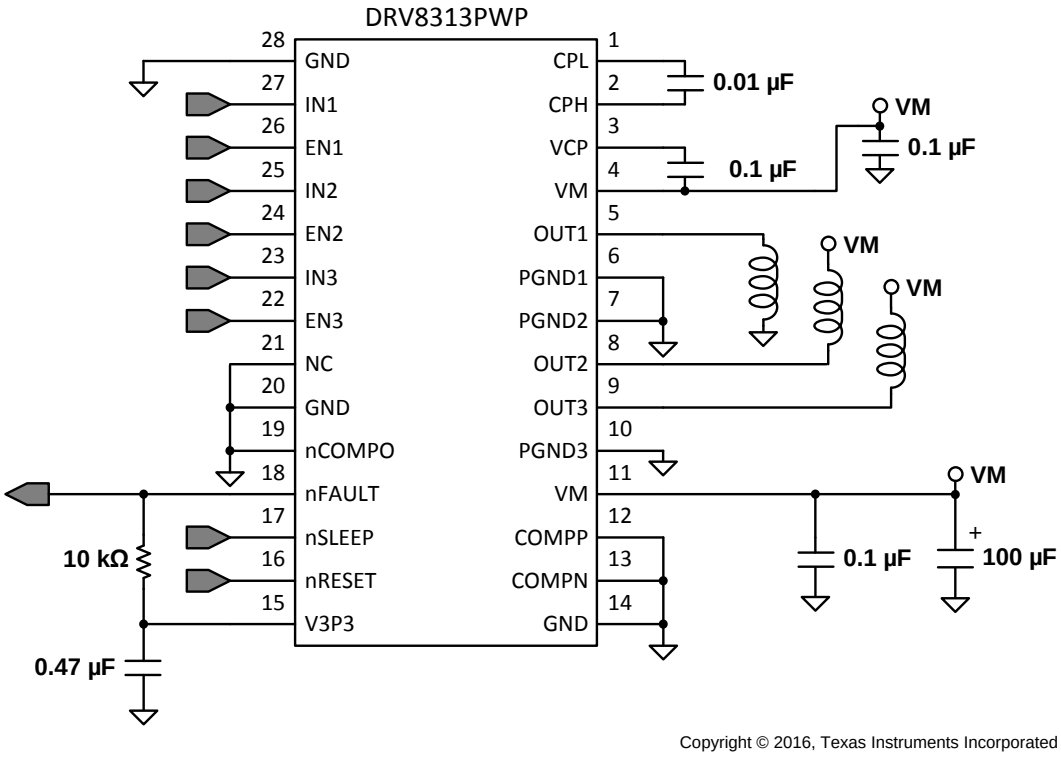


Figure 17. Three Independent Load Connections Schematic

8.2.4.1 Design Requirements

Table 10 gives design input parameters for system design.

Table 10. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Solenoid rms current	$I_{RMS, SOL}$	1.0 A
Solenoid peak current	$I_{PEAK, SOL}$	1.5 A

8.2.4.1.1 Detailed Design Procedure

Table 11. Solenoid Control (high-side load)

Function	IN2	EN2	OUT2
Coast / Off	X	0	Z
On	0	1	L
Brake	1	1	H

Table 12. Solenoid Control (low-side load)

Function	IN1	EN1	OUT1
Coast / Off	X	0	Z
On	1	1	H
Brake	0	1	L

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

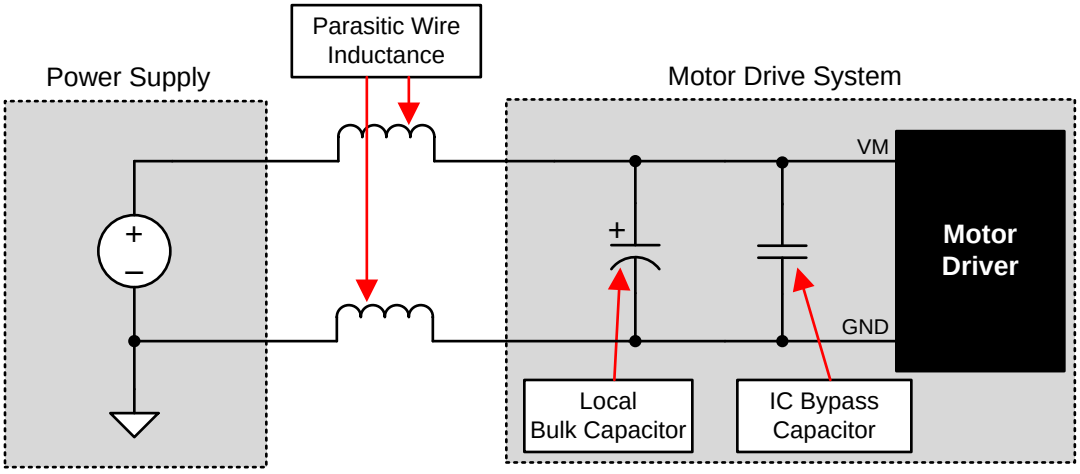


Figure 18. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the $I^2 \times r_{DS(on)}$ heat that is generated in the device.

In Figure 19 and Figure 20, the uncommitted comparator is not used. Because this is the case, the COMPP, COMPN, and COMPO pins are tied to GND.

10.2 Layout Example

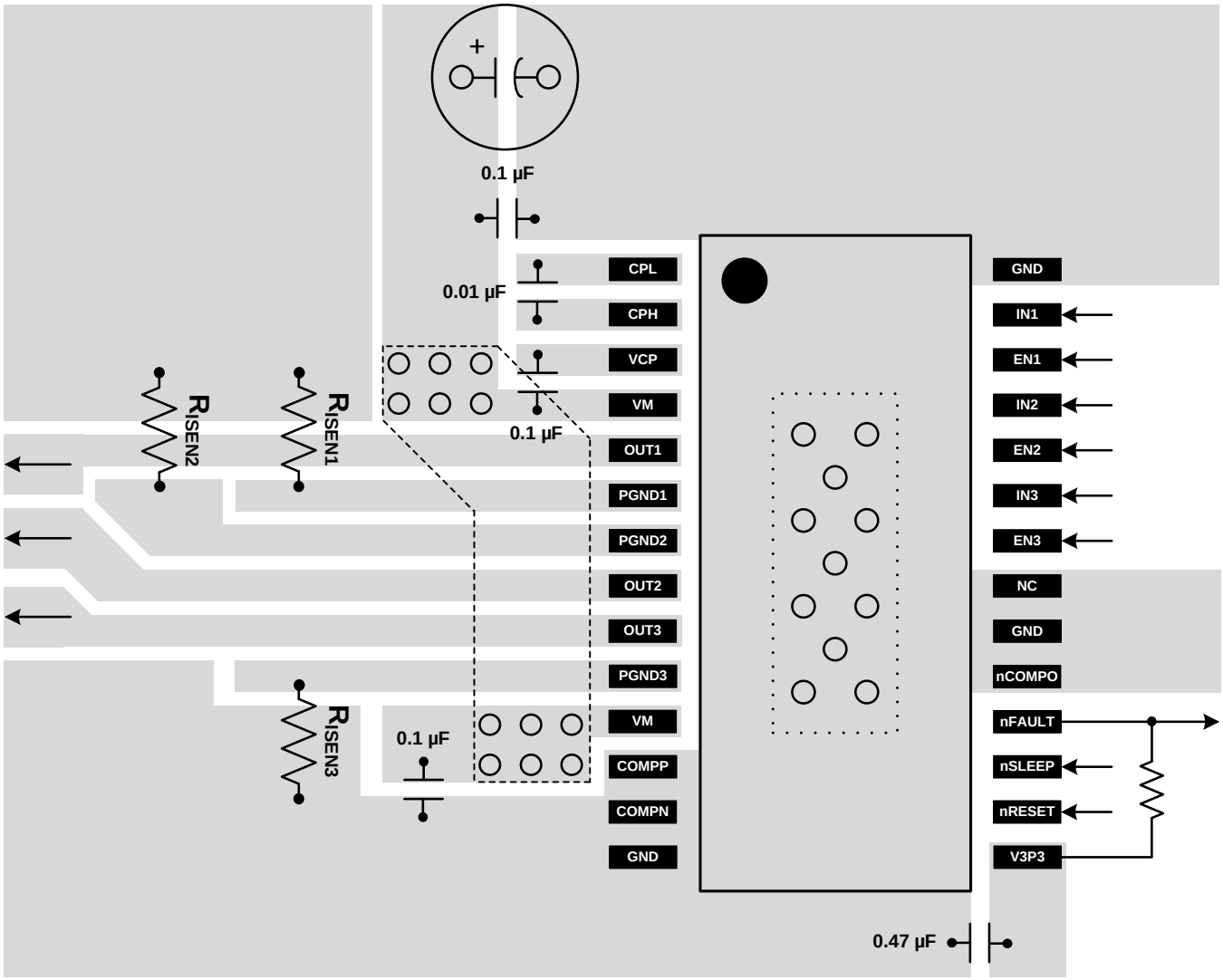


Figure 19. Recommended Layout Example For HTSSOP PWP Package

Layout Example (continued)

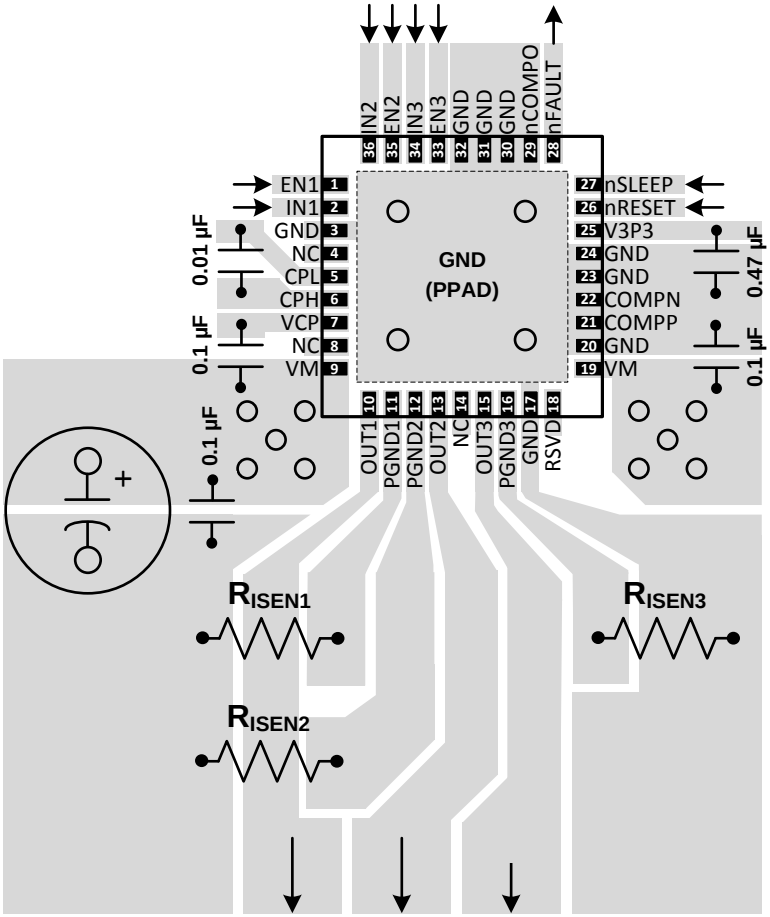


Figure 20. Recommended Layout Example For QFN RHH Package

10.3 Thermal Considerations

The DRV8313 has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Heatsinking

The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, add a number of vias to connect the thermal pad to the ground plane to accomplish this. On PCBs without internal planes, add copper area on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, use thermal vias to transfer the heat between the top and bottom layers.

For details about how to design the PCB, see *PowerPAD Thermally Enhanced Package* (SLMA002) and *PowerPAD Made Easy* (SLMA004), which are available at www.ti.com.

In general, providing more copper area allows the dissipation of more power.

10.4 Power Dissipation

The power dissipated in the output FET resistance, or $r_{DS(on)}$ dominates power dissipation in the DRV8313. A rough estimate of average power dissipation of each half-H-bridge when running a static load is:

$$P = r_{DS(on)} \times (I_{OUT})^2 \quad (2)$$

where

- P is the power dissipation of one H-bridge,
- $r_{DS(on)}$ is the resistance of each FET, and
- I_{OUT} is equal to the average current drawn by the load.

At start-up and fault conditions, this current is much higher than normal running current; remember to take these peak currents and their duration into consideration.

The total device dissipation is the power dissipated in each of the three half-H-bridges added together.

The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking.

Note that $r_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when sizing the heatsink.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *Calculating Motor Driver Power Dissipation*, SLVA504
- *DRV8313EVM User's Guide*, SLVU815
- *PowerPAD™ Thermally Enhanced Package*, SLMA002
- *PowerPAD™ Made Easy*, SLMA004
- *Sensored 3-Phase BLDC Motor Control Using MSP430*, SLAA503
- *Understanding Motor Driver Current Ratings*, SLVA505

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8313PWP	ACTIVE	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8313	Samples
DRV8313PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8313	Samples
DRV8313RHH	ACTIVE	VQFN	RHH	36	60	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8313	Samples
DRV8313RHHR	ACTIVE	VQFN	RHH	36	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8313	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

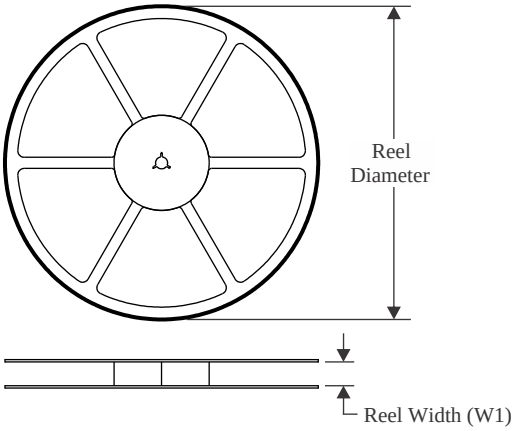
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

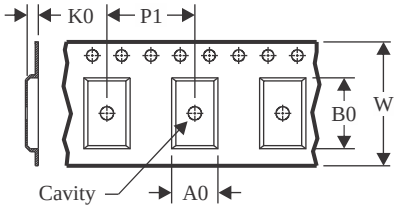
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

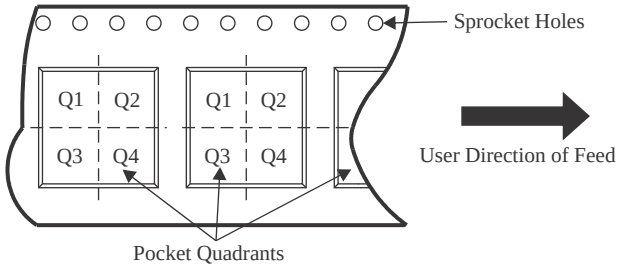


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

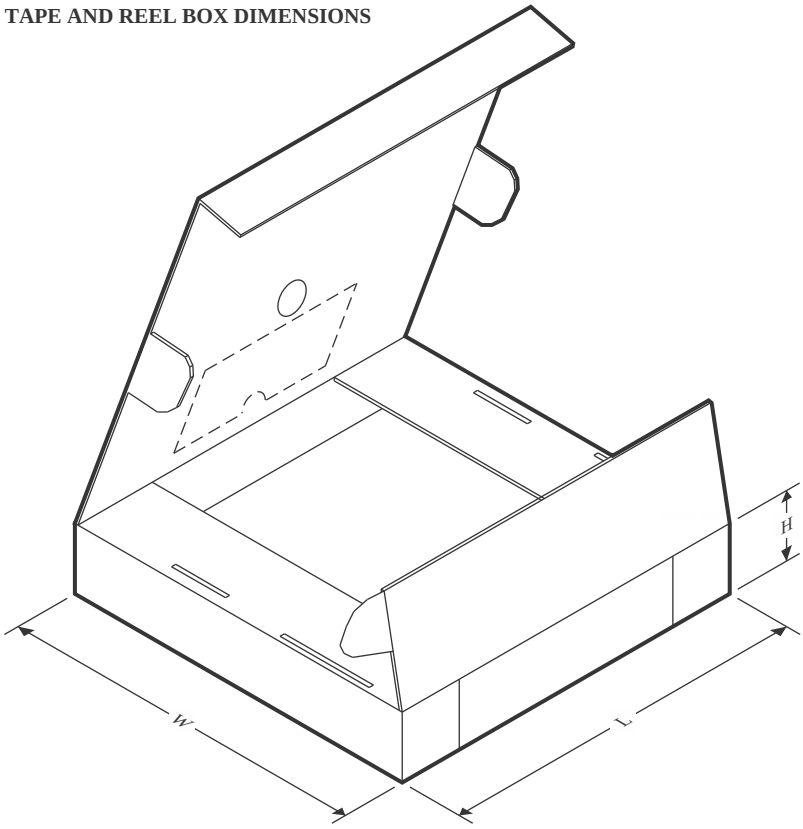
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8313PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
DRV8313RHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

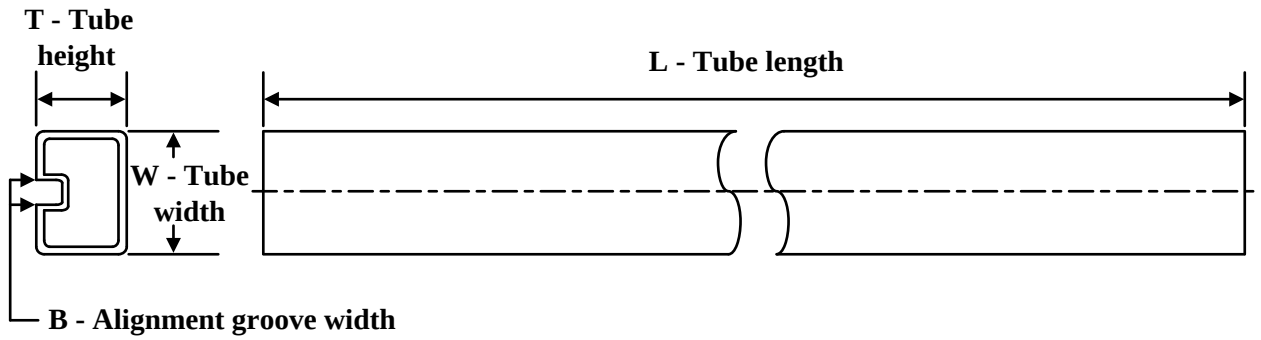
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8313PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
DRV8313RHHR	VQFN	RHH	36	2500	367.0	367.0	38.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV8313PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
DRV8313RHH	RHH	VQFN	36	60	381.5	7.92	2286	0

GENERIC PACKAGE VIEW

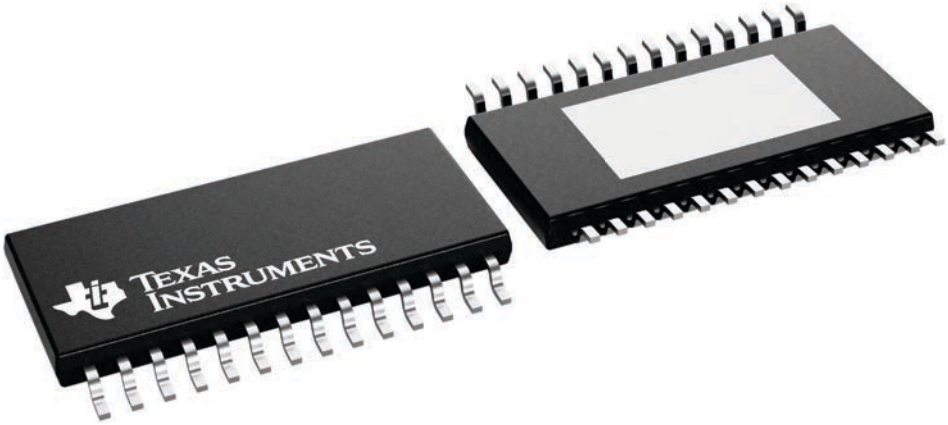
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

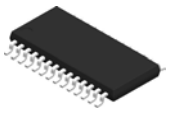
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

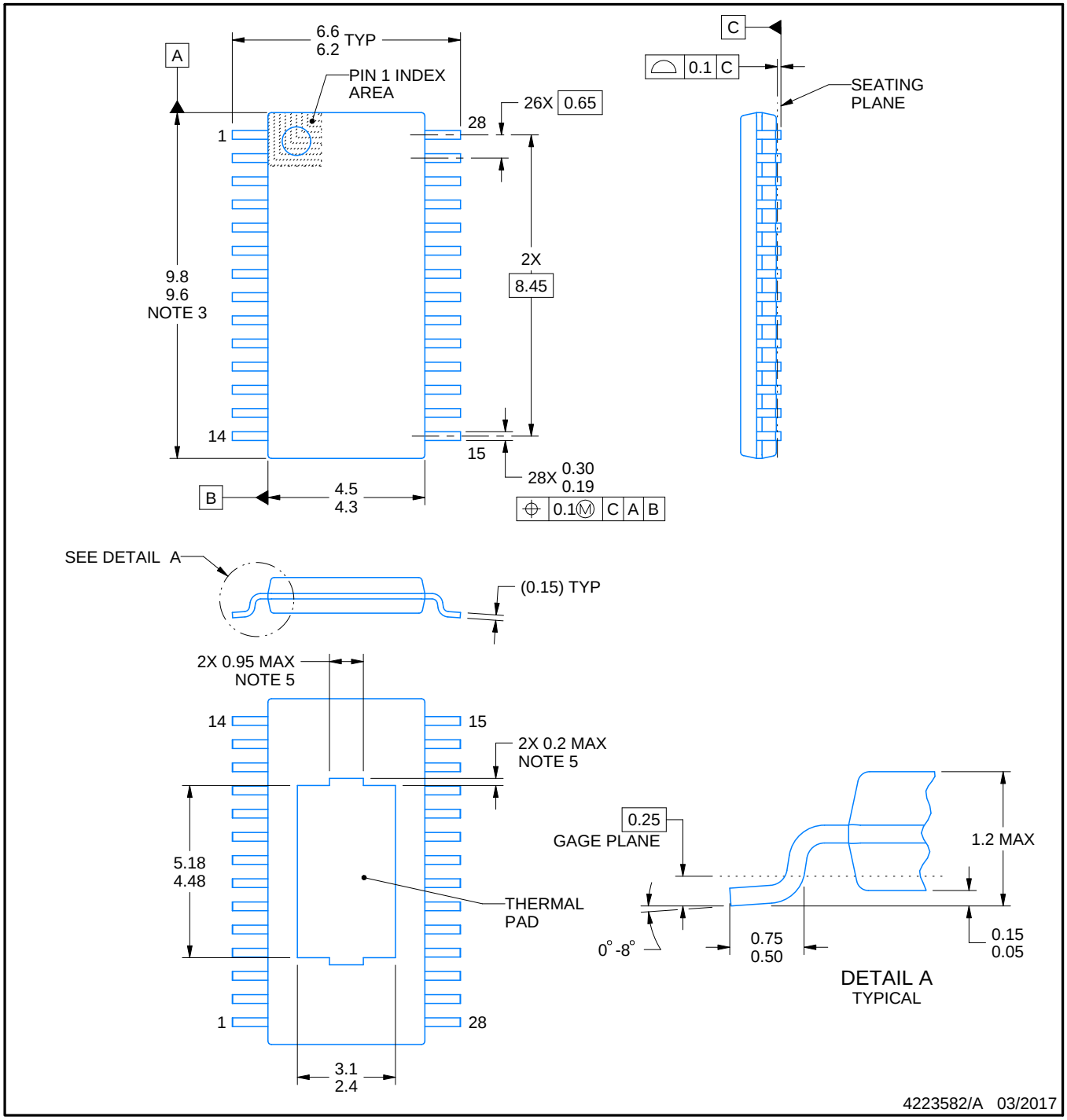
PACKAGE OUTLINE

PWP0028C



PowerPAD™ TSSOP - 1.2 mm max height

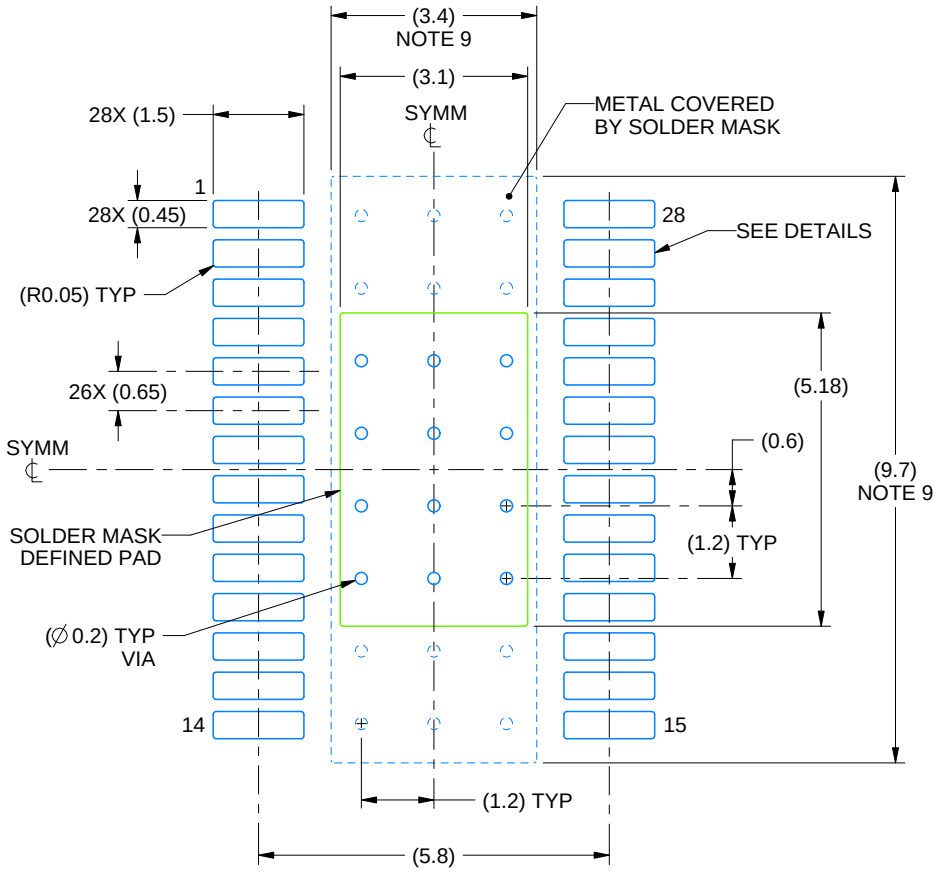
SMALL OUTLINE PACKAGE



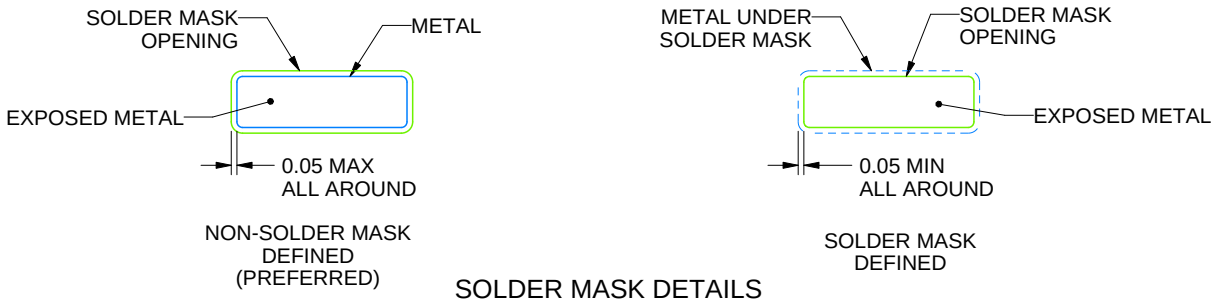
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

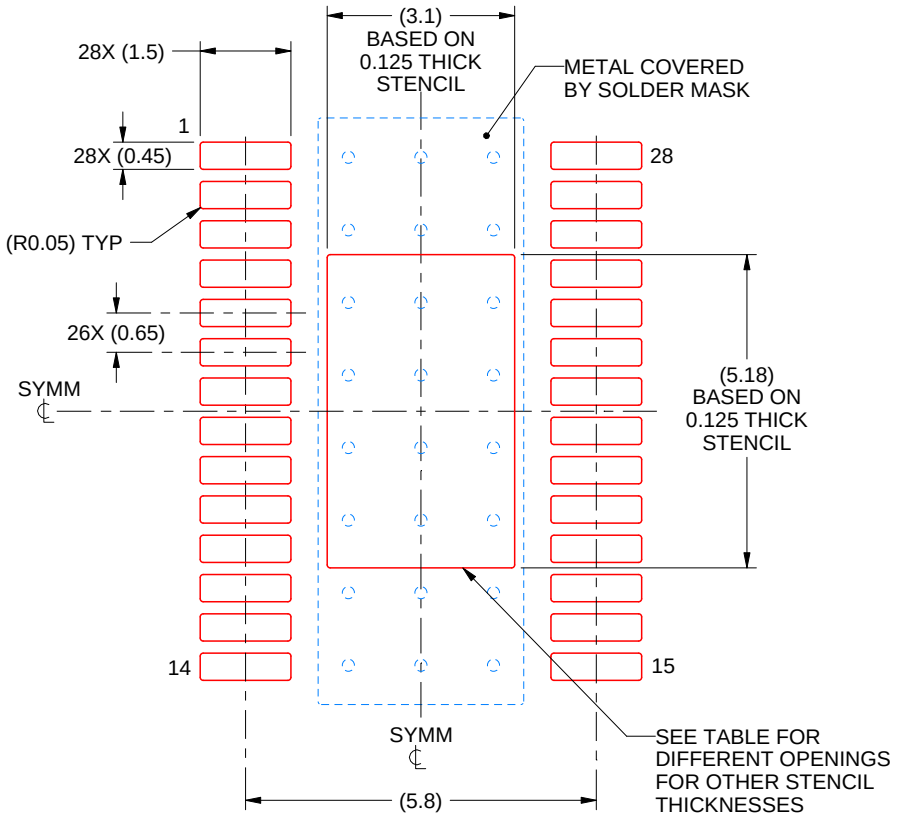


SOLDER MASK DETAILS

4223582/A 03/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 5.79
0.125	3.10 X 5.18 (SHOWN)
0.15	2.83 X 4.73
0.175	2.62 X 4.38

4223582/A 03/2017

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

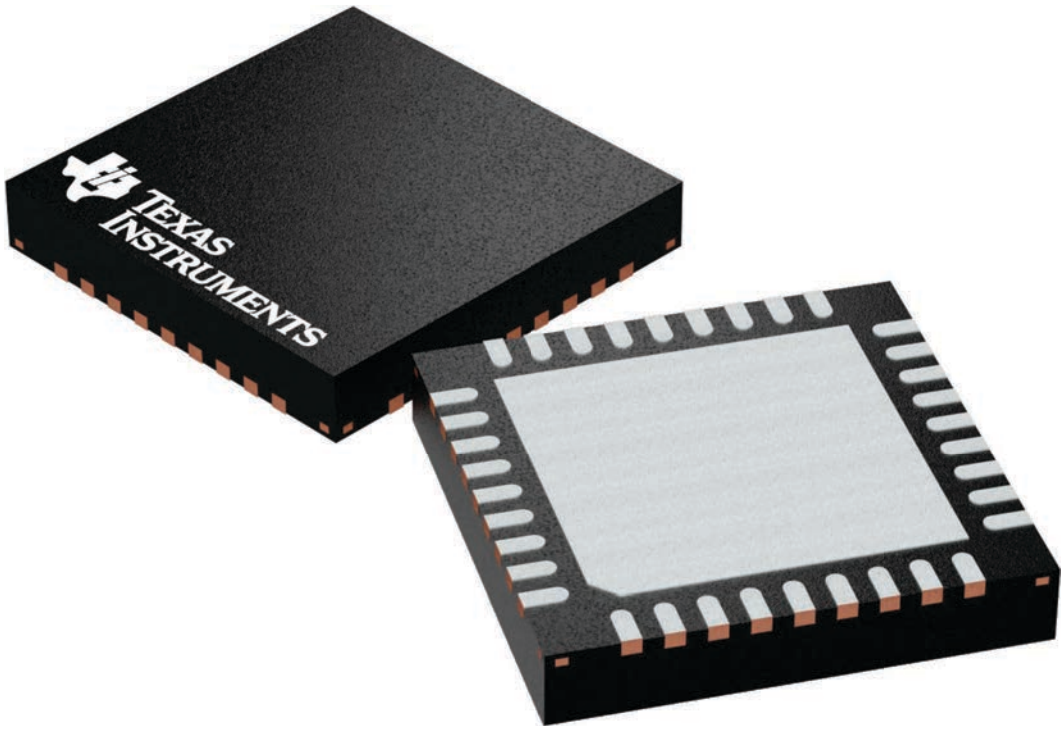
RHH 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



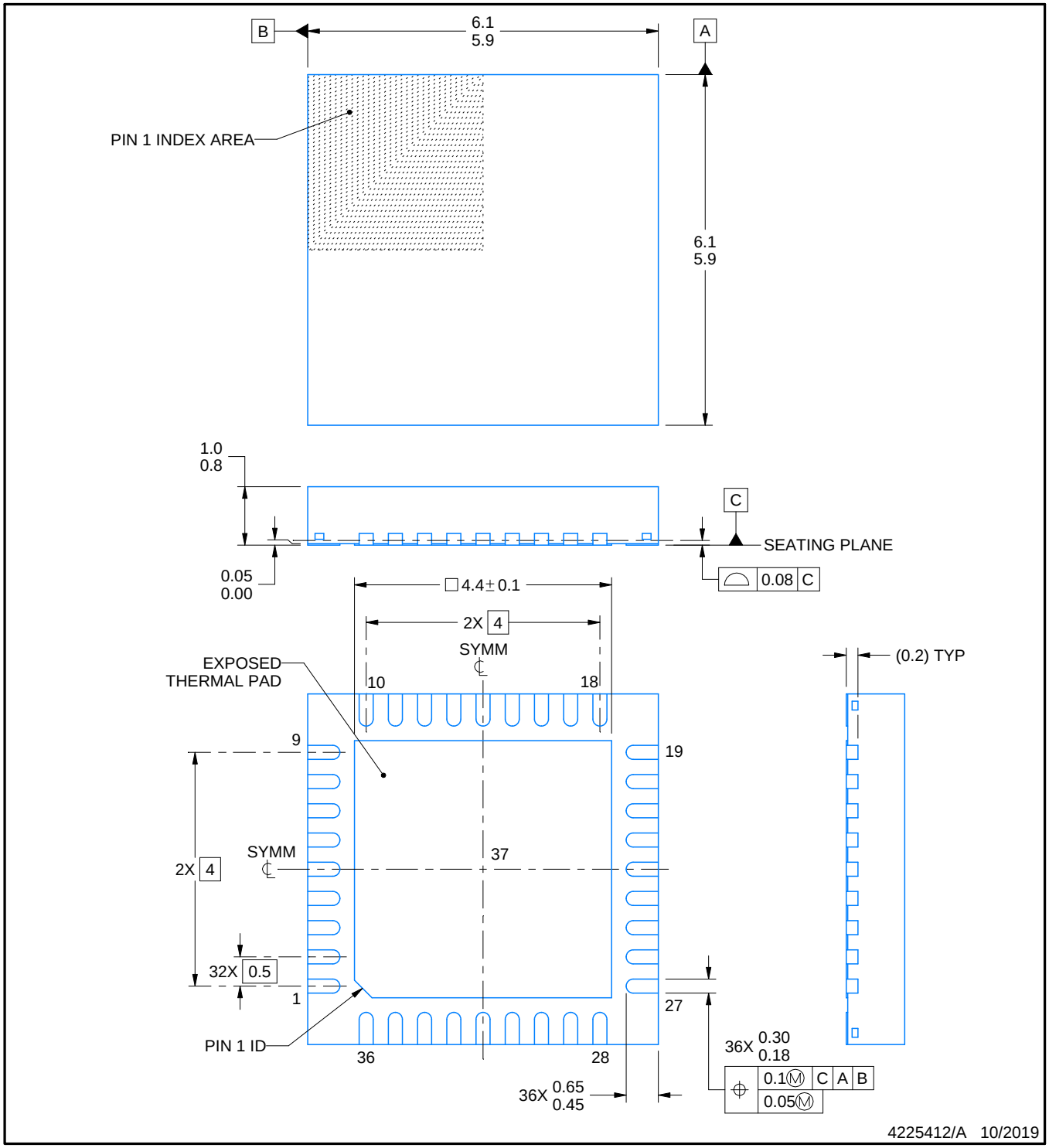
4225440/A

RHH0036C

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

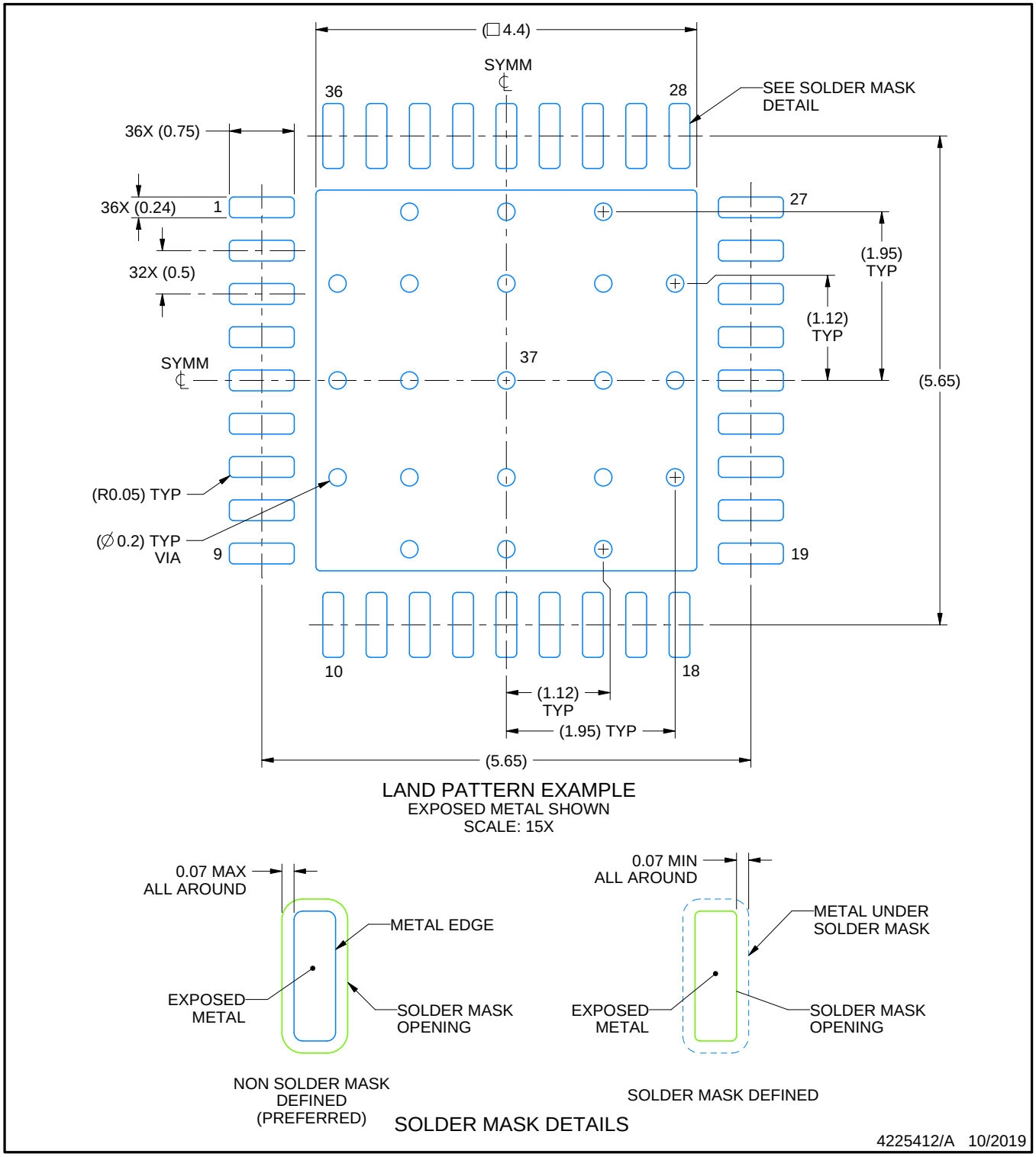
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHH0036C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

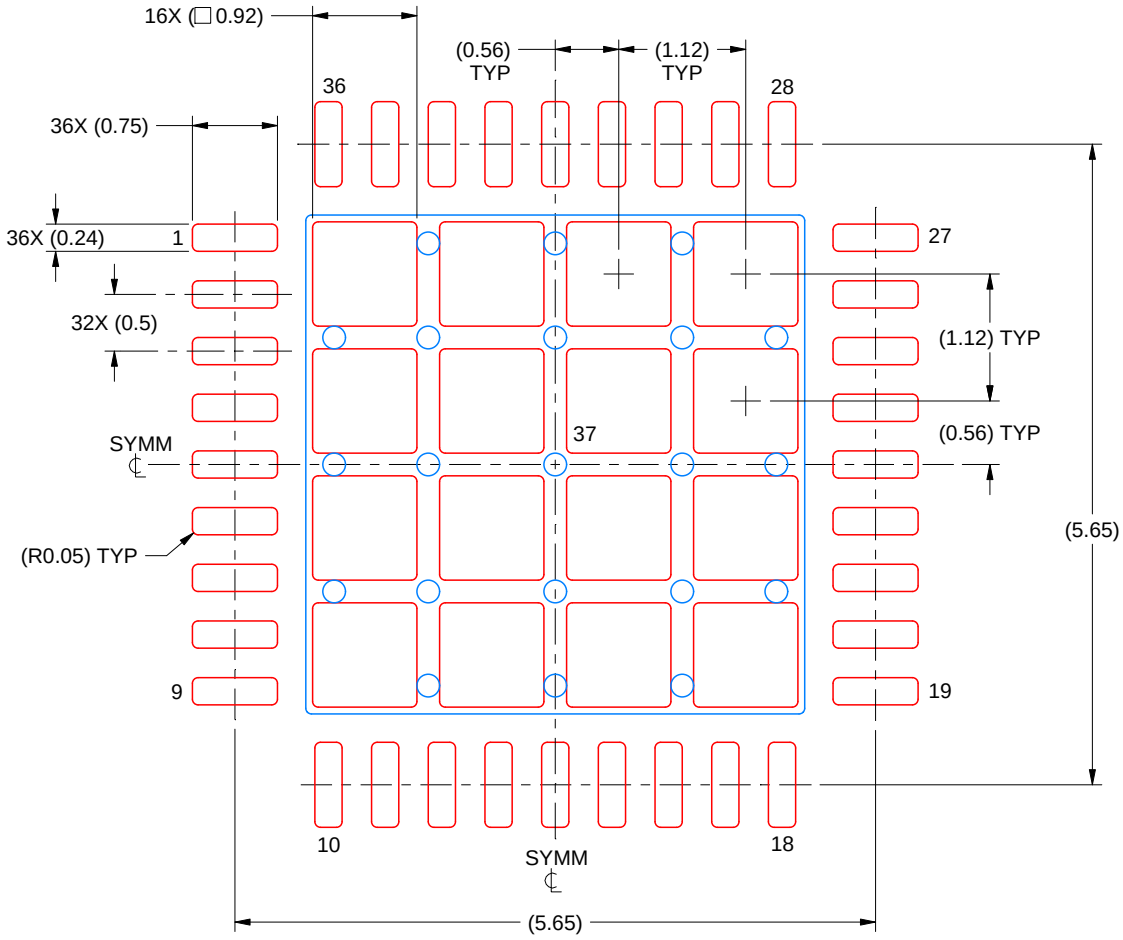
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHH0036C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225412/A 10/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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