

HIGH-SPEED FULLY DIFFERENTIAL I/O AMPLIFIERS

FEATURES

- **High Performance**
 - 100 MHz, -3 dB Bandwidth
 - 50 V/ μ s Slew Rate
 - 75 dB Total Harmonic Distortion at 1 MHz ($V_o = 2 V_{pp}$)
 - 5.4 nV/ \sqrt{Hz} Input-Referred Noise (10 kHz)
- **Differential Input/Differential Output**
 - **Balanced Outputs Reject Common-Mode Noise**
 - **Differential Reduced Second Harmonic Distortion**
- **Power Supply Range**
 - $V_{DD} = 3.3$ V

DESCRIPTION

The THS412x is one in a family of fully differential-input, differential-output devices fabricated using Texas Instruments' state-of-the-art submicron CMOS process.

The THS412x consists of a true, fully differential signal path from input to output. This results in excellent common-mode noise rejection and improved total harmonic distortion.

KEY APPLICATIONS

- **Simple Single-Ended To Differential Conversion**
- **Differential ADC Driver/Differential Antialiasing**
- **Differential Transmitter and Receiver**
- **Output Level Shifter**

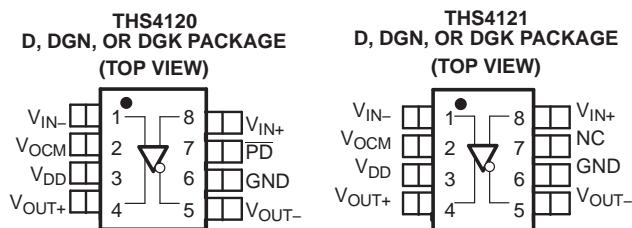


Table 1. HIGH-SPEED DIFFERENTIAL I/O FAMILY

DEVICE	NUMBER OF CHANNELS	POWERDOWN
THS4120 ⁽¹⁾	1	Yes
THS4121	1	—

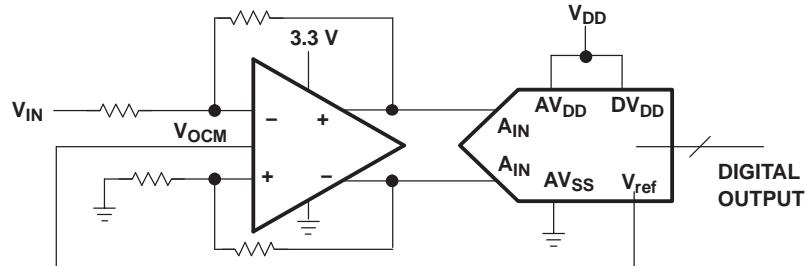
(1) For proper functionality, an external 10-k Ω pullup resistor is required between the PD pin and the positive supply.

RELATED DEVICES

DEVICE ⁽¹⁾	DESCRIPTION	SINGLE SUPPLY VOLTAGE RANGE	SPLIT SUPPLY VOLTAGE RANGE
THS413x	150 MHz, 51 V/ μ s, 1.3 nV/ \sqrt{Hz}	5 V to 30 V	± 2.5 to ± 15
THS414x	160 MHz, 450 V/ μ s, 6.5 nV/ \sqrt{Hz}	5 V to 30 V	± 2.5 to ± 15
THS415x	150 MHz, 650 V/ μ s, 7.6 nV/ \sqrt{Hz}	5 V to 30 V	± 2.5 to ± 15

(1) See the TI Web site for additional high-speed amplifier devices.

TYPICAL A/D APPLICATION CIRCUIT



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T _A	PACKAGED DEVICES					EVALUATION MODULES	
	SMALL OUTLINE(D)	MSOP PowerPAD™		MSOP			
		(DGN)	SYMBOL	(DGK)	SYMBOL		
0°C to 70°C	THS4120CD	THS4120CDGN	ARL	THS4120CDGK	ATZ	THS4120EVM	
	THS4121CD	THS4121CDGN	ASB	THS4121CDGK	ATO	THS4121EVM	
-40°C to 85°C	THS4120ID	THS4120IDGN	ARM	THS4120IDGK	ARN	-	
	THS4121ID	THS4121IDGN	ASC	THS4121IDGK	ASN	-	

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		UNIT
V _I	Supply voltage, GND to V _{DD}	3.6 V
I _O	Input voltage	±V _{DD}
V _{ID}	Output current (sink) ⁽²⁾	110 mA
T _A	Differential input voltage	±V _{DD}
T _J	Continuous total power dissipation	See Dissipation Rating Table
T _J	Maximum junction temperature ⁽³⁾	150°C
T _J	Maximum junction temperature, continuous operation, long-term reliability ⁽⁴⁾	125°C
T _A	Operating free-air temperature C suffix	0°C to 70°C
	I suffix	-40°C to 85°C
T _{stg}	Storage Temperature	-65°C to 150°C
Lead temperature 1.6 mm (1/16 Inch) from case for 10 seconds		300°C
ESD ratings	HBM	4000 V
	CDM	1500 V
	MM	200 V

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The THS412x may incorporate a PowerPad™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical brief [SLMA002](#) and [SLMA004](#) for more information about utilizing the PowerPad™ thermally enhanced package.
- (3) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.
- (4) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

DISSIPATION RATING TABLE

PACKAGE	θ _{JA} ⁽¹⁾ (°C/W)	θ _{JC} (°C/W)	POWER RATING ⁽²⁾	
			T _A = 25°C	T _A = 85°C
D	97.5	38.3	1.02 W	410 mW
DGN	58.4	4.7	1.71 W	685 mW
DGK	260	54.2	385 mW	154 mW

- (1) This data was taken using the JEDEC standard High-K test PCB.
- (2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V _{DD}	Supply voltage	Split supply	±1.5	±1.65	±1.75	V
		Single supply	3	3.3	3.5	
T _A	Operating free-air temperature	C suffix	0	70	70	°C
		I suffix	−40	85	85	

ELECTRICAL CHARACTERISTICS

 V_{DD} = 3.3 V, R_L = 800 Ω, T_A = 25°C (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC PERFORMANCE						
BW	Small-signal bandwidth (−3 dB)	V _{DD} = 3.3 V, Gain = 1, R _f = 200 Ω	100			MHz
SR	Slew rate ⁽²⁾	V _{DD} = 3.3 V, Gain = 1	55			V/μs
t _s	Settling time to 0.1%	Differential step voltage = 2 V _{PP} , Gain = 1	60			ns
	Settling time to 0.01%		292			
DISTORTION PERFORMANCE						
THD	Total harmonic distortion Differential input, differential output Gain = 1, R _f = 200 Ω, R _L = 800 Ω, V _O = 2 V _{PP}	V _{DD} = 3.3 V, f = 1 MHz	−75			dB
THD	Total harmonic distortion Differential input, differential output Gain = 1, R _f = 200 Ω, R _L = 800 Ω, V _O = 4 V _{PP}	V _{DD} = 3.3 V, f = 1 MHz	−66			dB
	Spurious free dynamic range (SFDR) Differential input, differential output, V _O = 4 V _{PP}	R _f = 200 Ω, f = 1 MHz	−69			dB
	Third intermodulation distortion	V _I = 0.071 V _{RMS}	Gain = 1, f = 10 MHz	−75		dBc
NOISE PERFORMANCE						
V _n	Input voltage noise	f = 10 kHz	5.4			nV/√Hz
I _n	Input current noise	f = 10 kHz	1			fA/√Hz
DC PERFORMANCE						
V _S		T _A = 25°C	60	66		dB
		T _A = full range	66			
V _S	Input offset voltage	T _A = 25°C	3	8		mV
		T _A = full range	4	9		
	Input offset voltage, referred to V _{OCM}	T _A = 25°C	5	13		
		T _A = full range	14			
Offset voltage drift		T _A = full range	25			μV/°C
I _{IB}	Input bias current	T _A = full range	1.2			pA
I _{OS}	Input offset current		100			fA
	Current offset drift	T _A = full range	5			fA/°C

(1) The full range temperature is 0°C to 70°C for the C suffix, and −40°C to 85°C for the I suffix.

(2) Slew rate is measured differentially from an output level range of 25% to 75%.

ELECTRICAL CHARACTERISTICS (Continued) $V_{DD} = 3.3 \text{ V}$, $R_L = 800 \Omega$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS					
CMRR Common-mode rejection ratio	$T_A = \text{full range}$	64	96		dB
V_{ICR} Common-mode input voltage range	$T_A = \text{full range}$	0.65 to $V_{DD} - 0.1$	0.35 to V_{DD}		V
r_i Input resistance (dc level)	Measured into each input terminal		820		$\text{M}\Omega$
C_i Input capacitance, closed loop			3		pF
r_o Output resistance	See Figure 16		1		Ω
OUTPUT CHARACTERISTICS					
V_{OH} High-level output Voltage	$V_{IC} = V_{DD}/2$, $V_{DD} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$	3.05	3.15		V
V_{OL} Low-level output Voltage	$V_{IC} = V_{DD}/2$, $V_{DD} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$	0.25	0.15		V
I_O Output current (sink), $R_L = 7 \Omega$	$V_{DD} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$	80	100		mA
I_O Output current (source), $R_L = 7 \Omega$	$V_{DD} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$	20	25		mA
POWER SUPPLY					
V_{DD} Supply voltage range	Single supply		3.3		V
I_{DD} Quiescent current (per amplifier)	$V_{DD} = 3.3 \text{ V}$	$T_A = 25^\circ\text{C}$	11	13.5	mA
		$T_A = \text{full range}$		16	
PSRR Power-supply rejection ratio	$T_A = 25^\circ\text{C}$	68	85		dB
POWER-DOWN CHARACTERISTICS (THS4120 ONLY)					
Power-down voltage level ⁽²⁾	Enable		>1.4		V
	Power down		<1.2		
Power-down quiescent current	$T_A = 25^\circ\text{C}$		120		μA
	$T_A = \text{full range}$		130		
t_{on} Turn-on time delay			4.8		μs
t_{off} Turn-off time delay	50% of final supply current value		3		ns
Z_o Output impedance	$f = 1 \text{ MHz}$		1		$\text{k}\Omega$

(1) The full range temperature is 0°C to 70°C for the C suffix, and -40°C to 85°C for the I suffix.

(2) For detail information on the power-down circuit, see the power-down section in the application section of this data sheet.

TYPICAL CHARACTERISTICS**Table of Graphs**

		FIGURE
Small-signal frequency response		1
SR Slew rate		2
THD Total harmonic distortion	vs Frequency	3
	vs Output voltage	4
Harmonic distortion	vs Frequency	5, 6, 7
	vs Output voltage	8, 9
Third intermodulation distortion	vs Output voltage	10
V_O Output voltage	vs Load resistance	11
Settling time		12
V_n Voltage noise	vs Frequency	13
V_{OO} Output offset voltage	vs Common-mode input voltage	14
CMMR Common-mode rejection ratio	vs Frequency	15
Z_{os} Single-ended output impedance (closed loop)	vs Frequency	16

TYPICAL CHARACTERISTICS (continued)

		FIGURE
z_o	Single-ended (V_{OCM}) input impedance vs Frequency	17

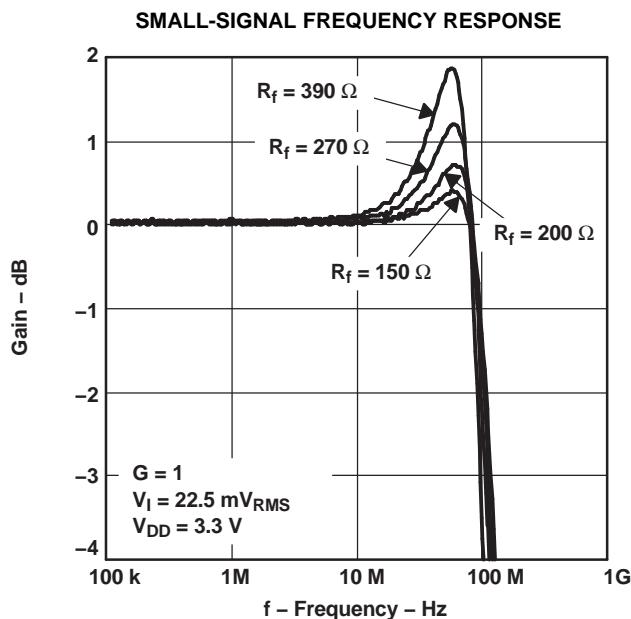


Figure 1.

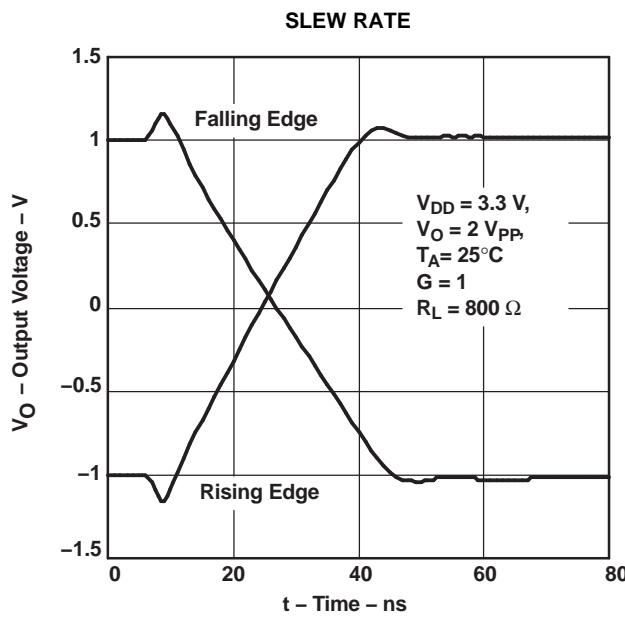


Figure 2.

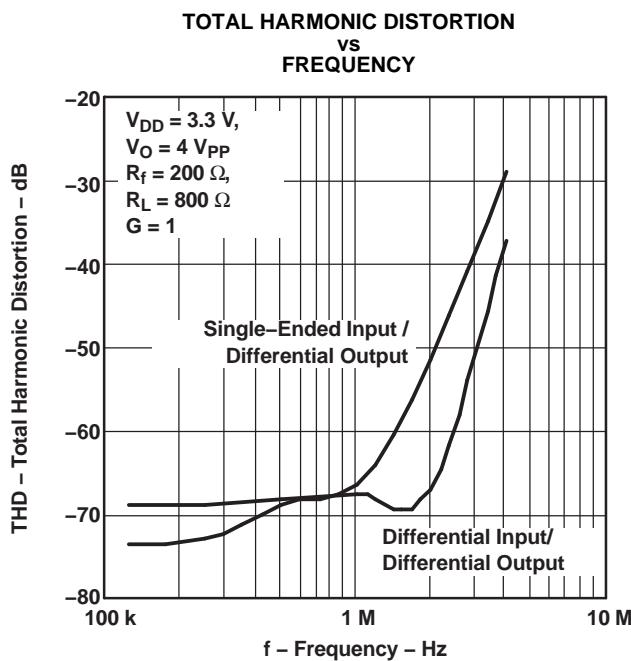


Figure 3.

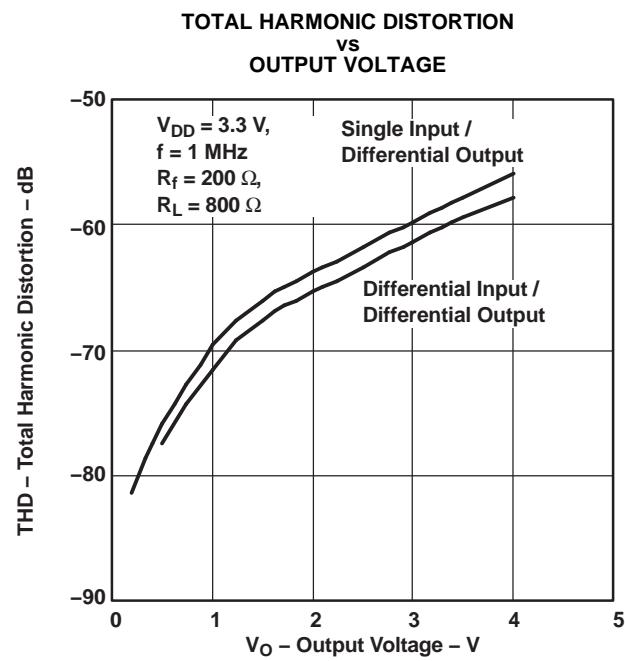


Figure 4.

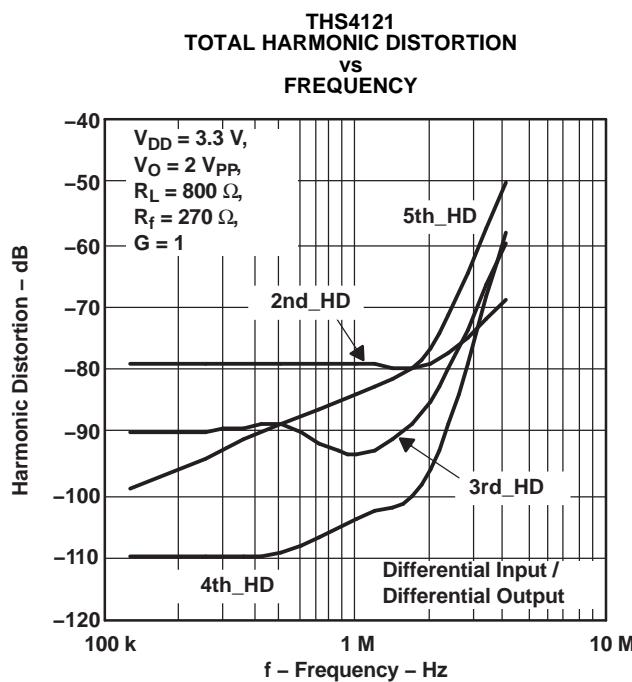


Figure 5.

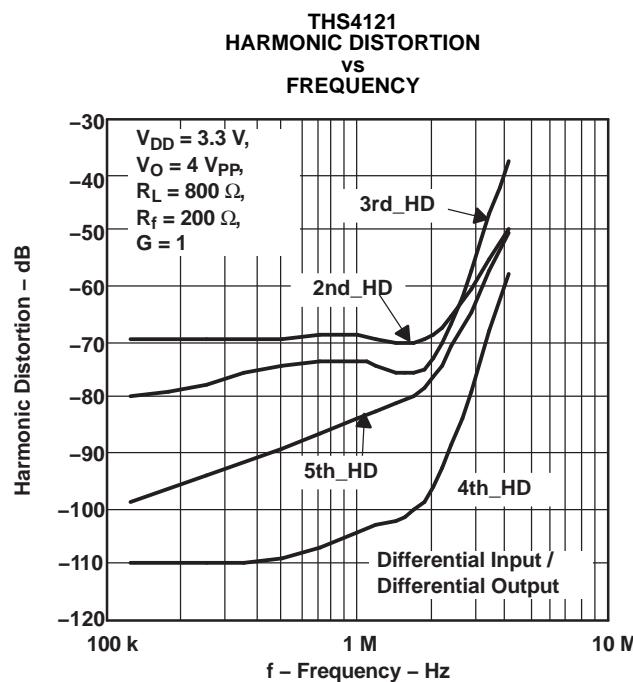


Figure 6.

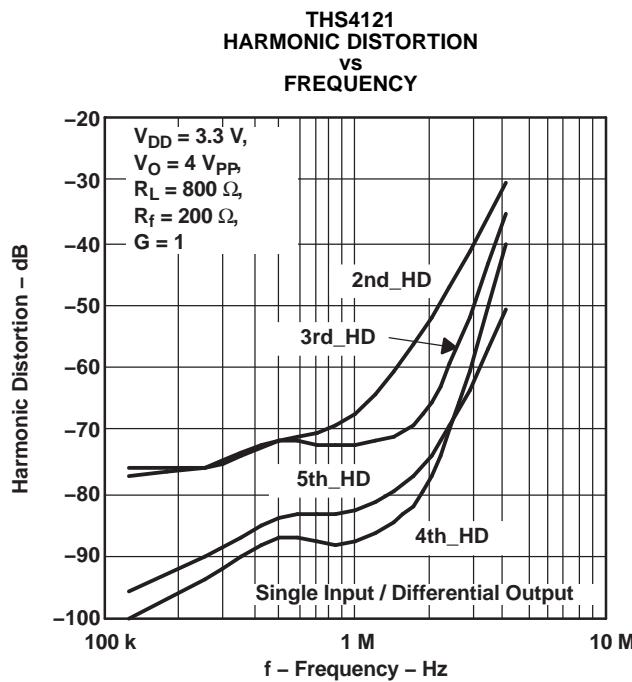


Figure 7.

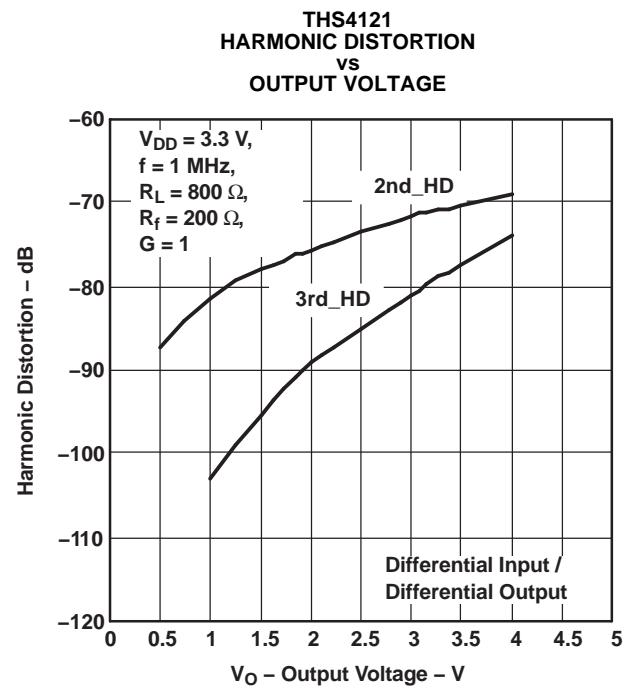


Figure 8.

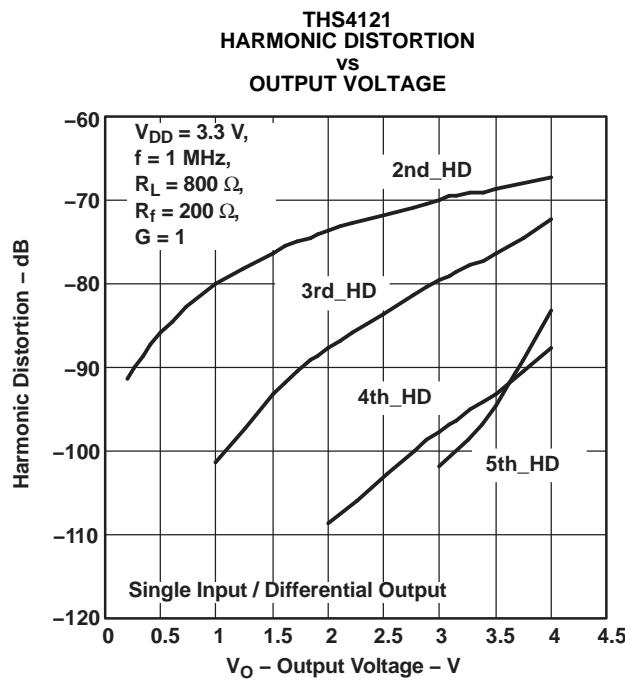


Figure 9.

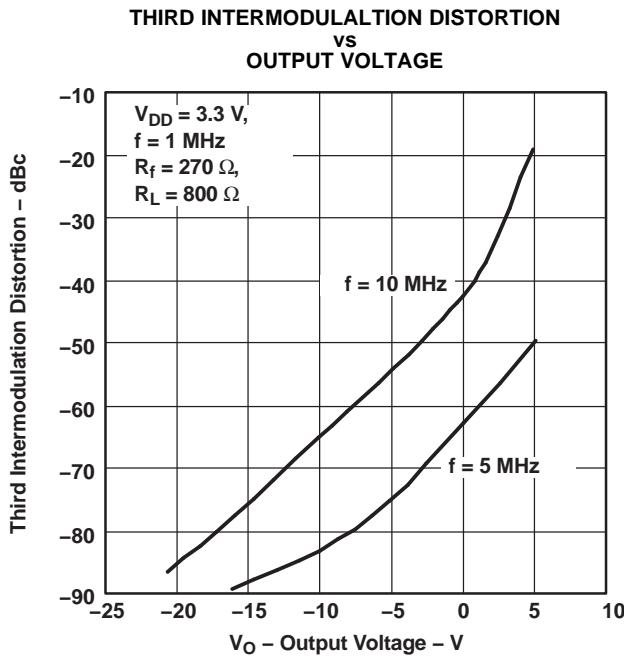


Figure 10.

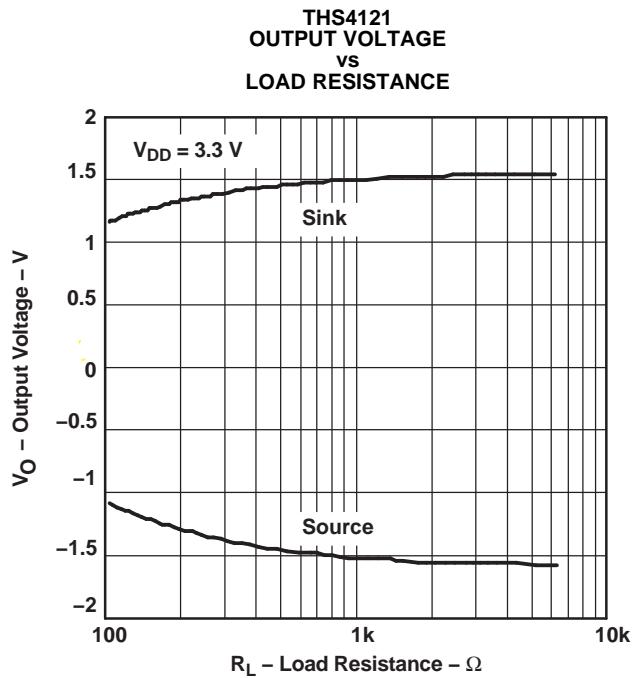


Figure 11.

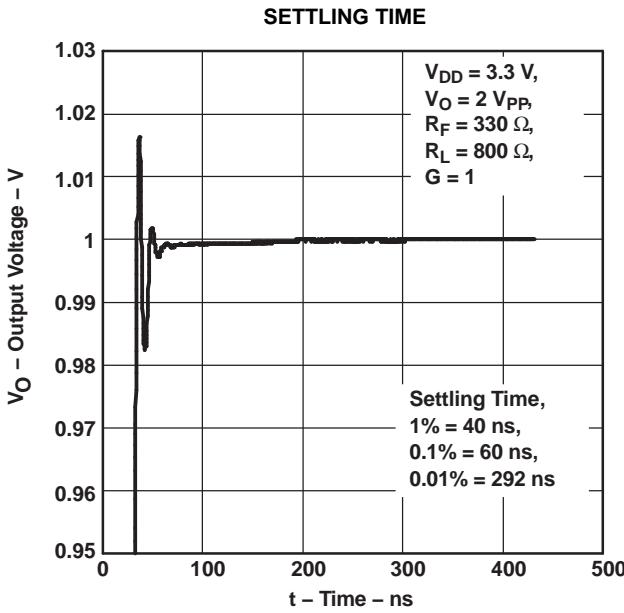


Figure 12.

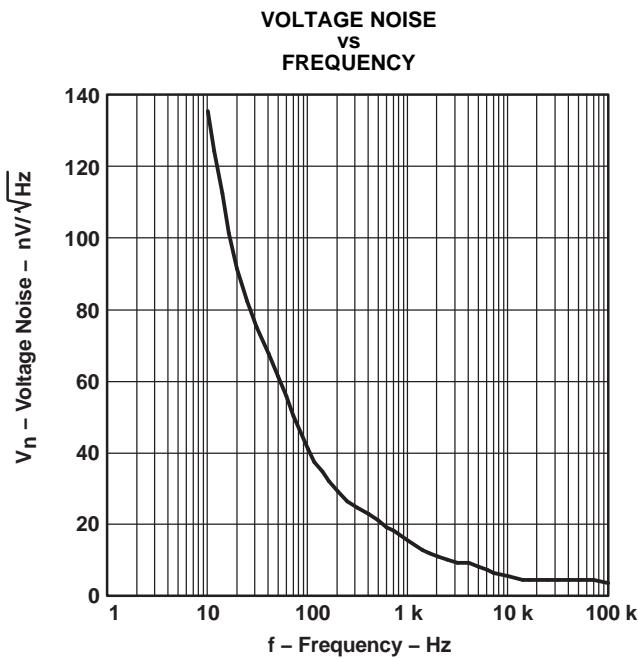


Figure 13.

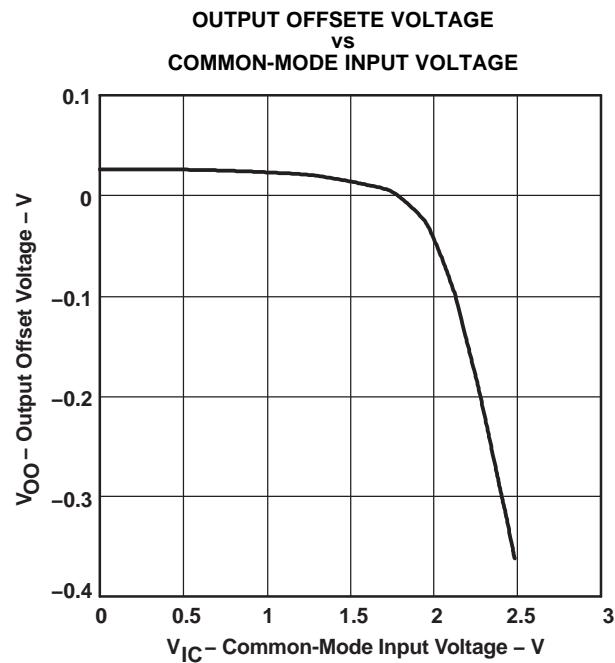


Figure 14.

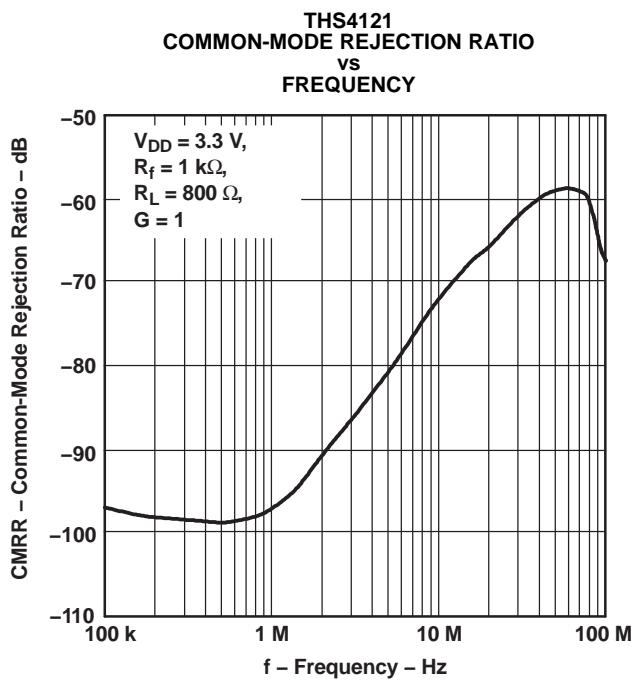


Figure 15.

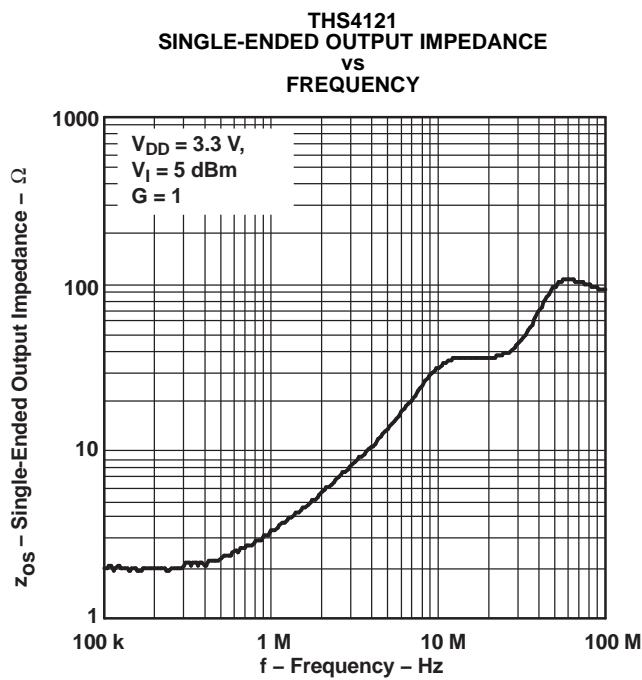


Figure 16.

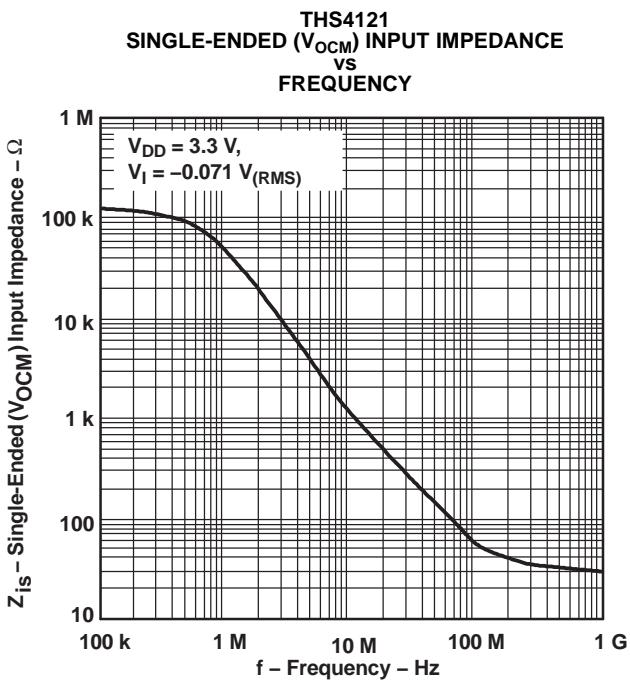


Figure 17.

APPLICATION INFORMATION

RESISTOR MATCHING

Resistor matching is important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized.

V_{OCM} sets the dc level of the output signals. If no voltage is applied to the V_{OCM} pin, it is set to the midrail voltage internally defined as:

$$\frac{(V_{DD}) + (V_{SS})}{2} \quad (1)$$

In the differential mode, the V_{OCM} on the two outputs cancel each other. Therefore, the output in the differential mode is the same as the input with the gain of 1. V_{OCM} has a high bandwidth capability up to the typical operation range of the amplifier. For the prevention of noise going through the device, use a $0.1\text{-}\mu\text{F}$ capacitor on the V_{OCM} pin as a bypass capacitor. The following graph shows the simplified diagram of the THS412x.

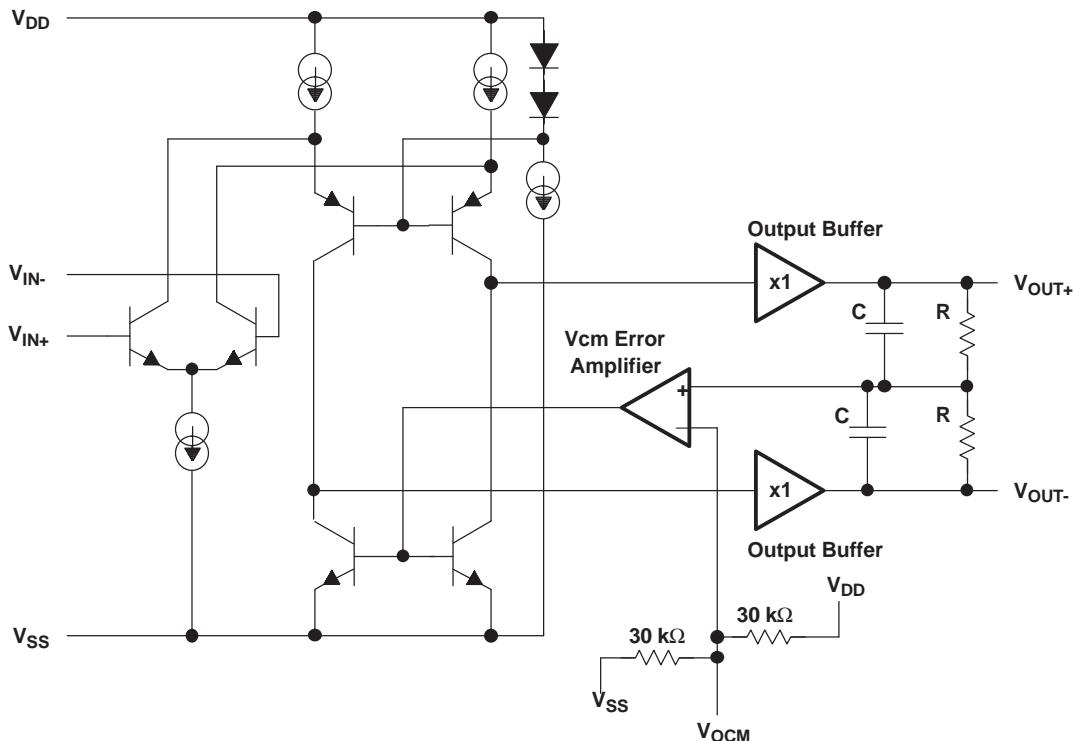


Figure 18. THS412x Simplified Diagram

APPLICATION INFORMATION (continued)

DATA CONVERTERS

Data converters are one of the most popular applications for the fully differential amplifiers.

Fully differential amplifiers can operate with a single supply. V_{OCM} defaults to the midrail voltage, $V_{DD}/2$. The differential output may be fed into a data converter. This method eliminates the use of a transformer in the circuit. If the ADC has a reference voltage output (V_{ref}), then it is recommended to connect it directly to the V_{OCM} of the amplifier using a bypass capacitor for stability. For proper operation, the input common-mode voltage to the input common-mode input terminal of the amplifier should not exceed the common-mode input voltage range.

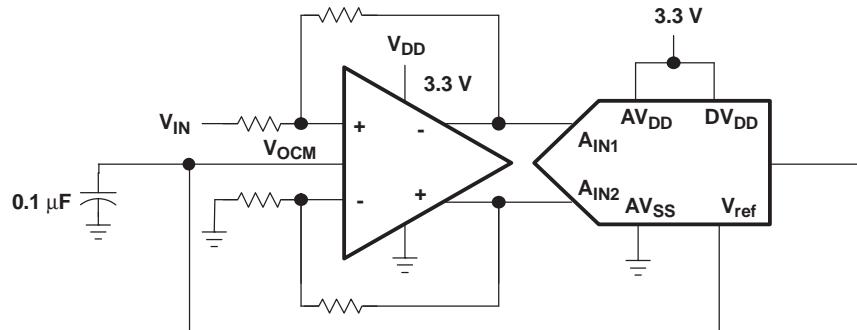


Figure 19. Differential Amplifier Using a Single Supply

Some single-supply applications may require the input voltage to exceed the common-mode input voltage range. In such cases, the following circuit configuration is suggested to bring the common-mode input voltage within the specifications of the amplifier.

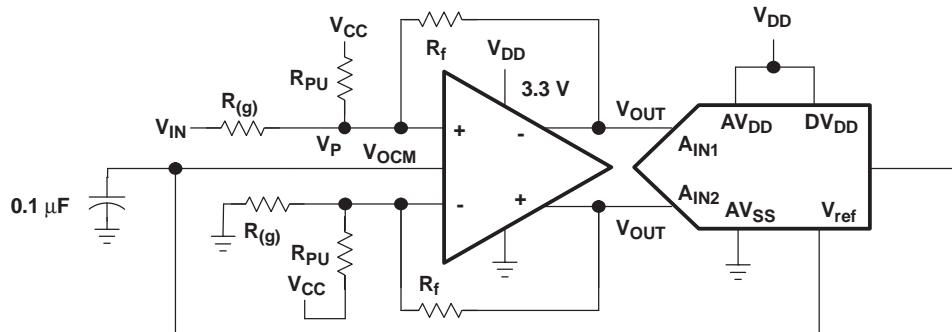


Figure 20. Circuit With Improved Common-Mode Input Voltage

The following equation is used to calculate R_{PU} :

$$R_{PU} = \frac{V_P - V_{DD}}{(V_{IN} - V_P) \frac{1}{R_{(g)}} + (V_{OUT} - V_P) \frac{1}{R_f}} \quad (2)$$

APPLICATION INFORMATION (continued)

DRIVING A CAPACITIVE LOAD

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS412x has been internally compensated to maximize its bandwidth and slew rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device's phase margin leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in [Figure 21](#). A minimum value of 20 Ω should work well for most applications. For example, in 50- Ω transmission systems, setting the series resistor value to 50 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

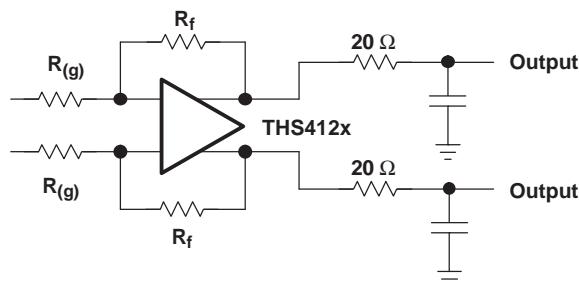


Figure 21. Driving a Capacitive Load

ACTIVE ANTIALIAS FILTERING

For signal conditioning in ADC applications, it is important to limit the input frequency to the ADC. Low-pass filters can prevent the aliasing of the high-frequency noise with the frequency of operation. [Figure 22](#) presents a method by which the noise may be filtered in the THS412x. Proper ground referencing should be considered.

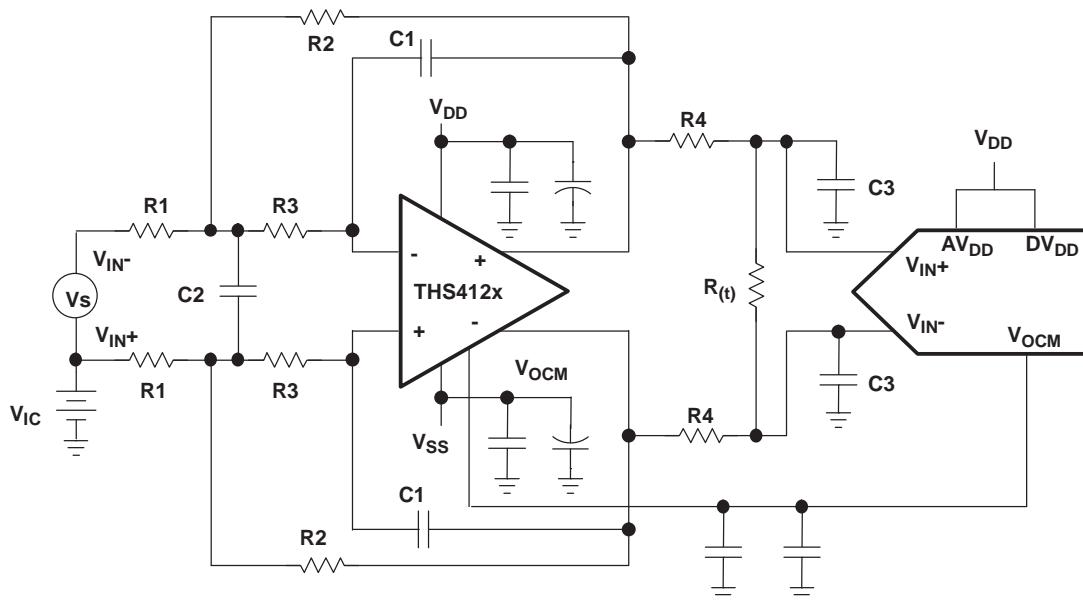


Figure 22. Antialias Filtering

APPLICATION INFORMATION (continued)

The transfer function for this filter circuit is:

$$H_d(f) = \left(\frac{K}{-\left(\frac{f}{FSF \times fc} \right)^2 + \frac{1}{Q} \frac{jf}{FSF \times fc} + 1} \right) \times \left(\frac{\frac{Rt}{2R4 + Rt}}{1 + \frac{j2\pi f R4 R t C3}{2R4 + Rt}} \right) \quad \text{Where } K = \frac{R2}{R1} \quad (3)$$

$$FSF \times fc = \frac{1}{2\pi\sqrt{2 \times R2 R3 C1 C2}} \quad \text{and} \quad Q = \frac{\sqrt{2 \times R2 R3 C1 C2}}{R3 C1 + R2 C1 + K R3 C1} \quad (4)$$

K sets the pass-band gain, fc is the cutoff frequency for the filter, FSF is a frequency scaling factor, and Q is the quality factor.

$$FSF = \sqrt{Re^2 + |Im|^2} \quad \text{and} \quad Q = \frac{\sqrt{Re^2 + |Im|^2}}{2Re} \quad (5)$$

Where Re is the real part, and Im is the imaginary part of the complex pole pair. Setting R2 = R, R3 = mR, C1 = C, and C2 = nC results in:

$$FSF \times fc = \frac{1}{2\pi R C \sqrt{2 \times m n}} \quad \text{and} \quad Q = \frac{\sqrt{2 \times m n}}{1 + m(1 + K)} \quad (6)$$

Start by determining the ratios, m and n, required for the gain and Q of the filter type being designed, then select C and calculate R for the desired fc.

PRINCIPLES OF OPERATION

THEORY OF OPERATION

The THS412x is a fully differential amplifier. Differential amplifiers are typically *differential in/single out*, whereas fully differential amplifiers are *differential in/differential out*.

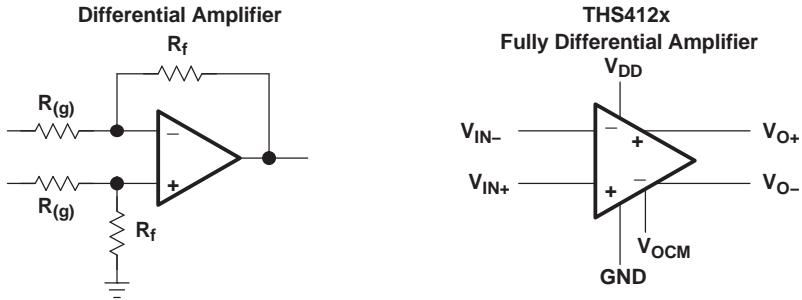


Figure 23. Differential Amplifier Versus a Fully Differential Amplifier

To understand the THS412x fully differential amplifiers, the definition for the pinouts of the amplifier are provided.

$$\text{Input voltage definition} \quad V_{ID} = (V_{I+}) - (V_{I-}) \quad V_{IC} = \frac{(V_{I+}) + (V_{I-})}{2} \quad (7)$$

$$\text{Output voltage definition} \quad V_{OD} = (V_{O+}) - (V_{O-}) \quad V_{OC} = \frac{(V_{O+}) + (V_{O-})}{2} \quad (8)$$

$$\text{Transfer function} \quad V_{OD} = V_{ID} \times A_{(f)} \quad (9)$$

$$\text{Output common-mode voltage} \quad V_{OC} \quad (10)$$

PRINCIPLES OF OPERATION (continued)

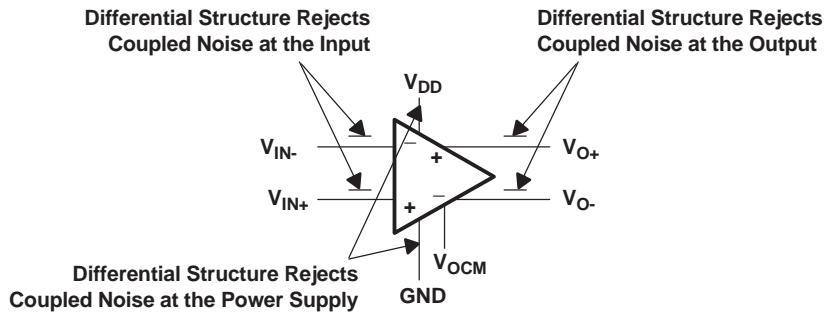


Figure 24. Definition of the Fully Differential Amplifier

The following schematics depict the differences between the operation of the THS412x, fully differential amplifier, in two different modes. Fully differential amplifiers can work with differential input or can be implemented as single in/differential out.

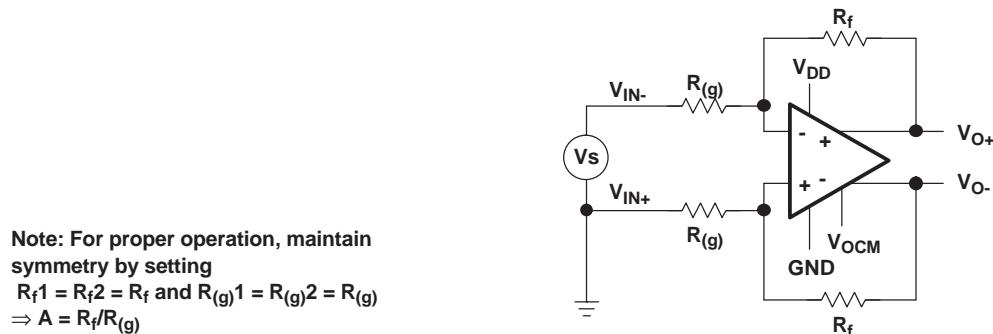


Figure 25. Amplifying Differential Signals

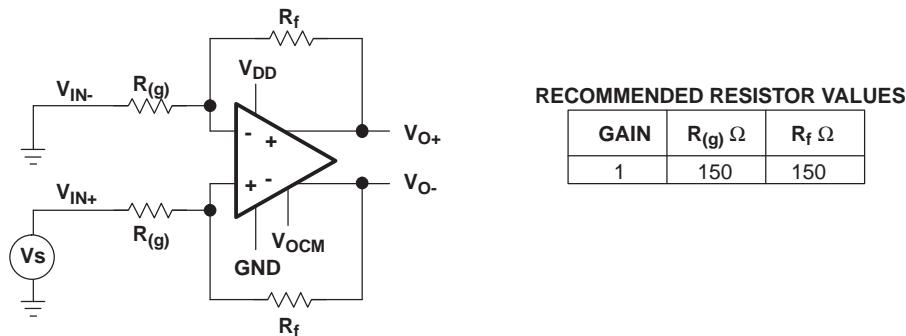


Figure 26. Single In With Differential Out

If each output is measured independently, each output is one-half of the input signal when gain is 1. The following equations express the transfer function for each output:

$$V_O = \frac{1}{2} V_I \quad (11)$$

The second output is equal and opposite in sign:

$$V_O = -\frac{1}{2} V_I \quad (12)$$

PRINCIPLES OF OPERATION (continued)

Fully differential amplifiers may be viewed as two inverting amplifiers. In this case, the equation of an inverting amplifier holds true for gain calculations. One advantage of fully differential amplifiers is that they offer twice as much dynamic range compared to single-ended amplifiers. For example, a 1-V_{PP} ADC can only support an input signal of 1 V_{PP}. If the output of the amplifier is 2 V_{PP}, then it is not practical to feed a 2-V_{PP} signal into the targeted ADC. Using a fully differential amplifier enables the user to break down the output into two 1-V_{PP} signals with opposite signs and feed them into the differential input nodes of the ADC. In practice, the designer has been able to feed a 2-V peak-to-peak signal into a 1-V differential ADC with the help of a fully differential amplifier. The final result indicates twice as much dynamic range. Figure 27 illustrates the increase in dynamic range. The gain factor should be considered in this scenario. The THS412x fully differential amplifier offers an improved CMRR and PSRR due to its symmetrical input and output. Furthermore, second harmonic distortion is improved. Second harmonics tend to cancel because of the symmetrical output.

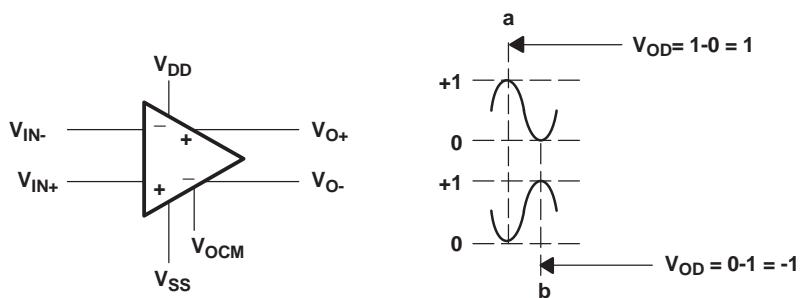


Figure 27. Fully Differential Amplifier With Two 1-V_{PP} Signals

CIRCUIT LAYOUT CONSIDERATIONS

To achieve the levels of high-frequency performance of the THS412x, follow proper printed-circuit board high frequency design techniques. A general set of guidelines is given below. In addition, a THS412x evaluation board is available to use as a guide for layout or for evaluating the device performance.

- **Ground planes** - It is highly recommended that a ground plane be used on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- **Proper power supply decoupling** - Use a 6.8- μ F tantalum capacitor in parallel with a 0.1- μ F ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1- μ F ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1- μ F capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inch (2.54 mm) between the device power terminals and the ceramic capacitors.
- **Sockets** - Sockets are not recommended for high-speed operational amplifiers. The additional lead inductance in the socket pins often lead to stability problems. Surface-mount packages soldered directly to the printed-circuit board is the best implementation.
- **Short trace runs/compact part placements** - Optimum high-frequency performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout should be made as compact as possible, thereby minimizing the length of all trace runs. Particular attention should be paid to the inverting input of the amplifier. Its length should be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- **Surface-mount passive components** - Using surface-mount passive components is recommended for high-frequency amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout thereby minimizing both stray inductance and capacitance. If leaded components are used, it is recommended that the lead lengths be kept as short as possible.

POWER-DOWN MODE

The THS4120 features a power-down pin (\overline{PD}) which lowers the quiescent current from 11 mA down to 120 μ A, ideal for reducing system power. The power-down pin of the amplifier must be pulled high via a 10-k Ω pullup resistor between the \overline{PD} pin and the positive supply (see Figure 28) in the absence of an applied voltage, putting

PRINCIPLES OF OPERATION (continued)

the amplifier in the power-on mode of operation. To turn off (disable) the amplifier in an effort to conserve power, the power-down pin can be driven towards the negative rail or ground. The threshold voltages for power-on and power-down are relative to the supply rails and given in the specification tables. Above the *Enable Threshold Voltage*, the device is on. Below the *Disable Threshold Voltage*, the device is off. Behavior in between these threshold voltages is not specified.

Note that this power-down functionality is just that; the amplifier consumes less power in power-down mode. The power-down mode is not intended to provide a high-impedance output. The power-down functionality is not intended to allow use as a 3-state bus driver. When in power-down mode, the impedance looking back into the output of the amplifier is dominated by the feedback and gain-setting resistors, but the output impedance of the device itself varies depending on the voltage applied to the outputs.

The time delays associated with turning the device on and off are specified as the time it takes for the amplifier to reach 50% of the nominal quiescent current. The enable time delay is in the order of microseconds due to the amplifier moving in and out of the linear mode of operation.

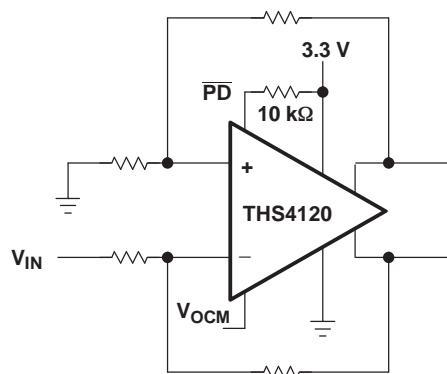


Figure 28.

Due to the similarity of the standard inverting amplifier configuration, the output impedance appears to be low while in the power-down state. This is because the feedback resistor (R_f) and the gain resistor (R_g) are still connected to the circuit. Therefore, a current path is allowed between the input of the amplifier and the output of the amplifier. An example of the closed-loop output impedance is shown in [Figure 29](#).

PRINCIPLES OF OPERATION (continued)

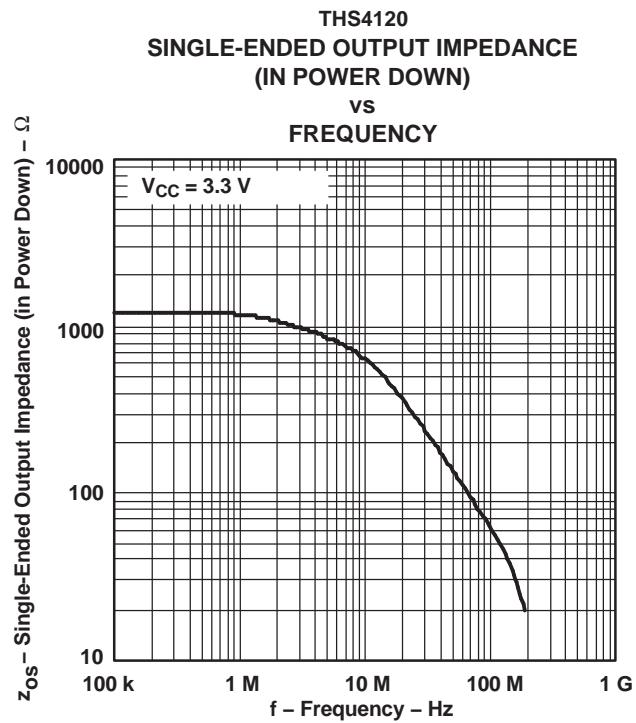


Figure 29.

PRINCIPLES OF OPERATION (continued)

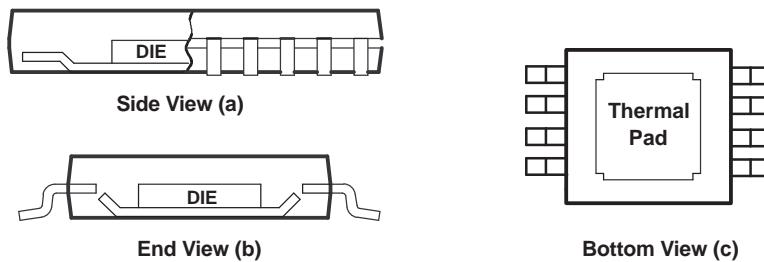
GENERAL PowerPAD DESIGN CONSIDERATIONS (APPLICABLE TO DIFFERENTIAL AMPLIFIER FAMILY)

The THS412x is available packaged in a thermally enhanced DGN package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe on which the die is mounted [see [Figure 30\(a\)](#) and [Figure 30\(b\)](#)]. This arrangement results in the leadframe being exposed as a thermal pad on the underside of the package [see [Figure 30\(c\)](#)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of the surface mount with the, heretofore, awkward mechanical methods of heatsinking.

More complete details of the PowerPAD installation process and thermal management techniques can be found in the Texas Instruments Technical Brief, *PowerPAD Thermally Enhanced Package (SLMA002)*. This document can be found at the TI Web site (www.ti.com) by searching on the key word PowerPAD. The document can also be ordered through your local TI sales office. Refer to literature number [SLMA002](#) when ordering.



A. The thermal pad is electrically isolated from all terminals in the package.

Figure 30. Views of Thermally Enhanced DGN Package

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4120CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4120C	Samples
THS4120CDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ARL	Samples
THS4120ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4120I	Samples
THS4120IDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ARN	Samples
THS4120IDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ARM	Samples
THS4120IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ARM	Samples
THS4120IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4120I	Samples
THS4121CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	4121C	Samples
THS4121CDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	0 to 70	ATO	Samples
THS4121CDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	0 to 70	ATO	Samples
THS4121ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	4121I	Samples
THS4121IDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	0 to 70	ASN	Samples
THS4121IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	0 to 70	ASN	Samples
THS4121IDGKRG4	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ASN	Samples
THS4121IDGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ASC	Samples
THS4121IDGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ASC	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

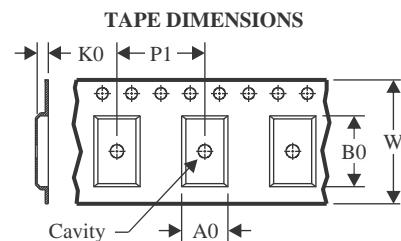
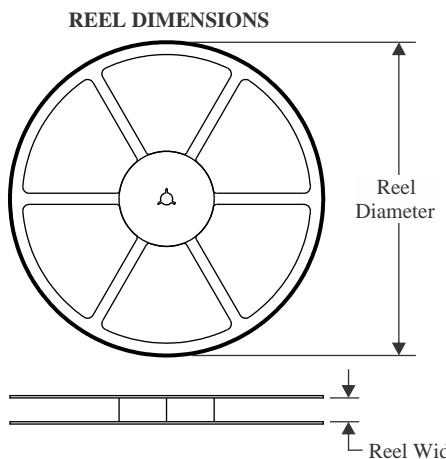
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

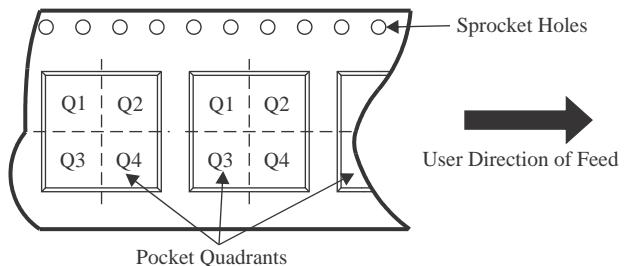
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


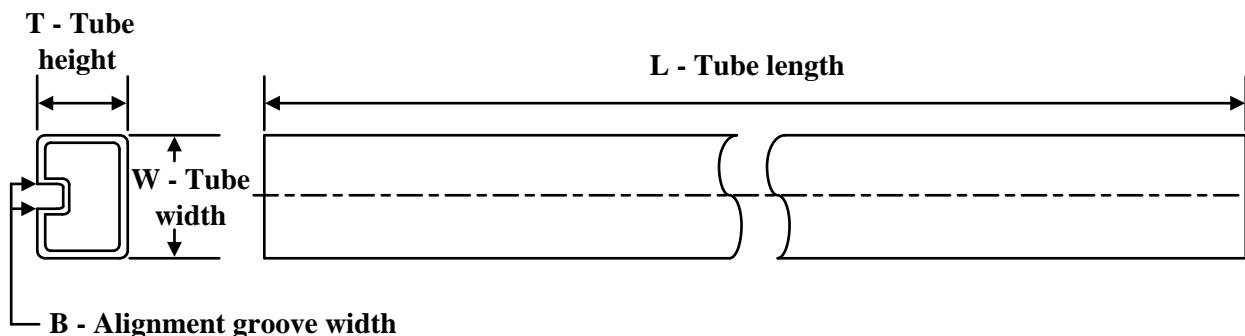
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS4120IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4120IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
THS4121CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4121IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4121IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
THS4121IDGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS4120IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4120IDR	SOIC	D	8	2500	350.0	350.0	43.0
THS4121CDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4121IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
THS4121IDGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
THS4121IDGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
THS4120CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4120ID	D	SOIC	8	75	505.46	6.76	3810	4
THS4121CD	D	SOIC	8	75	505.46	6.76	3810	4
THS4121CDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THS4121ID	D	SOIC	8	75	505.46	6.76	3810	4
THS4121IDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
THS4121IDGN	DGN	HVSSOP	8	80	330	6.55	500	2.88

GENERIC PACKAGE VIEW

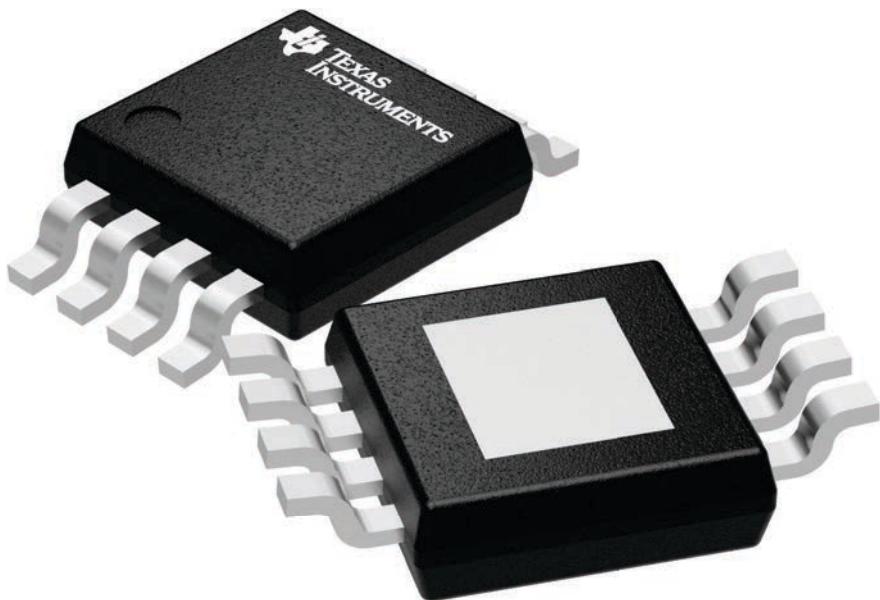
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

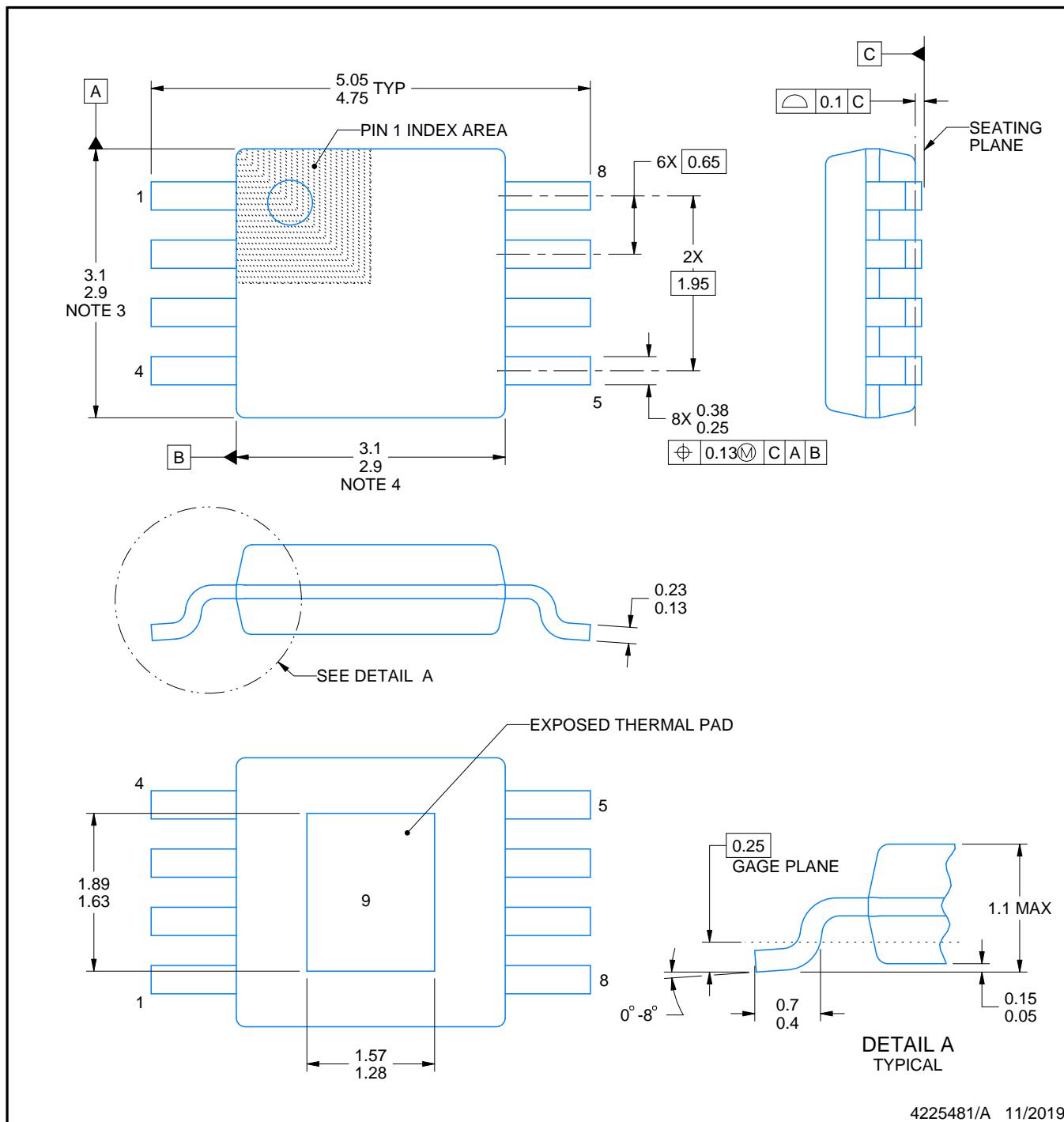
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

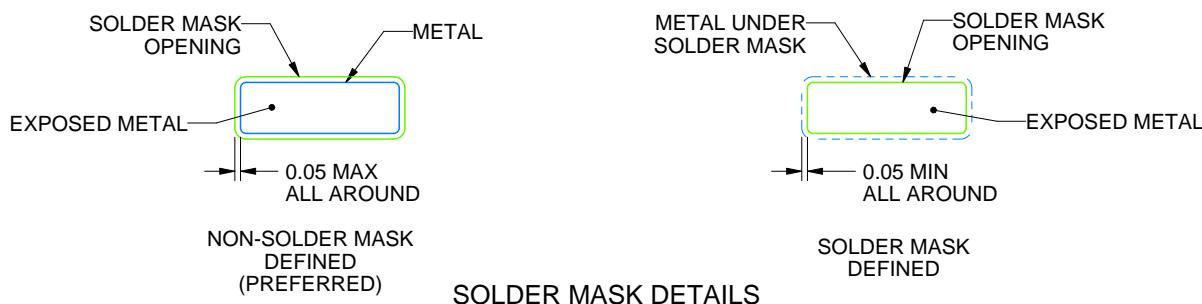
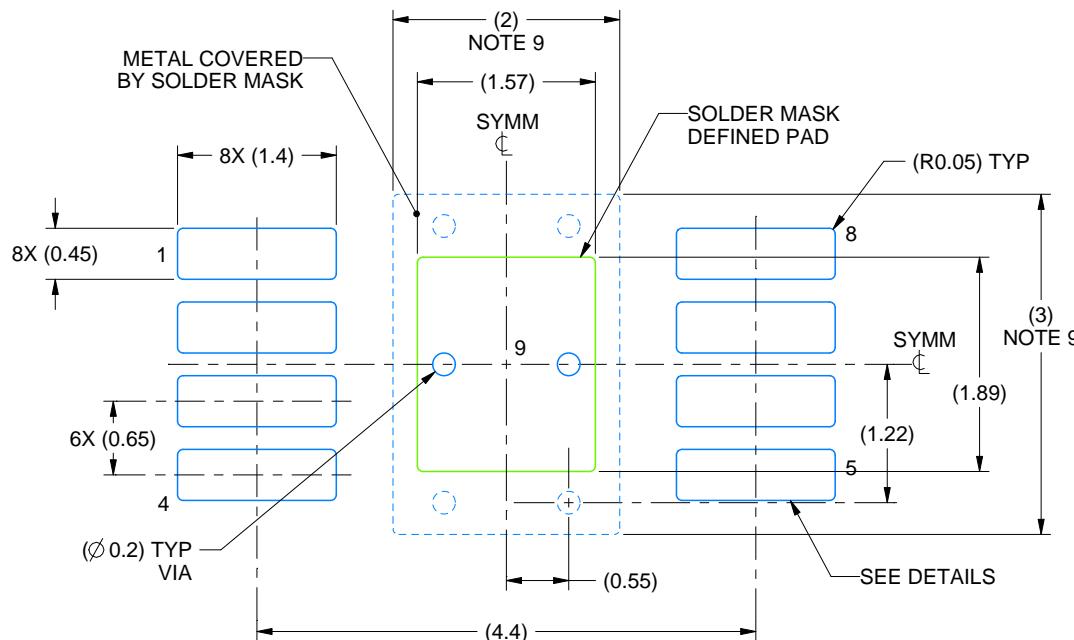
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4225481/A 11/2019

NOTES: (continued)

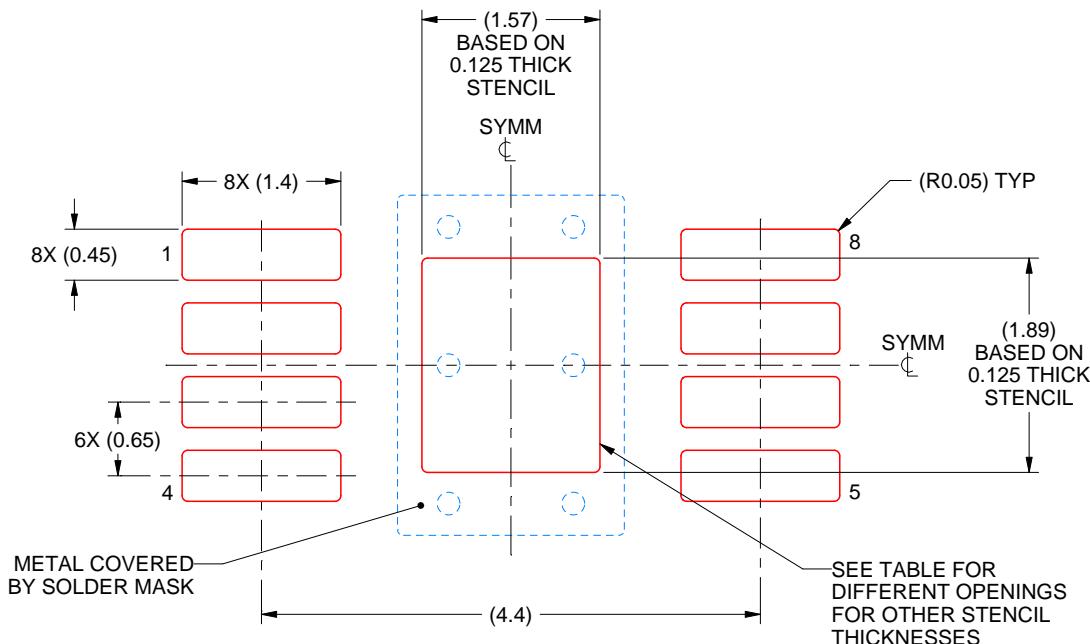
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008D

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

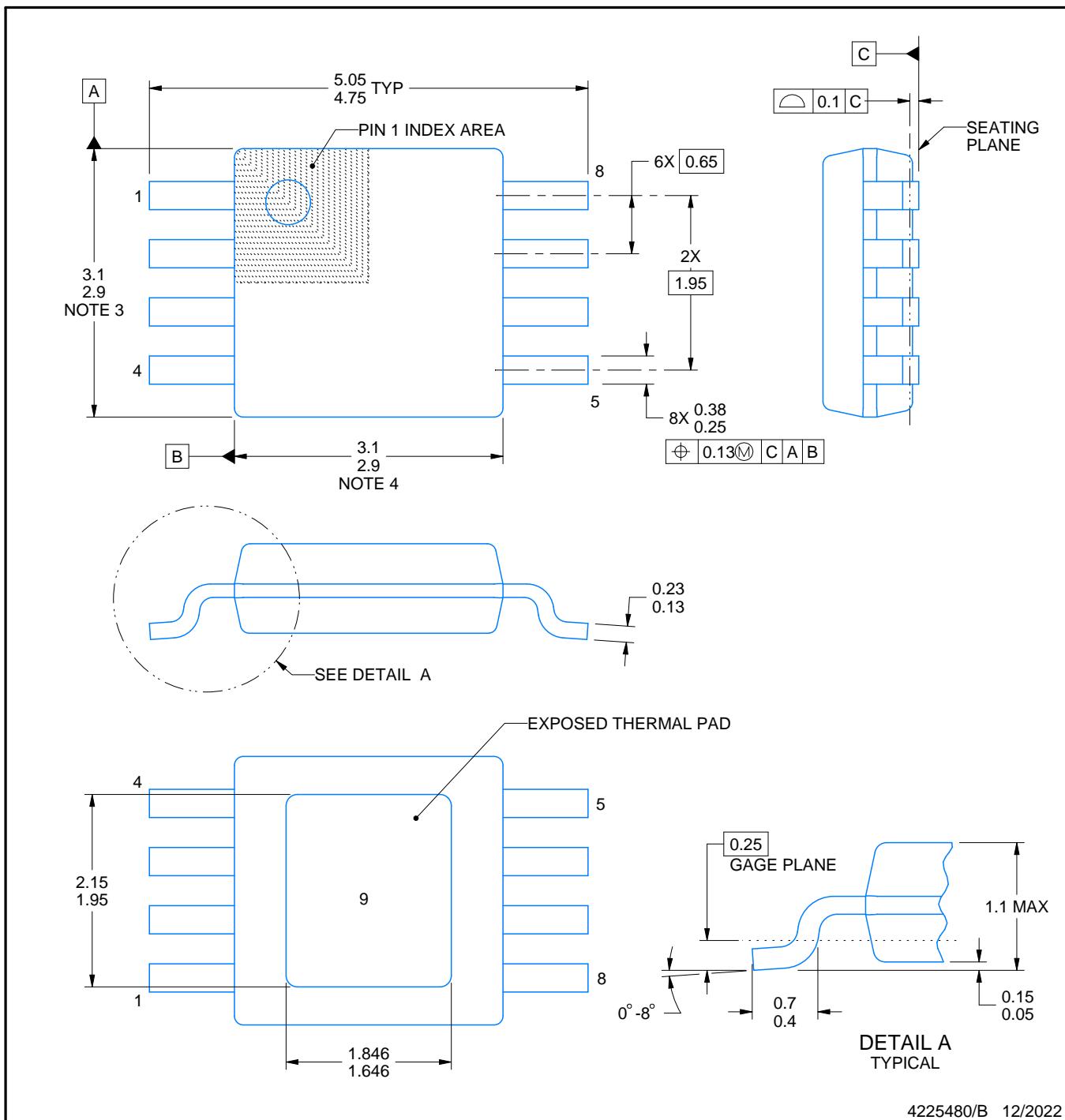
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4225480/B 12/2022

NOTES:

PowerPAD is a trademark of Texas Instruments.

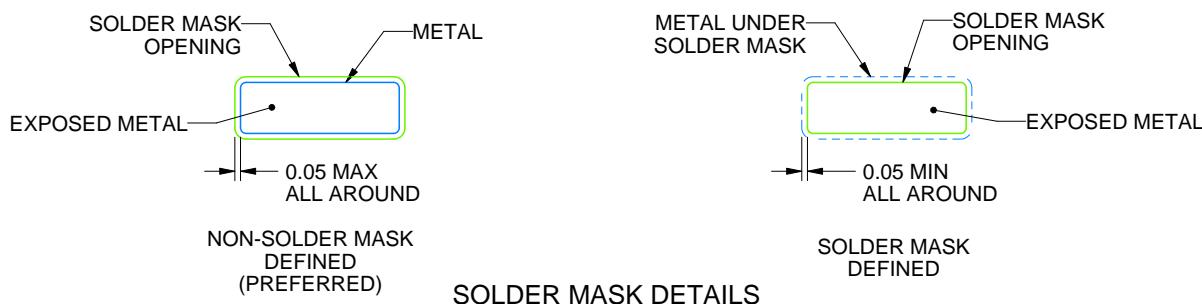
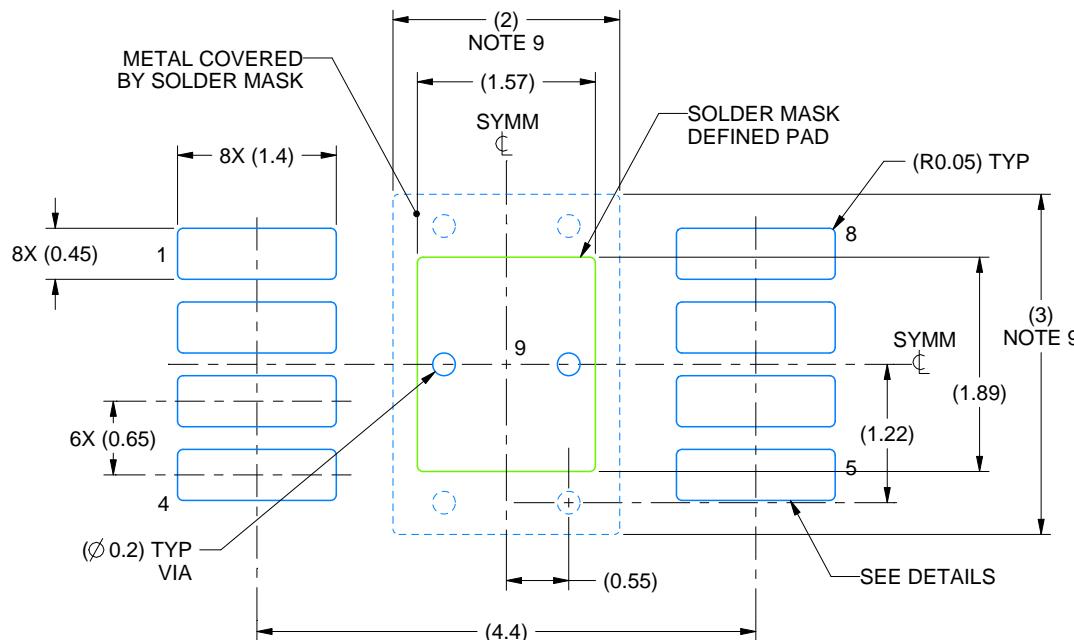
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4225480/B 12/2022

NOTES: (continued)

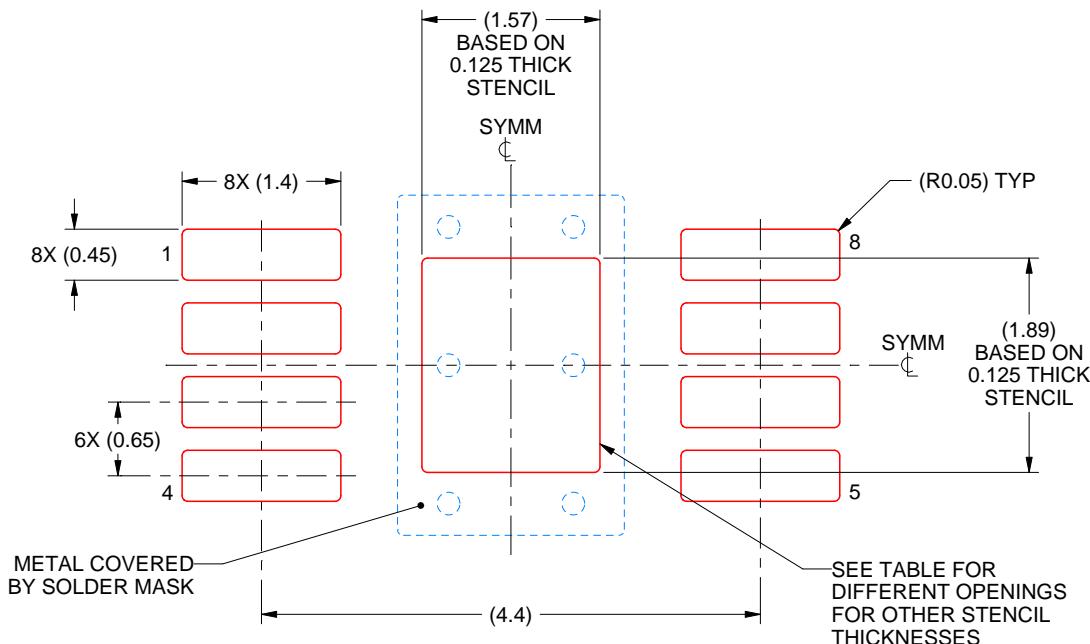
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008G

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/B 12/2022

NOTES: (continued)

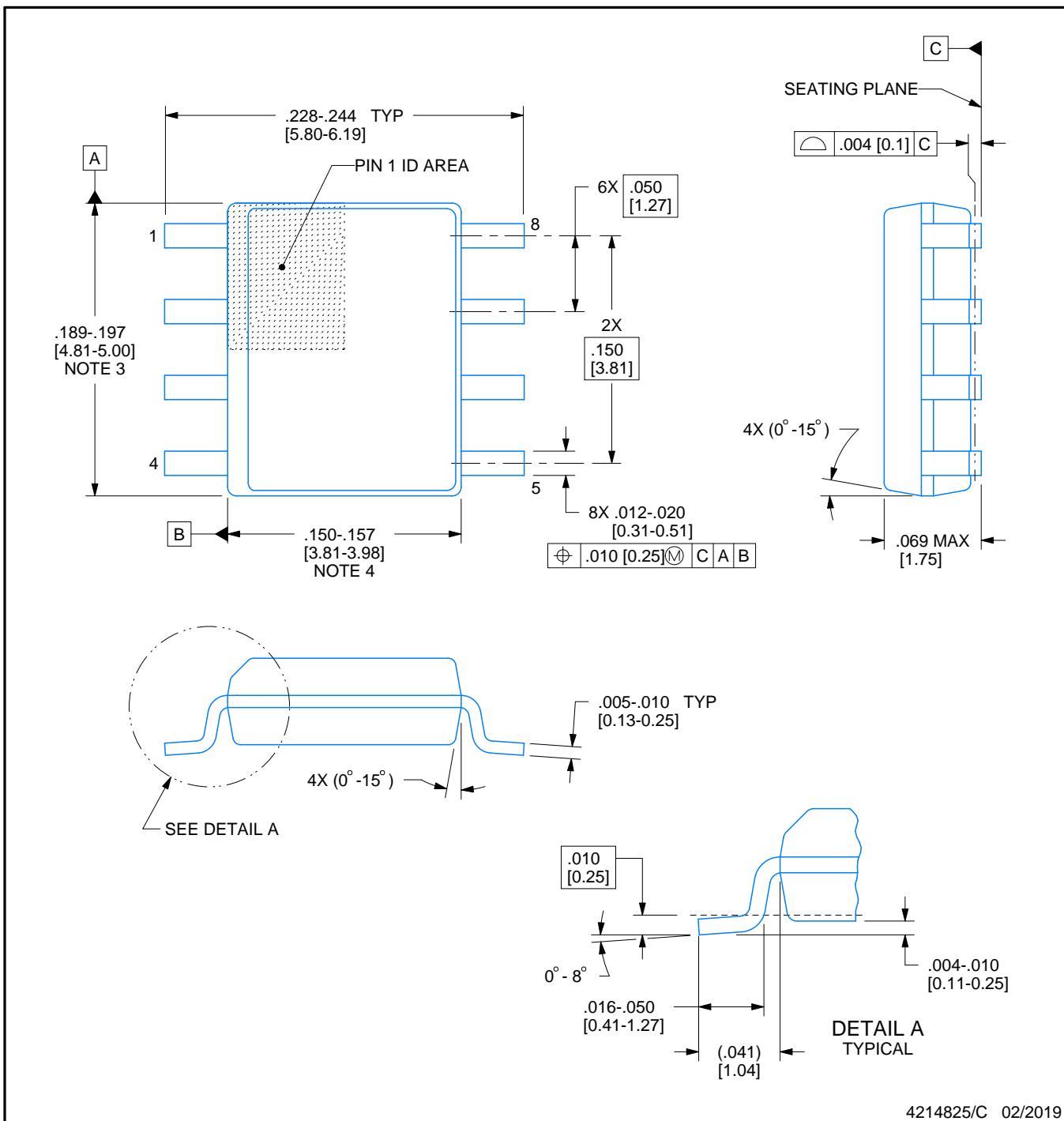
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

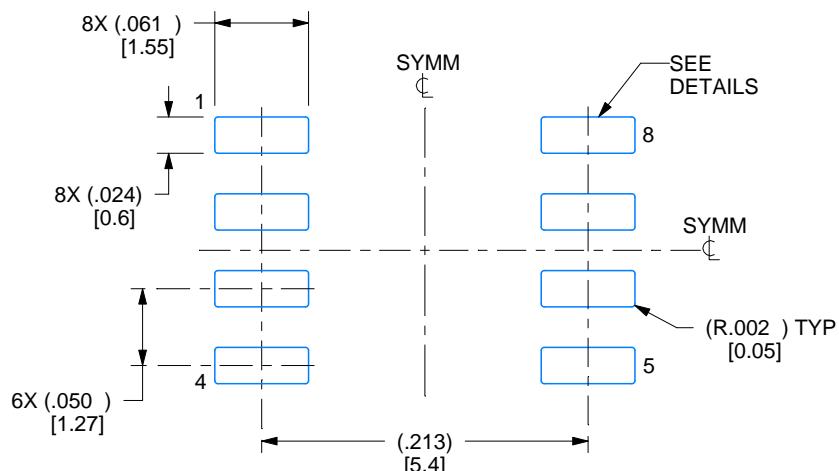
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

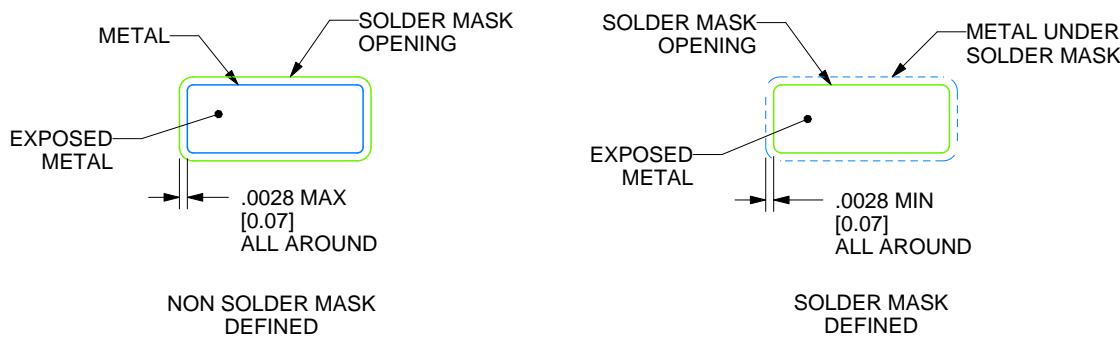
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

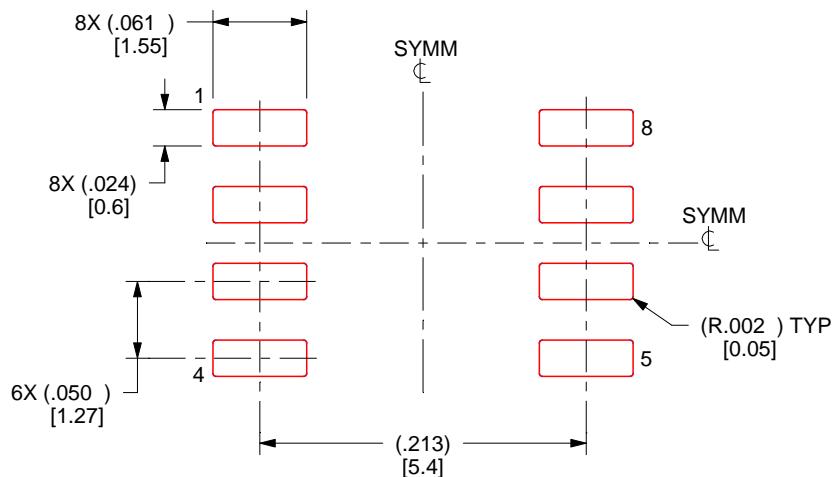
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

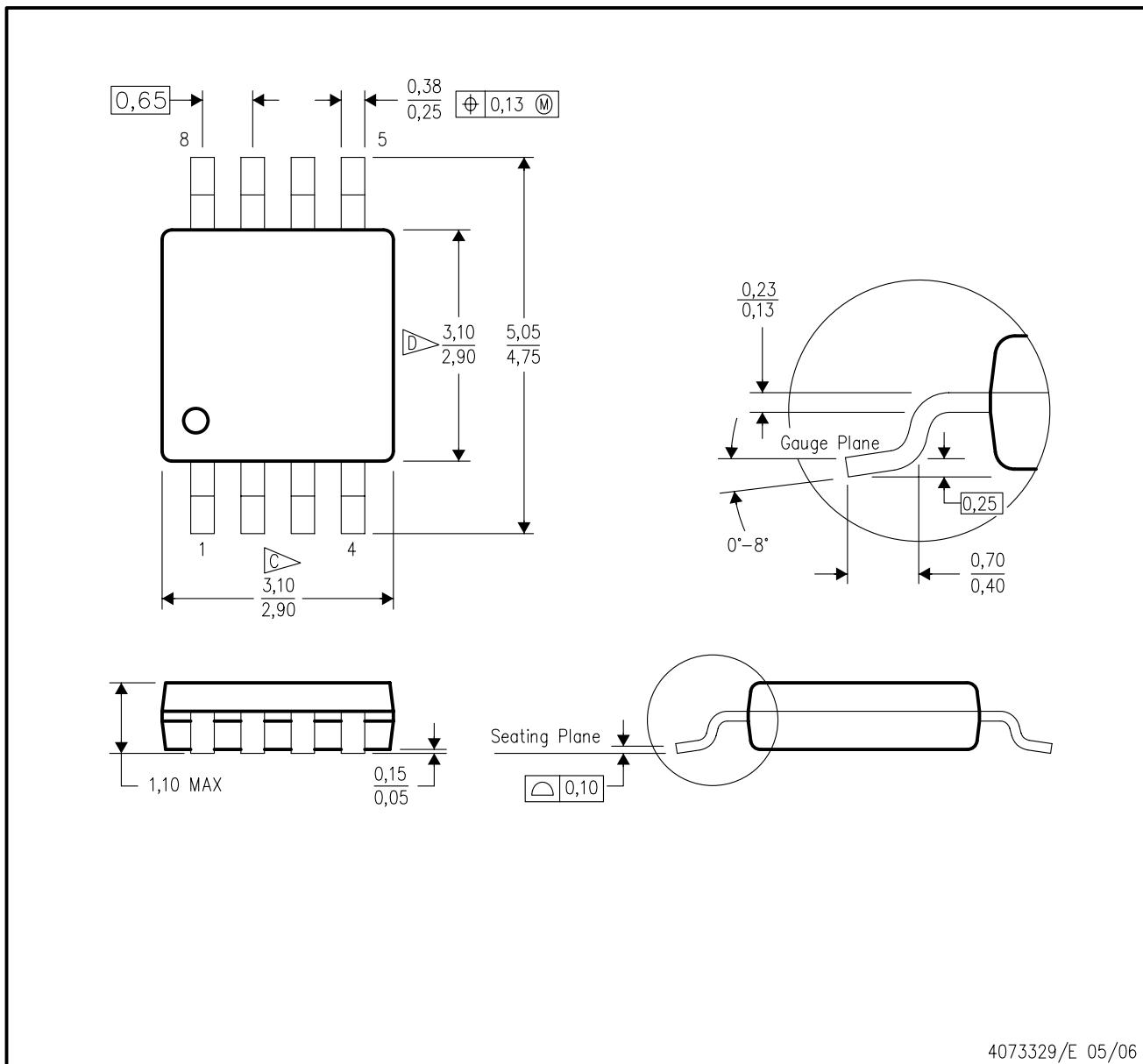
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

 C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 per end.

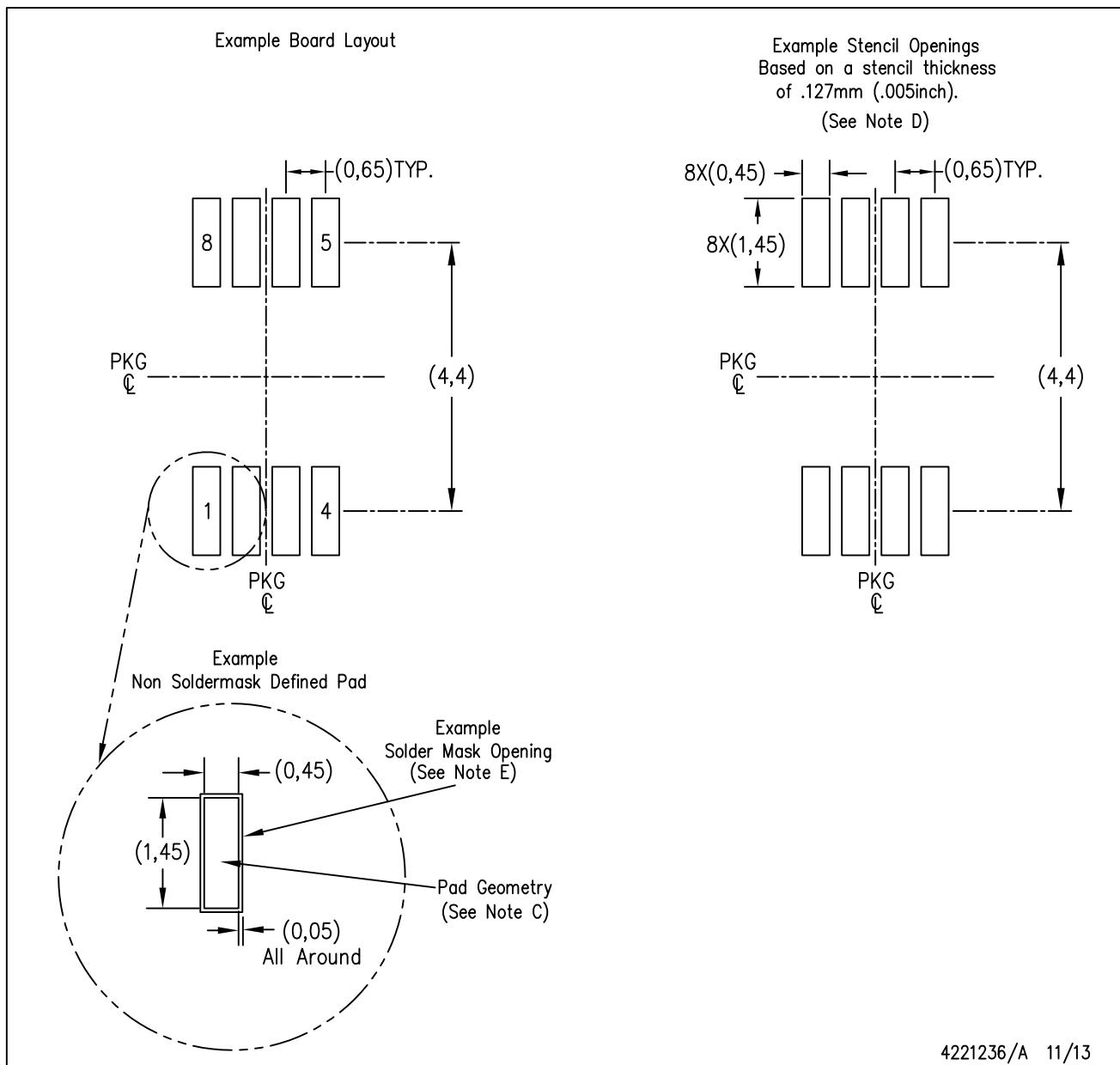
 D Body width does not include interlead flash. Interlead flash shall not exceed 0,50 per side.

E. Falls within JEDEC MO-187 variation AA, except interlead flash.

4073329/E 05/06

DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated