MP2249

1MHz, 6V, 3A, Low-Voltage Synchronous Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2249 is a 1MHz constant frequency, current mode, PWM step-down converter. The device integrates a main switch and a synchronous rectifier for high efficiency and eliminates the need for an external Schottky diode. It is ideal for powering portable equipment that runs from a single cell Lithium-Ion (Li+) battery.

The MP2249 can supply 3A of load current from a 2.5V to 6V input voltage. It can run at 100% duty cycle for low dropout applications. The MP2249 provides internal soft-start control to reduce rush current and output discharge function to control discharging of the output capacitor.

The MP2249 is available in small 3mmx3mm TQFN10 or SOIC8E package.

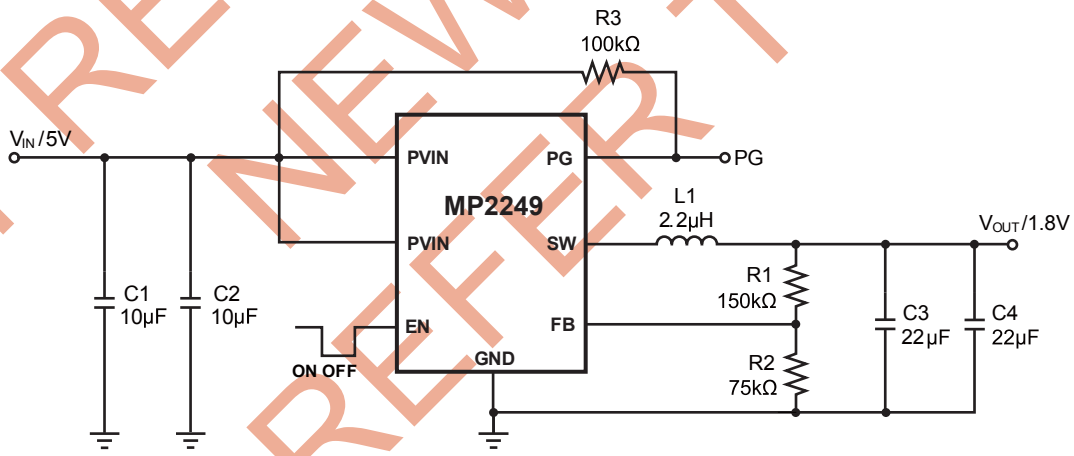
FEATURES

- High Efficiency: Up to 90%
- Power Save Mode at Light Load
- 1MHz Constant Switching Frequency
- Up to 4.5A PeakCurrent
- 2.5V to 6V Input Voltage Range
- Output Adjustable from 0.6V to VIN
- 100% Duty Cycle in Dropout
- Output Discharge Function
- Internal Soft-Start Control
- Power Good Indicator
- Short Circuit Protection
- Thermal Fault Protection
- Available in 3mmx3mm TQFN10 or SOIC8E Package

APPLICATIONS

- Cellular and Smart Phones
- Microprocessors and DSP Core Supplies
- PDAs
- MP3 Players
- Digital Still and Video Cameras
- Portable Instruments

TYPICAL APPLICATION

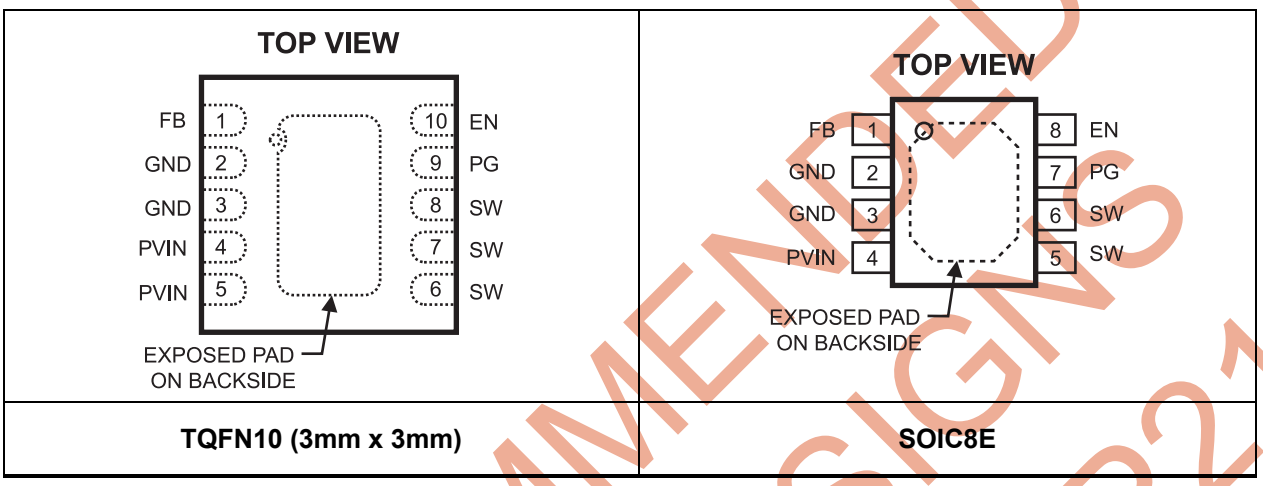


ORDERING INFORMATION

Part Number	Package	Top Marking	Free Air Temperature (T_A)
MP2249DN	SOIC8E	MP2249	-40°C to +85°C
MP2249DQT *	TQFN10 (3mm x 3mm)	AAVY	

* For Tape and Reel, add suffix -Z (e.g. MP2249DQT–Z).
For RoHS Compliant Packaging, add suffix - LF (e.g. MP2249DQT–LF–Z);

PACKAGE REFERENCE



TQFN10 (3mm x 3mm) | SOIC8E

ABSOLUTE MAXIMUM RATINGS (1)

PVIN to GND ..... -0.3V to +6.5V
SW to GND ..... -0.3V to V_{IN} +0.3V
FB, EN & PG to GND ..... -0.3V to +6.5V
Junction Temperature ..... +150°C
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC8E 2.5W
TQFN10 (3mmx3mm) 2.5W
Lead Temperature ..... +260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} ..... 2.5V to 6V
Output Voltage V_{OUT} ..... 0.6V to 6V
Operating Junct. Temp. ..... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}
SOIC8E	50	10... °C/W
TQFN10 (3mmx3mm)	50	12... °C/W

Notes:
1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature. T_J(MAX) the junction-to-ambient thermal resistance θ_{JA} and the ambient temperature T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_D(MAX)=(T_J(MAX)-T_A)/\ \theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.6V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current	I_Q	V_{EN} = V_{IN}, V_{FB} = 0.51V		480	600	μA
Shutdown Current		V_{EN} = 0V, V_{IN} = 6V		0.01	1	μA
IN Under Voltage Lockout (UVLO) Threshold		Rising Edge	2.15	2.3	2.45	V
IN Under Voltage Lockout Hysteresis				210		mV
Soft-Start Time				1		ms
Discharge MOSFET On Resistance				100		Ω
Regulated FB Voltage	V_{FB}	T_A = +25°C	0.594	0.600	0.606	V
		-40°C ≤ T_A ≤ +85°C	0.588	0.600	0.612	
FB Input Bias Current		V_{FB} = 0.65V	-50	0.5	+50	nA
PFET On Resistance (5)		I_{SW} = 100mA		92		mΩ
NFET On Resistance (5)		I_{SW} = -100mA		72		mΩ
SW Leakage Current		V_{EN} = 0V,V_{IN} = 6V, V_{SW} = 0V or 6V	-1		+1	μA
PFET Current Limit (5)	I_{LIMIT}	Duty Cycle = 100%, Current Pulse Width < 1ms		4.5		A
Oscillator Frequency	f_{SW}			1		MHz
Minimum On Time (5)	t_{ON}			100		ns
Thermal Shutdown Trip Threshold (5)				145		°C
EN Turn-on Trip Threshold		-40°C ≤ T_A ≤ +85°C			1.8	V
EN Turn-off Trip Threshold		-40°C ≤ T_A ≤ +85°C	0.4			V
EN-pull down resistor			360	450	540	kΩ
Latch Off Under Voltage (UV) Threshold				67%		V_{FB}
PG Upper Trip Threshold				90%		V_{FB}
PG Lower Trip Threshold				85%		V_{FB}
PG Output Low Voltage		I_{SINK}=1mA			0.3	V

Notes:

5) 100% production test at +25°C. Typical and temperature specifications are guaranteed by design and characterization.

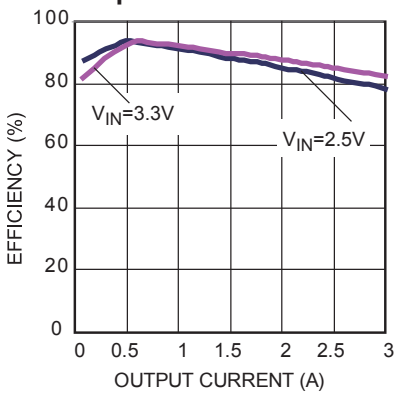
PIN FUNCTIONS

Pin #		Name	Description
TQFN10	SOIC8E		
6, 7, 8	5, 6	SW	Power Switch Output. Inductor connection to drains of the internal PFET and NFET switches.
9	7	PG	Power-good indicator. PG is pulled low when output is outside the window of regulation or the device enters shutdown.
10	8	EN	Regulator Enable Control Input. Drive EN above 1.8V to turn on the MP2249. Drive EN below 0.4V to turn it off. EN is pulled to GND with a 450kΩ internal resistor.
1	1	FB	Feedback Input. Connect FB to the center point of the external resistor divider. The feedback threshold voltage is 0.6V.
2, 3 Exposed Pad	2, 3 Exposed Pad	GND	Ground. Connect Exposed Pad to ground plane for optimal thermal performance.
4, 5	4	PVIN	Power Stage Supply Input. Bypass to GND with a 2.2µF or bigger ceramic capacitor.

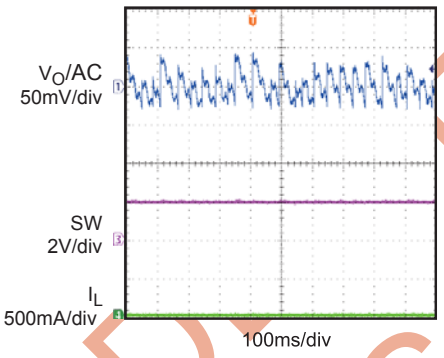
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5V, EN = 5V, V_O = 1.8V, L1 = 2.2µH, and T_A = +25°C, unless otherwise noted.

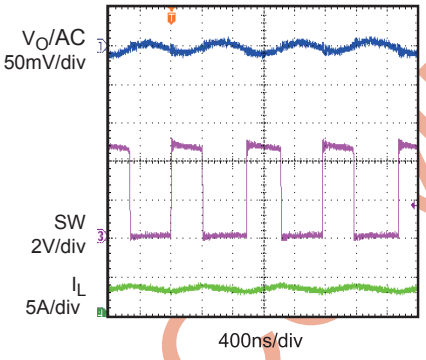
Efficiency vs. Output Current



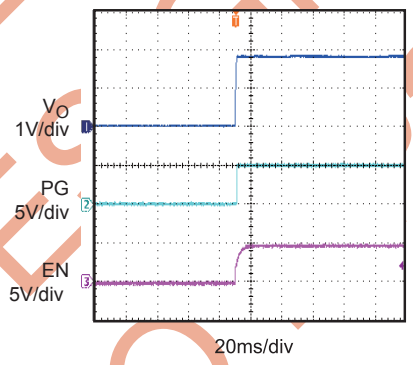
Steady State Operation
I_O=0A



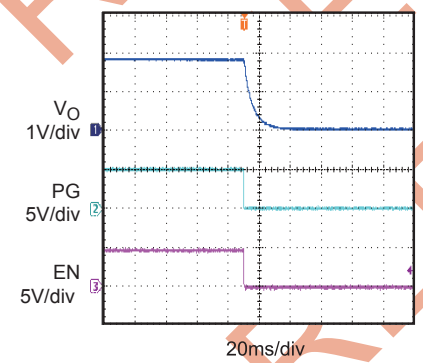
Steady State Operation
I_O=3A



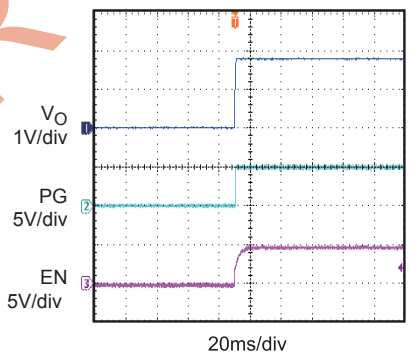
Start-up through EN
I_O=0A



Shut-down through EN
I_O=0A



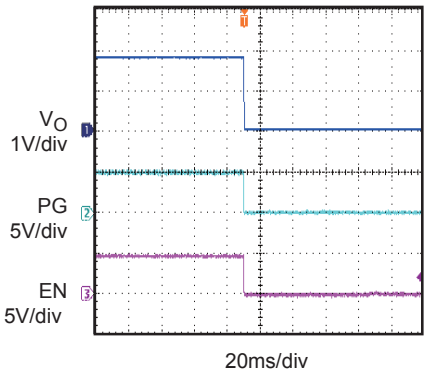
Start-up through EN
I_O=3A



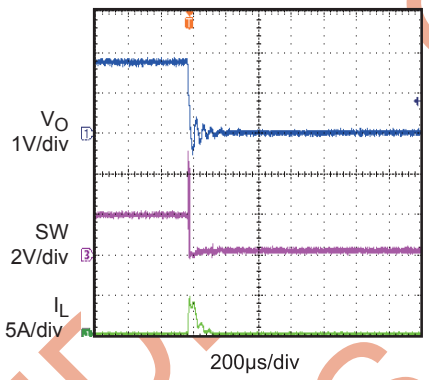
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 5V, EN = 5V, V_O = 1.8V, L1 = 2.2µH, and T_A = +25°C, unless otherwise noted.

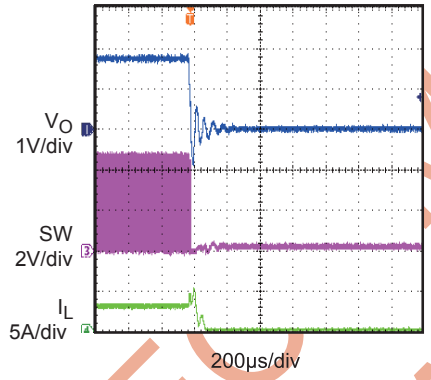
Shut-down through EN
I_O=3A



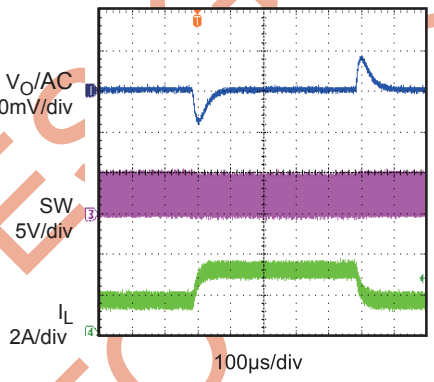
Short Cuit Protection
I_O=0A to short



Short Cuit Protection
I_O=3A to short



Load Transient
I_O=1.5A to 3A



FUNCTION BLOCK DIAGRAM

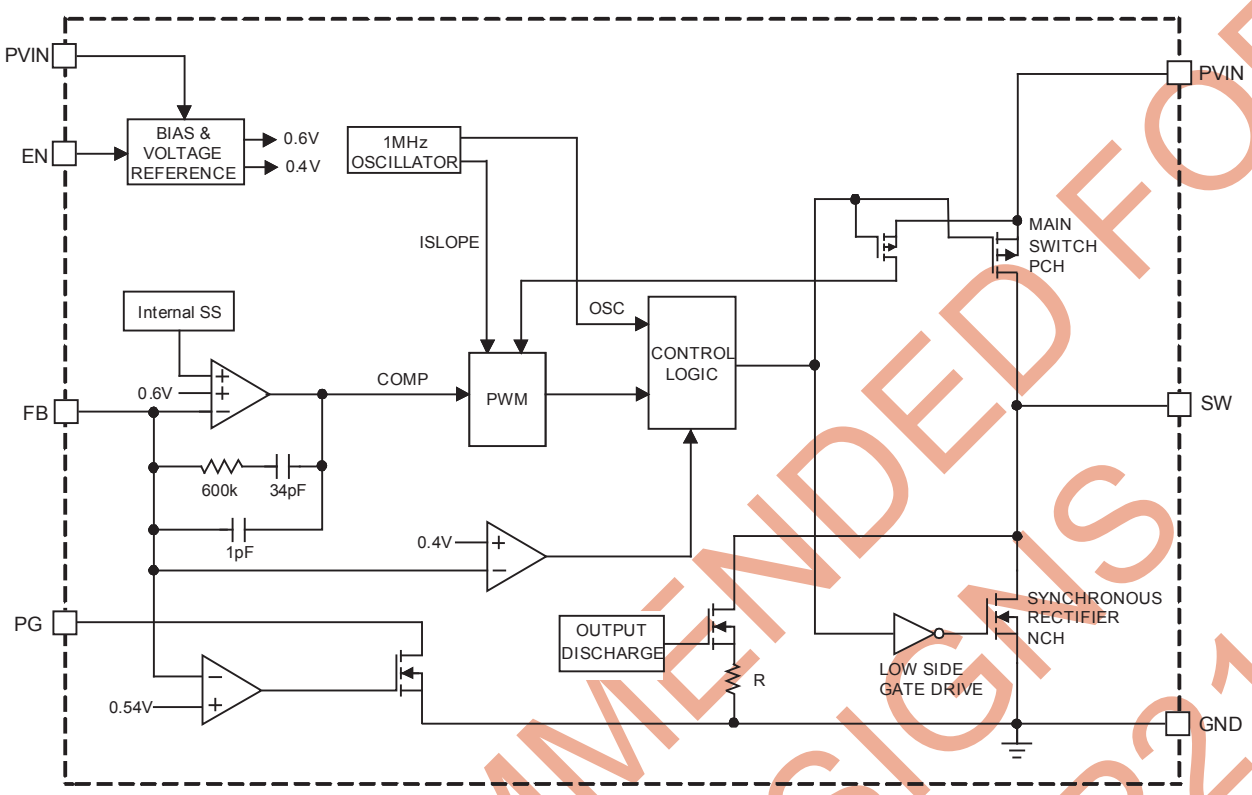


Figure 1—Function Block Diagram

OPERATION

The MP2249 is a constant frequency current mode PWM step-down converter. The MP2249 is optimized for low voltage, Li-Ion battery powered applications where high efficiency and small size are critical. The MP2249 uses an external resistor divider to set the output voltage from 0.6V to 6V. The device integrates both a main switch and synchronous rectifier, which provides high efficiency and eliminates an external Schottky diode. The MP2249 can achieve 100% duty cycle. The duty cycle D of a step-down converter is defined as:

$$D = T_{ON} \times f_{OSC} \times 100\% \approx \frac{V_{OUT}}{V_{IN}} \times 100\%$$

Where T_{ON} is the main switch on time, f_{OSC} is the oscillator frequency (1MHz), V_{OUT} is the output voltage and VIN is the input voltage

Current Mode PWM Control

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limit for superior load and line response and protection of the internal main switch and synchronous rectifier. The MP2249 switches at a constant frequency (1MHz) and regulates the output voltage. During each cycle the PWM comparator modulates the power transferred to the load by changing the inductor peak current based on the feedback error voltage. During normal operation, the main switch is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is above the error voltage. When the main switch is off, the synchronous rectifier will be turned on immediately.

Power Save Mode Operation

The MP2249 enters asynchronous mode as soon as current of LS MOS goes below zero. When the load is light enough and comp voltage is lower than the set value, the part goes into power skipping mode. This mode improves efficiency at light load condition.

Dropout Operation

The MP2249 allows the main switch to remain on for more than one switching cycle and increases the duty cycle while the input voltage is dropping close to the output voltage. When the duty cycle reaches 100%, the main switch is held on continuously to deliver current to the output up to the switch's current limit. The output voltage then is the input voltage minus the voltage drop across the main switch and the inductor.

Over-Current-Protection and Latchoff

The MP2249 provides cycle-by-cycle over current limit when inductor current peak value exceeds the current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 33% below the reference. Once the UV is triggered, the MP2249 enters latched off mode.

This protection mode is especially useful when the output is dead-short to ground. The MP2249 exits the latch off mode once the EN or input power is recycled. This operation mode will be masked off for the soft start stage.

Maximum Load current

The MP2249 can operate down to 2.5V input voltage. However, the maximum load current decreases at lower input due to large IR drop across the main switch and synchronous rectifier. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%. Conversely the current limit increases as the duty cycle decreases.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 1.2V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control.

Output Discharge Function

When the device is disabled, the part goes into output discharge mode automatically and its internal discharge MOSFET provides a resistive discharge path for the output capacitor. This function is only suitable for discharge output capacitor for the limited time. If the part is used in a pre-bias application, the external power supply providing the pre-bias should supply larger current than the discharge MOSFET sinks.

PG Indicator

MP2249 provides an open-drain PG output that goes high after output level reaches regulation after startup. PG is pulled low immediately if the output goes out of regulation level or when device enters shutdown.

APPLICATION INFORMATION

Output Voltage Setting

The external resistor divider sets the output voltage (see Page 1, Schematic Diagram). The feedback resistor R1 also set the feedback loop bandwidth with the internal compensation.

The feedback loop bandwidth (f_C) is no higher than 1/10th of switching frequency of MP2249. In the case of output ceramic capacitor as C_O, it is usually set in the range of 50kHz and 100kHz for optimal transient performance and good phase margin. If an electrolytic capacitor is used, the loop bandwidth is no higher than 1/4 of the ESR zero frequency (f_{ESR}). f_{ESR} is given by:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_O}$$

For example, choose f_C=80kHz with a ceramic capacitor, C_O=47µF, R1 is estimated to be 150kΩ. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1}$$

Table 1—Resistor Selection vs. Output Voltage Setting

V_{OUT}	R1	R2	L	C_{OUT} (Ceramic)
1.2V	150kΩ	150kΩ	1.5µH-2.2µH	22µF x 2
1.5V	150kΩ	100kΩ	1.5µH-2.2µH	22µF x 2
1.8V	150kΩ	75kΩ	1.5µH-2.2µH	22µF x 2
2.5V	150kΩ	47.5kΩ	1.5µH-2.2µH	22µF x 2
3.3V	150kΩ	33.2kΩ	1.5µH-2.2µH	22µF x 2

Inductor Selection

A 1.5µH to 2.2µH inductor with DC current rating at least 25% higher than the maximum load current is recommended for most applications. For best efficiency, the inductor DC resistance shall be <20mΩ. See Table 2 for recommended inductors and Vendors. For most designs, the inductance value can be derived from the following equation:

$$L = \frac{V_{OUT} x (V_{IN} - V_{OUT})}{V_{IN} x \Delta I_L x f_{OSC}}$$

where ΔI_L is Inductor Ripple Current. Choose inductor ripple current approximately 30% of the maximum load current 3A.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Table 2—Suggested Surface Mount Inductors

Vendor	Part Number	L (µH)	DCR (mΩ)	SC (A)	L x W x H (mm^3)
WURTH					
	744777002	2.2	13	6	7.3×7.3×4.5
	744310200	2	14.2	6.5	7×6.9×3
TDK					
	RLF7030T-1R5N6R1-T	1.5	8	6.5	7.8×6.8×3.2

Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and the switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input source. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 47µF capacitor is sufficient.

Output Capacitor Selection

The output capacitor keeps output voltage ripple small and ensures a stable regulation loop. The output capacitor impedance shall be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended. If an electrolytic capacitor is used, pay attention to output ripple voltage, extra heating, and the selection of feedback resistor R1 (refer to "Output Voltage Setting" section) due to the large ESR of electrolytic capacitor. The output ripple ΔV_{OUT} is approximately:

$$\Delta V_{OUT} \leq \frac{V_{OUT} x (V_{IN} - V_{OUT})}{V_{IN} x f_{OSC} x L} x (ESR + \frac{1}{8 x f_{OSC} x C_O})$$

TYPICAL APPLICATION CIRCUIT

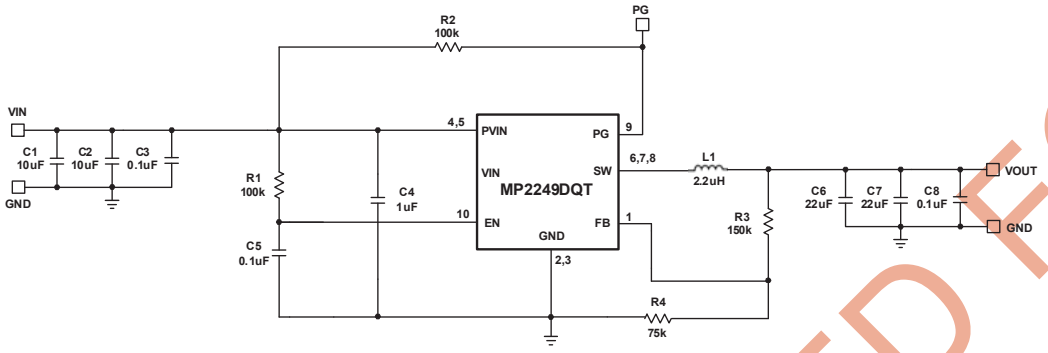


Figure 2—Typical application circuit of MP2249DQT

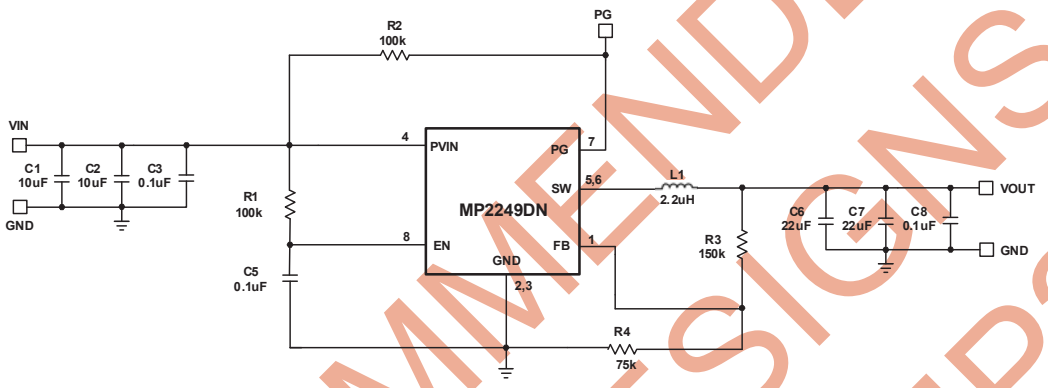
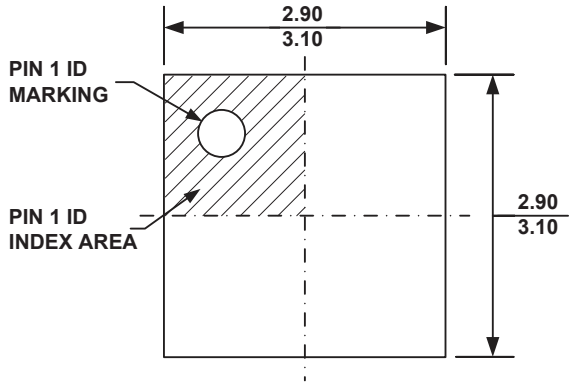


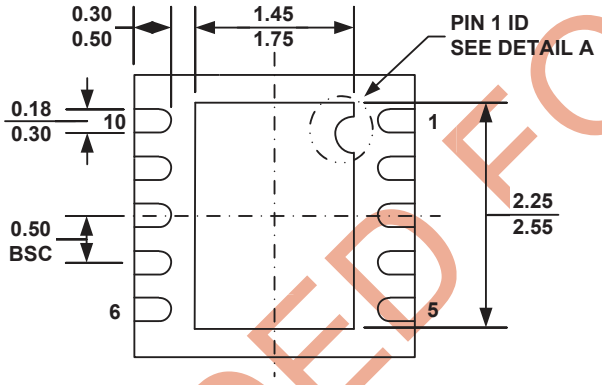
Figure 3—Typical application circuit of MP2249DN

PACKAGE INFORMATION

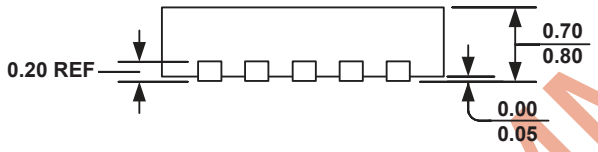
TQFN10 (3mm x 3mm)



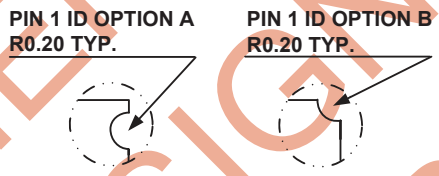
TOP VIEW



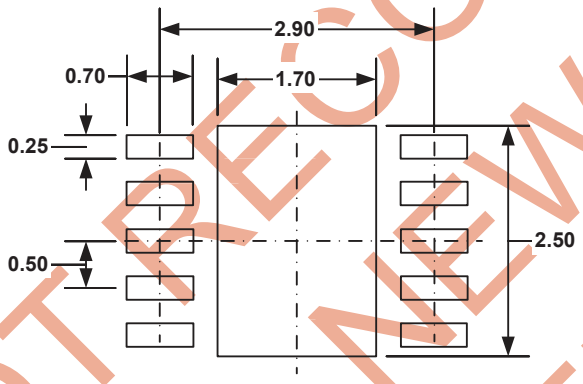
BOTTOM VIEW



SIDE VIEW



DETAIL A

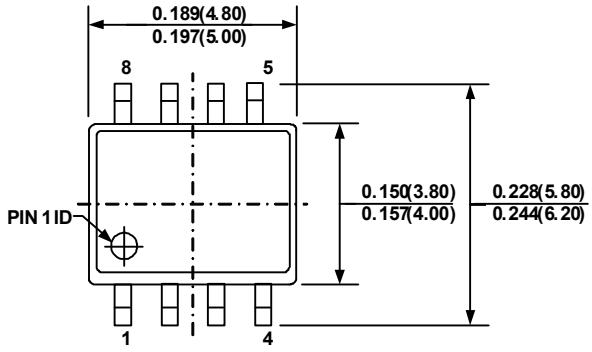


RECOMMENDED LAND PATTERN

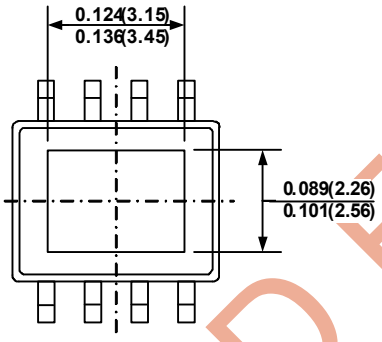
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.

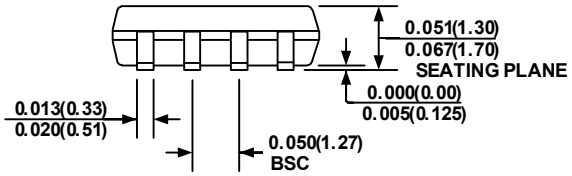
SOIC8E (exposed pad)



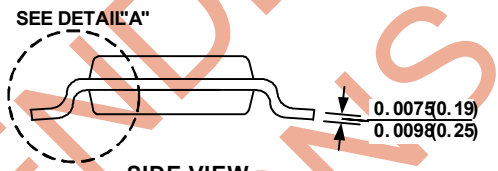
TOP VIEW



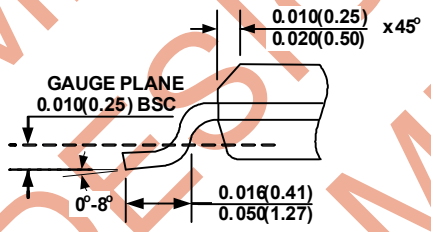
BOTTOM VIEW



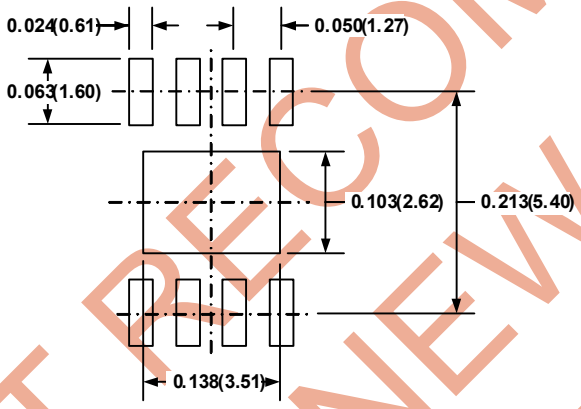
FRONT VIEW



SIDE VIEW



DETAIL "A"



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS
4) LEAD COPLANARITY (Y) BOTTOM OF LEADS AFTER FORMING SHALL BE 0.004" INCHES MAX
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA
6) DRAWING IS NOT TO SCALE