

NCV8505 Series

LDO Linear Regulators - Micropower, ENABLE, DELAY, RESET

400 mA

The NCV8505 is a family of precision micropower voltage regulators. Their output current capability is 400 mA. The family has output voltage options for Adjustable, 2.5 V, 3.3 V and 5.0 V.

The output voltage is accurate within $\pm 2.0\%$ with a maximum dropout voltage of 0.6 V at 400 mA. Low quiescent current is a feature drawing less than 1.0 μA with $\text{ENABLE} = 0\text{ V}$. With $\text{ENABLE} = 5.0\text{ V}$, the part only draws 200 μA with 100 μA load. This part is ideal for any and all battery operated microprocessor equipment.

Microprocessor control logic includes an active $\overline{\text{RESET}}$ (with DELAY).

The active $\overline{\text{RESET}}$ circuit operates correctly at an output voltage as low as 1.0 V. The $\overline{\text{RESET}}$ function is activated during the power up sequence or during normal operation if the output voltage drops below the regulation limits.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments. The device has also been optimized for EMC conditions.

Features

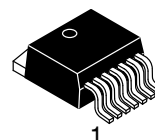
- Output Voltage Options: Adjustable, 2.5 V, 3.3 V, 5.0 V
- $\pm 2.0\%$ Output
- Low $< 1.0\text{ }\mu\text{A}$ Sleep Current
- Low 200 μA Quiescent Current
- Fixed or Adjustable Output Voltage
- Active $\overline{\text{RESET}}$
- ENABLE
- 400 mA Output Current Capability
- Fault Protection
 - ♦ +60 V Peak Transient Voltage
 - ♦ -15 V Reverse Voltage
 - ♦ Short Circuit
 - ♦ Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- AEC Qualified
- PPAP Capable
- These are Pb-Free Devices



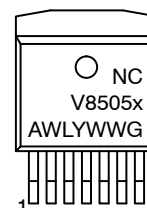
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MARKING DIAGRAM



**D²PAK-7
DPS SUFFIX
CASE 936AB**



- x = Voltage Ratings as Indicated Below:
- A = Adjustable
 - 2 = 2.5 V
 - 3 = 3.3 V
 - 5 = 5.0 V
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

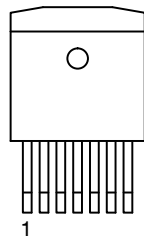
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

NCV8505 Series

PIN CONNECTIONS

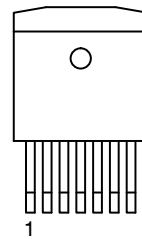
ADJUSTABLE OUTPUT



Tab = GND
Lead

1. DELAY
2. ENABLE
3. RESET
4. GND
5. V_{ADJ}
6. V_{OUT}
7. V_{IN}

FIXED OUTPUT



Tab = GND
Lead

1. DELAY
2. ENABLE
3. RESET
4. GND
5. SENSE
6. V_{OUT}
7. V_{IN}

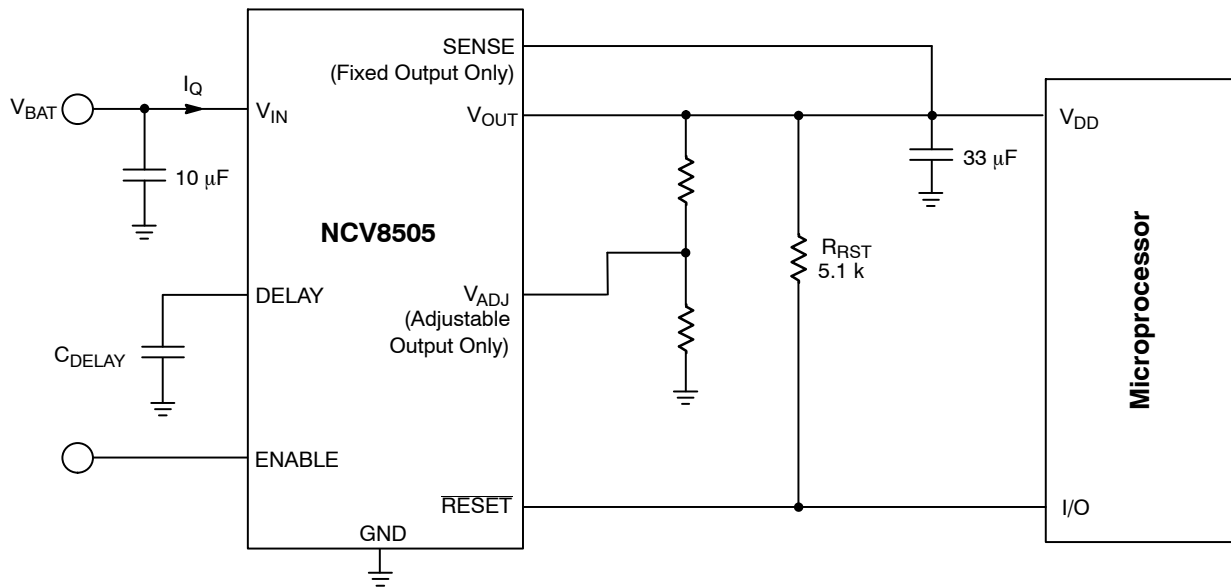


Figure 1. Application Diagram

NCV8505 Series

MAXIMUM RATINGS

Rating	Value	Unit
V_{IN} (DC)	–15 to 45	V
Peak Transient Voltage (46 V Load Dump @ $V_{IN} = 14$ V)	60	V
Operating Voltage	45	V
V_{OUT} (DC)	–0.3 to 16	V
Voltage Range ($\overline{RESET}$, DELAY)	–0.3 to 10	V
Input Voltage Range: V_{ADJ}	–0.3 to 16	V
Input Voltage Range (ENABLE)	–0.3 to 10*	V
ESD Susceptibility (Human Body Model) (Machine Model)	4.0 200	kV V
Junction Temperature, T_J	–40 to +150	°C
Storage Temperature, T_S	–55 to 150	°C
Package Thermal Resistance, 7 Lead D ² PAK Junction-to-Case, $R_{\theta JC}$ Junction-to-Ambient, $R_{\theta JA}$	2.0 10–50**	°C/W °C/W
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)	240 peak (Note 2)	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 60 second maximum above 183°C.

2. –5°C/+0°C allowable conditions.

*Reference Figure 16 for switched-battery ENABLE application.

**Depending on thermal properties of substrate, $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$.

ELECTRICAL CHARACTERISTICS ($I_{OUT} = 1.0$ mA, ENABLE = 5.0 V, –40°C ≤ T_J ≤ 150°C; V_{IN} = dependent on voltage option (Note 3); unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Stage					
Output Voltage for 2.5 V Option (V_O)	$6.5 \text{ V} < V_{IN} < 16 \text{ V}$, $1.0 \text{ mA} \leq I_{OUT} \leq 400 \text{ mA}$ $4.5 \text{ V} < V_{IN} < 26 \text{ V}$, $1.0 \text{ mA} \leq I_{OUT} \leq 400 \text{ mA}$	2.450 2.425	2.5 2.5	2.550 2.575	V V
Output Voltage for 3.3 V Option (V_O)	$7.3 \text{ V} < V_{IN} < 16 \text{ V}$, $1.0 \text{ mA} \leq I_{OUT} \leq 400 \text{ mA}$ $4.5 \text{ V} < V_{IN} < 26 \text{ V}$, $1.0 \text{ mA} \leq I_{OUT} \leq 400 \text{ mA}$	3.234 3.201	3.3 3.3	3.366 3.399	V V
Output Voltage for 5.0 V Option (V_O)	$9.0 \text{ V} < V_{IN} < 16 \text{ V}$, $1.0 \text{ mA} \leq I_{OUT} \leq 400 \text{ mA}$ $6.0 \text{ V} < V_{IN} < 26 \text{ V}$, $1.0 \text{ mA} \leq I_{OUT} \leq 400 \text{ mA}$	4.90 4.85	5.0 5.0	5.10 5.15	V V
Output Voltage for Adjustable Option (V_O)	$V_{OUT} = V_{ADJ}$ (Unity Gain) $6.5 \text{ V} < V_{IN} < 16 \text{ V}$, $1.0 \text{ mA} < I_{OUT} < 400 \text{ mA}$ $4.5 \text{ V} < V_{IN} < 26 \text{ V}$, $1.0 \text{ mA} < I_{OUT} < 400 \text{ mA}$	1.274 1.261	1.300 1.300	1.326 1.339	V V
Dropout Voltage ($V_{IN} - V_{OUT}$) (5.0 V and Adj. > 5.0 V Options Only)	$I_{OUT} = 400 \text{ mA}$ $I_{OUT} = 1.0 \text{ mA}$	– –	400 30	600 150	mV mV
Load Regulation	$V_{IN} = 14 \text{ V}$, $5.0 \text{ mA} \leq I_{OUT} \leq 400 \text{ mA}$	–30	5.0	30	mV
Line Regulation (2.5 V, 3.3 V, and Adjustable Options)	$4.5 \text{ V} < V_{IN} < 26 \text{ V}$, $I_{OUT} = 1.0 \text{ mA}$	–	5.0	25	mV
Line Regulation (5.0 V Option)	$6.0 \text{ V} < V_{IN} < 26 \text{ V}$, $I_{OUT} = 1.0 \text{ mA}$	–	5.0	25	mV
Quiescent Current, (I_Q) Active Mode	$I_{OUT} = 100 \mu\text{A}$, $V_{IN} = 12 \text{ V}$ $I_{OUT} = 75 \text{ mA}$, $V_{IN} = 14 \text{ V}$ $I_{OUT} \leq 400 \text{ mA}$, $V_{IN} = 14 \text{ V}$	– – –	200 2.5 25	350 5.0 45	μA mA mA
Quiescent Current, (I_Q) Sleep Mode	ENABLE = 0 V, $V_{IN} = 12 \text{ V}$, –40°C ≤ T_J ≤ 125°C	–	–	1.0	μA
Current Limit	–	425	800	–	mA
Short Circuit Output Current	$V_{OUT} = 0 \text{ V}$	100	500	–	mA
Thermal Shutdown	(Guaranteed by Design)	150	180	–	°C

3. Voltage range specified in the Output Stage of the Electrical Characteristics in boldface type.

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ELECTRICAL CHARACTERISTICS (continued) ($I_{OUT} = 1.0 \text{ mA}$, $ENABLE = 5.0 \text{ V}$, $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$; V_{IN} = dependent on voltage option (Note 4); unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Reset Function (RESET)					
RESET Threshold for 2.5 V Option HIGH (V_{RH}) LOW (V_{RL}) Hysteresis	$V_{IN} = 4.5 \text{ V}$ (Note 5) (Note 6) V_{OUT} Increasing V_{OUT} Decreasing	2.35 2.30 25	– – –	$1.0 \times V_O$ – –	V V mV
RESET Threshold for 3.3 V Option HIGH (V_{RH}) LOW (V_{RL}) Hysteresis	$V_{IN} = 4.5 \text{ V}$ (Note 5) (Note 6) V_{OUT} Increasing V_{OUT} Decreasing	3.10 3.00 35	– – –	$1.0 \times V_O$ – –	V V mV
RESET Threshold for 5.0 V Option HIGH (V_{RH}) LOW (V_{RL}) Hysteresis	$V_{IN} = 6.0 \text{ V}$ (Note 6) V_{OUT} Increasing V_{OUT} Decreasing	4.70 4.60 50	– – –	$1.0 \times V_O$ – –	V V mV
RESET Threshold for Adjustable Option HIGH (V_{RH}) LOW (V_{RL}) Hysteresis	$V_{IN} = 4.5 \text{ V}$ (Note 5) (Note 6) V_{OUT} Increasing V_{OUT} Decreasing	1.22 1.19 10	– – –	$1.0 \times V_O$ – –	V V mV
RESET Output Voltage Low (V_{RLO})	$V_{IN} = \text{Minimum}$ (Note 6) (Note 7) $1.0 \text{ V} \leq V_{OUT} \leq V_{RL}$, $R_{RESET} = 5.1 \text{ k}$	–	0.1	0.4	V
DELAY Switching Threshold (V_{DT}) (2.5 V, 3.3 V, and 5.0 V Options)	$V_{IN} = \text{Minimum}$ (Note 6) (Note 7)	1.4	1.8	2.2	V
DELAY Switching Threshold (V_{DT}) (Adjustable Option)	$V_{IN} = \text{Minimum}$ (Note 6) (Note 7)	1.0	1.3	1.6	V
DELAY Low Voltage	$V_{IN} = \text{Minimum}$ (Note 6) (Note 7) $V_{OUT} < \text{RESET Threshold Low(min)}$	–	–	0.2	V
DELAY Charge Current	$V_{IN} = \text{Minimum}$ (Note 6) (Note 7) DELAY = 1.0 V, $V_{OUT} > V_{RH}$	2.5	4.0	5.5	μA
DELAY Discharge Current	$V_{IN} = \text{Minimum}$ (Note 6) (Note 7) DELAY = 1.0 V, $V_{OUT} < V_{RL}$	5.0	–	–	mA

Voltage Adjust (Adjustable Output only)

Input Current	$V_{ADJ} = 1.25 \text{ V}$, $V_{IN} = \text{Minimum}$ (Note 6) (Note 7)	–0.5	–	0.5	μA
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ENABLE

Input Threshold	Low, $V_{IN} = 14 \text{ V}$ (Note 6) High, $V_{IN} = 14 \text{ V}$ (Note 6)	– 2.0	– –	1.0 –	V V
Input Current	ENABLE = 5.0 V, $V_{IN} = 14 \text{ V}$ (Note 6)	–	30	75	μA

4. Voltage range specified in the Output Stage of the Electrical Characteristics in boldface type.

5. For $V_{IN} \leq 4.5 \text{ V}$, a RESET = Low may occur with the output in regulation.

6. Part is guaranteed by design to meet specification over the entire V_{IN} voltage range, but is production tested only at the specified V_{IN} voltage.

7. Minimum $V_{IN} = 4.5 \text{ V}$ for 2.5 V, 3.3 V, and Adjustable options. Minimum $V_{IN} = 6.0 \text{ V}$ for 5.0 V option.

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PACKAGE PIN DESCRIPTION, ADJUSTABLE OUTPUT

Pin Number	Pin Symbol	Function
1	DELAY	Timing capacitor for $\overline{\text{RESET}}$ function.
2	ENABLE	ENABLE control for the IC. A high powers the device up.
3	$\overline{\text{RESET}}$	Active reset (accurate to $V_{\text{OUT}} \geq 1.0 \text{ V}$)
4	GND	Ground. All GND leads must be connected to Ground.
5	V_{ADJ}	Voltage Adjust. A resistor divider from V_{OUT} to this lead sets the output voltage.
6	V_{OUT}	$\pm 2.0\%$, 400 mA output.
7	V_{IN}	Input Voltage.

PACKAGE PIN DESCRIPTION, FIXED OUTPUT

Pin Number	Pin Symbol	Function
1	DELAY	Timing capacitor for $\overline{\text{RESET}}$ function.
2	ENABLE	ENABLE control for the IC. A high powers the device up.
3	$\overline{\text{RESET}}$	Active reset (accurate to $V_{\text{OUT}} \geq 1.0 \text{ V}$)
4	GND	Ground. All GND leads must be connected to Ground.
5	SENSE	Kelvin connection which allows remote sensing of output voltage for improved regulation. If remote sensing is not desired, connect to V_{OUT} .
6	V_{OUT}	$\pm 2.0\%$, 400 mA output.
7	V_{IN}	Input Voltage.

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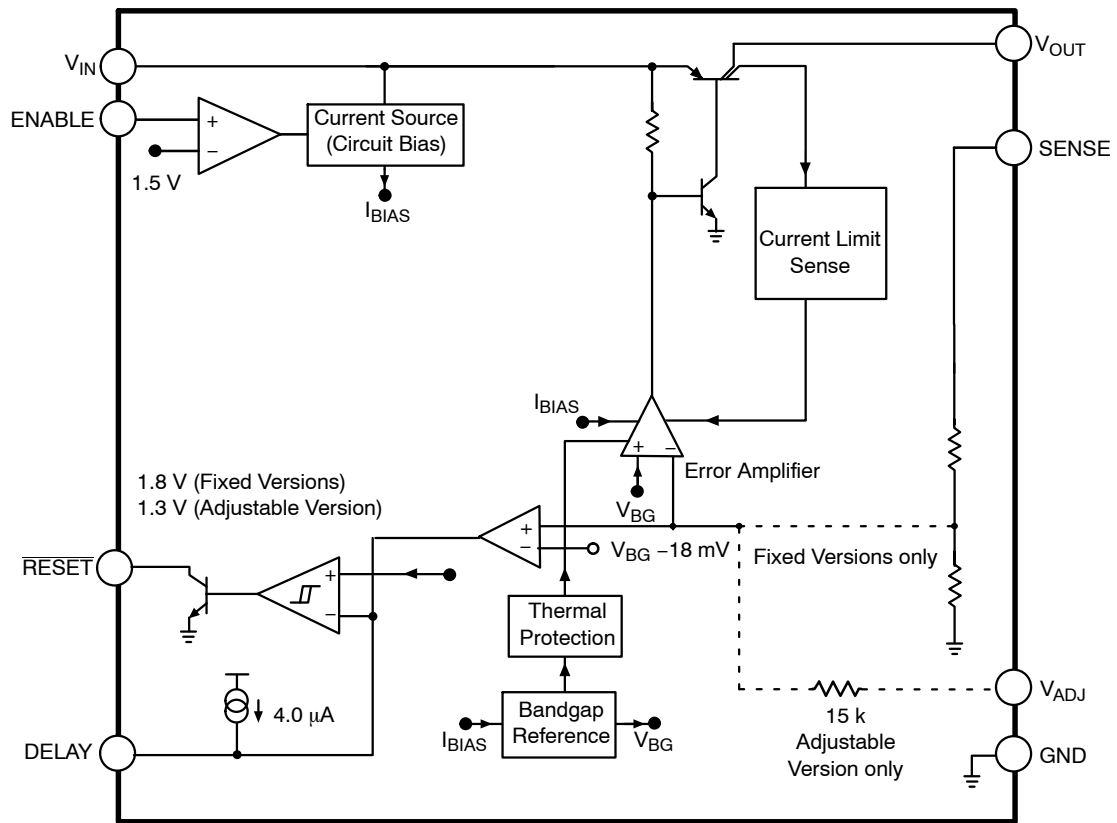


Figure 2. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

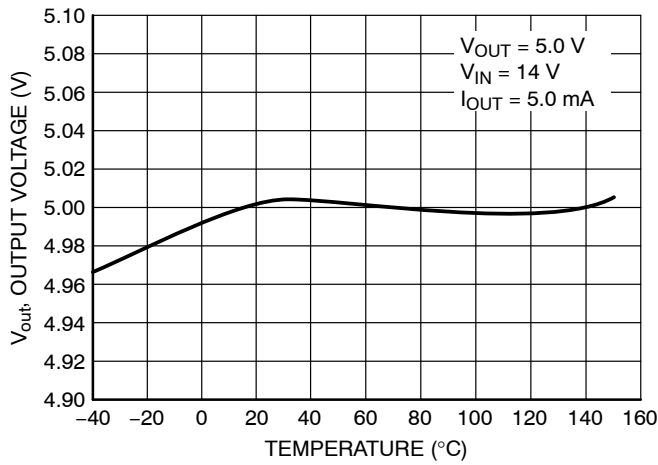


Figure 3. 5 V Output Voltage vs. Temperature

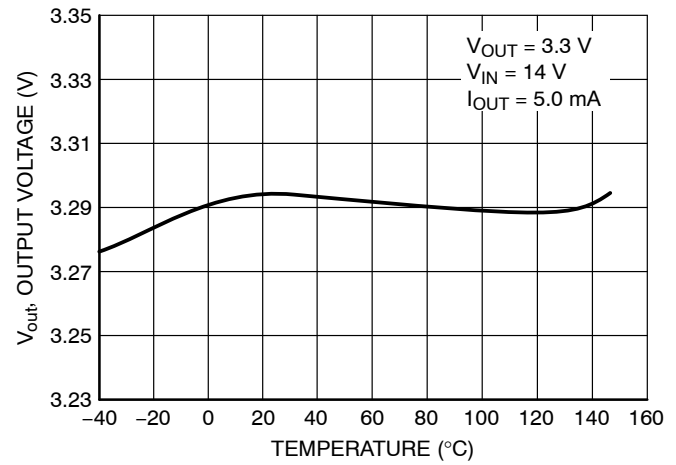


Figure 4. 3.3 V Output Voltage vs. Temperature

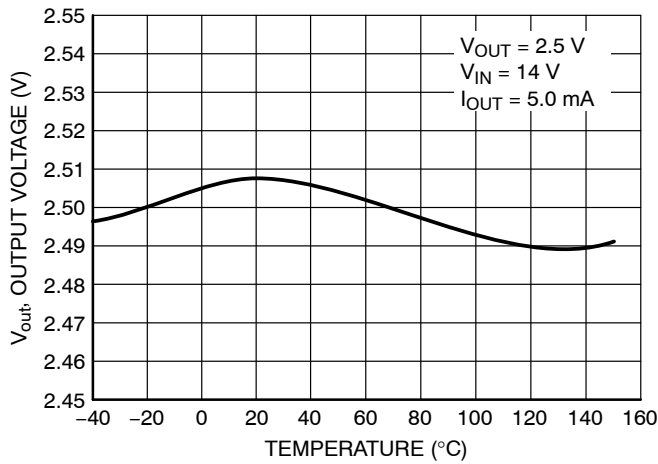


Figure 5. 2.5 V Output Voltage vs. Temperature

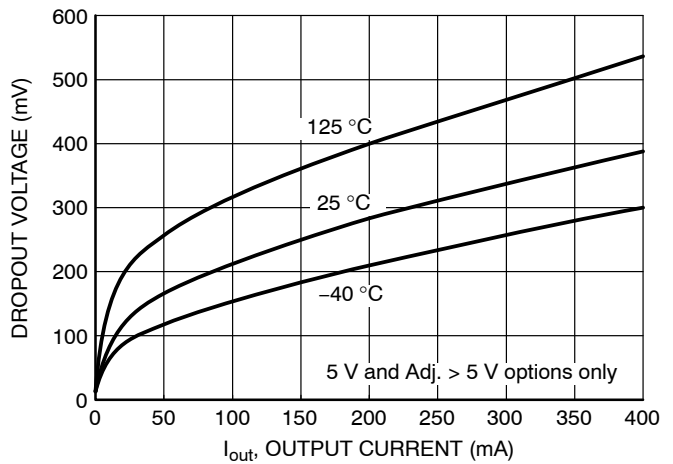


Figure 6. Dropout Voltage vs. Output Current

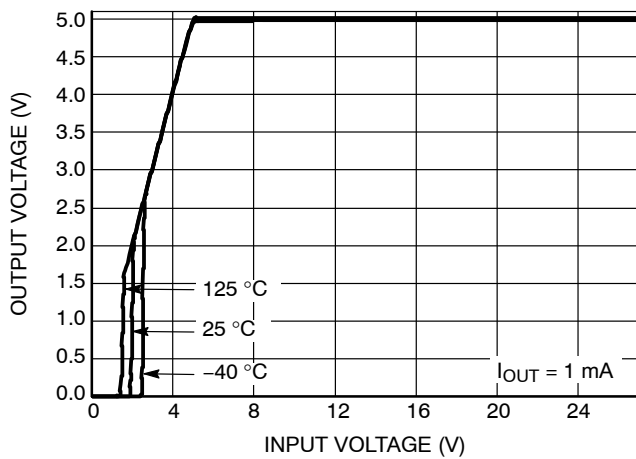


Figure 7. Output Voltage vs. Input Voltage

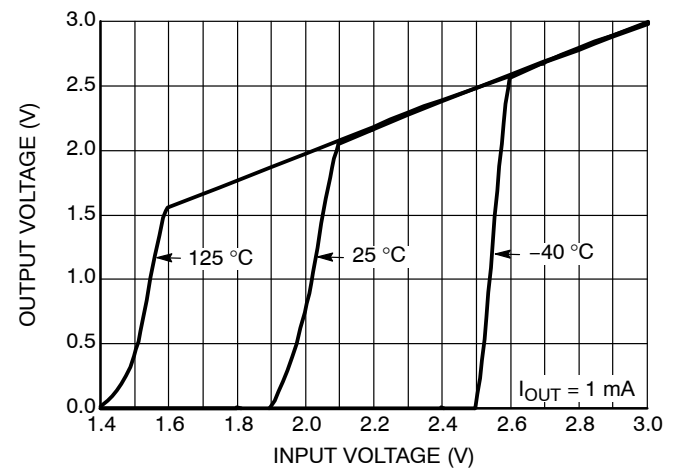


Figure 8. Output Voltage vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

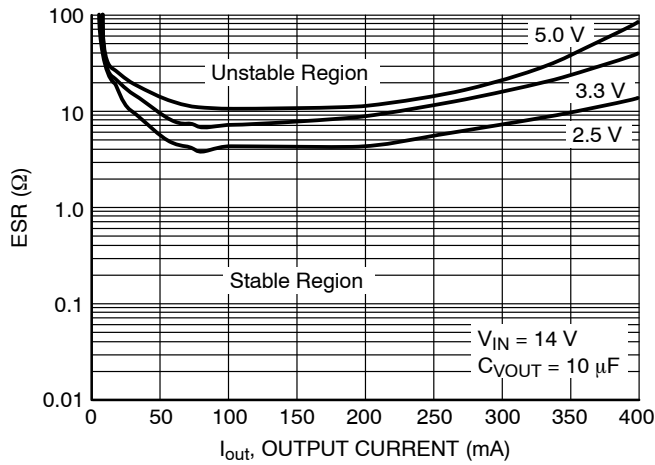


Figure 9. Output Stability with Output Voltage Change

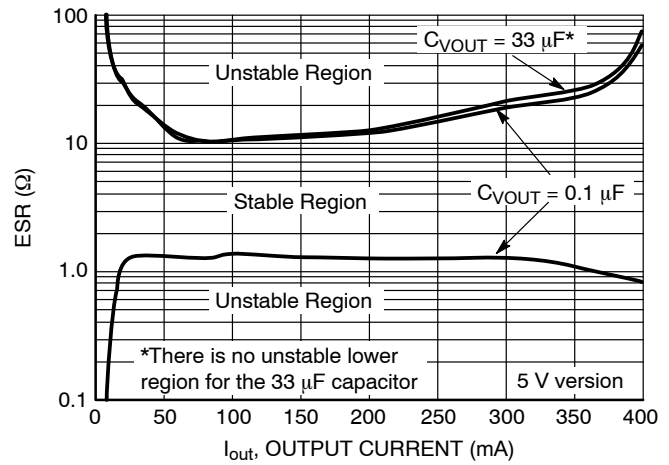


Figure 10. Output Stability with Output Capacitor Change

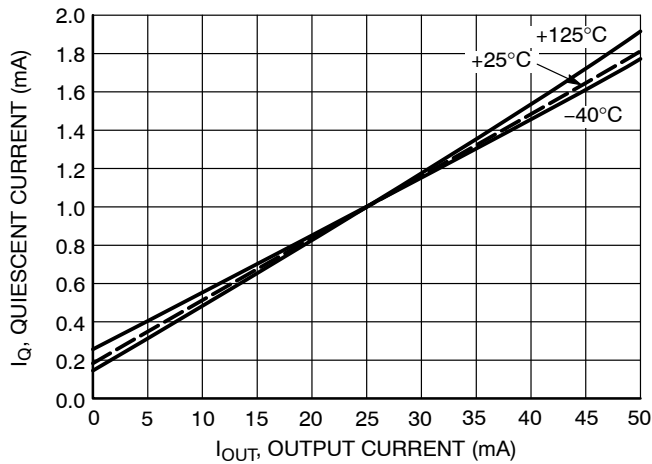


Figure 11. Quiescent Current vs. Output Current

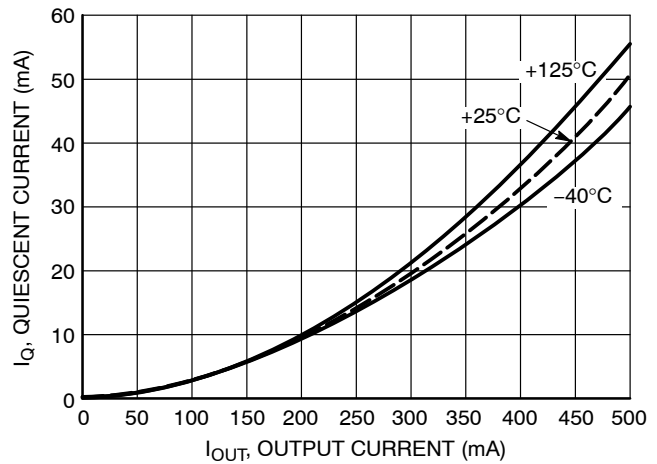


Figure 12. Quiescent Current vs. Output Current

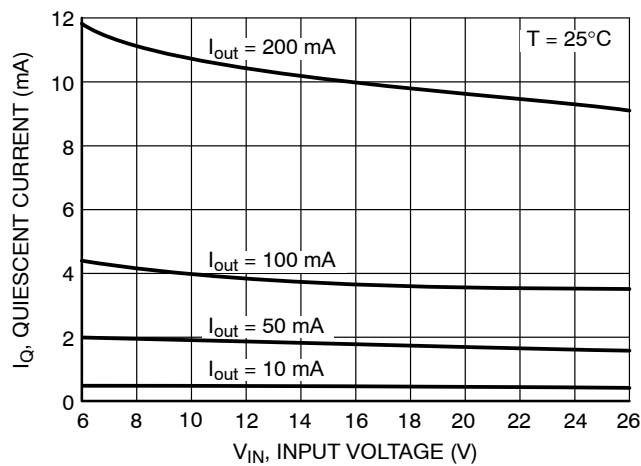


Figure 13. Quiescent Current vs. Input Voltage

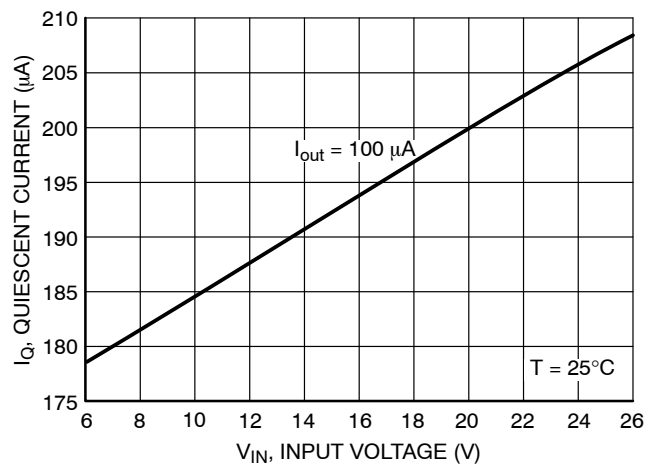


Figure 14. Quiescent Current vs. Input Voltage

CIRCUIT DESCRIPTION

REGULATOR CONTROL FUNCTIONS

The NCV8505 contains the microprocessor compatible control function $\overline{\text{RESET}}$ (Figure 15).

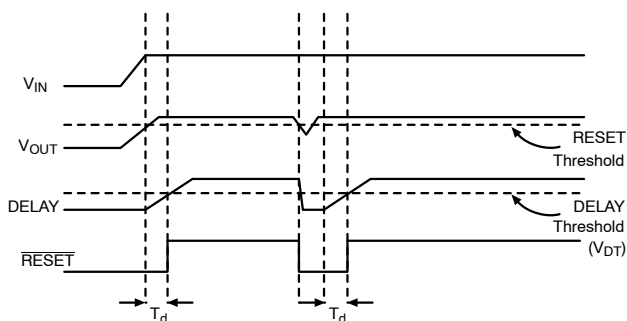


Figure 15. Reset and Delay Circuit Wave Forms

RESET Function

A $\overline{\text{RESET}}$ signal (low voltage) is generated as the IC powers up until V_{OUT} is within 1.5% of the regulated output voltage, or when V_{OUT} drops out of regulation, and is lower than 4.0% below the regulated output voltage. Hysteresis is included in the function to minimize oscillations.

The $\overline{\text{RESET}}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC thereby guaranteeing that the $\overline{\text{RESET}}$ signal is valid for V_{OUT} as low as 1.0 V.

ENABLE Function

The part stays in a low I_Q sleep mode when the ENABLE pin is held low. The part has an internal pull down if the pin is left floating.

The integrity of the ENABLE pin allows it to be tied to the battery line through an external resistor. It will withstand load dump potentials in this configuration.

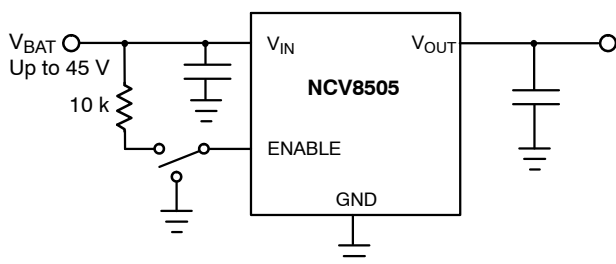


Figure 16. ENABLE Function

DELAY Function

The reset delay circuit provides a programmable (by external capacitor) delay on the $\overline{\text{RESET}}$ output lead.

The DELAY lead provides source current (typically 4.0 μA) to the external DELAY capacitor during the following proceedings:

1. During Power Up (once the regulation threshold has been verified).
2. After a reset event has occurred and the device is back in regulation. The DELAY capacitor is discharged when the regulation ($\overline{\text{RESET}}$ threshold) has been violated. This is a latched incident. The capacitor will fully discharge and wait for the device to regulate before going through the delay time event again.

Voltage Adjust

Figure 17 shows the device setup for a user configurable output voltage. The feedback to the V_{ADJ} pin is taken from a voltage divider referenced to the output voltage. The loop is balanced around the Unity Gain threshold (1.30 V typical).

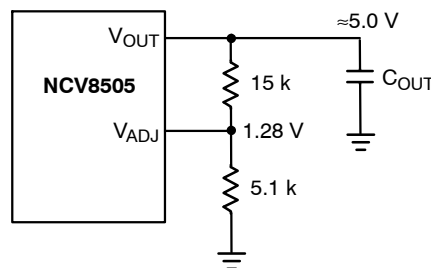


Figure 17. Adjustable Output Voltage

APPLICATION NOTES

SETTING THE DELAY TIME

The delay time is controlled by the Reset Delay Low Voltage, Delay Switching Threshold, and the Delay Charge Current. The delay follows the equation:

$$t_{\text{DELAY}} = \frac{C_{\text{DELAY}}(V_{\text{dt}} - \text{Reset Delay Low Voltage})}{\text{Delay Charge Current}}$$

Example:

Using $C_{\text{DELAY}} = 33 \text{ nF}$.

Assume reset Delay Low Voltage = 0.

Use the typical value for $V_{\text{dt}} = 1.8 \text{ V}$ (2.5 V, 3.3 V, and 5.0 V options).

Use the typical value for Delay Charge Current = $4.2 \mu\text{A}$.

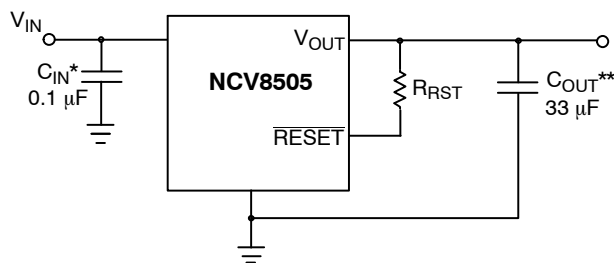
$$t_{\text{DELAY}} = \frac{[33 \text{ nF}(1.8 - 0)]}{4.2 \mu\text{A}} = 14 \text{ ms}$$

STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (-25°C to -40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_{OUT} shown in Figure 18 should work for most applications, however it is not necessarily the optimized solution.



* C_{IN} required if regulator is located far from the power supply filter.

** C_{OUT} required for stability. Capacitor must operate at minimum temperature expected.

Figure 18. Test and Application Circuit Showing Output Compensation

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 19) is:

$$P_{\text{D(max)}} = [V_{\text{IN(max)}} - V_{\text{OUT(min)}}]I_{\text{OUT(max)}} + V_{\text{IN(max)}}I_{\text{Q}} \quad (1)$$

where:

$V_{\text{IN(max)}}$ is the maximum input voltage,

$V_{\text{OUT(min)}}$ is the minimum output voltage,

$I_{\text{OUT(max)}}$ is the maximum output current for the application, and

I_{Q} is the quiescent current the regulator consumes at $I_{\text{OUT(max)}}$.

Once the value of $P_{\text{D(max)}}$ is known, the maximum permissible value of $R_{\theta\text{JA}}$ can be calculated:

$$R_{\theta\text{JA}} = \frac{150^{\circ}\text{C} - T_{\text{A}}}{P_{\text{D}}} \quad (2)$$

The value of $R_{\theta\text{JA}}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta\text{JA}}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C .

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

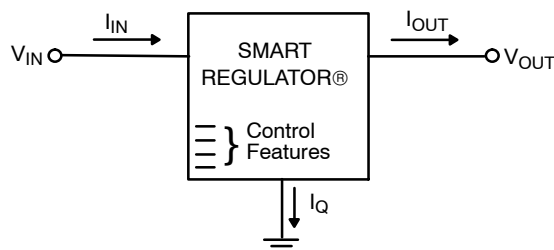


Figure 19. Single Output Regulator with Key Performance Parameters Labeled

HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta\text{JA}}$:

$$R_{\theta\text{JA}} = R_{\theta\text{JC}} + R_{\theta\text{CS}} + R_{\theta\text{SA}} \quad (3)$$

where:

$R_{\theta\text{JC}}$ = the junction-to-case thermal resistance,

$R_{\theta\text{CS}}$ = the case-to-heatsink thermal resistance, and

$R_{\theta\text{SA}}$ = the heatsink-to-ambient thermal resistance.

$R_{\theta\text{JC}}$ appears in the package section of the data sheet. Like $R_{\theta\text{JA}}$, it too is a function of package type. $R_{\theta\text{CS}}$ and $R_{\theta\text{SA}}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

NCV8505 Series

ORDERING INFORMATION

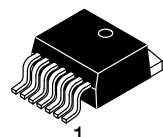
Device	Output Voltage	Package	Shipping [†]
NCV8505D2TADJG	Adjustable	D ² PAK-7 (Pb-Free)	50 Units / Rail
NCV8505D2TADJR4G		D ² PAK-7 (Pb-Free)	750 Tape & Reel
NCV8505D2T25G	2.5 V	D ² PAK-7 (Pb-Free)	50 Units / Rail
NCV8505D2T25R4G		D ² PAK-7 (Pb-Free)	750 Tape & Reel
NCV8505D2T33G	3.3 V	D ² PAK-7 (Pb-Free)	50 Units / Rail
NCV8505D2T33R4G		D ² PAK-7 (Pb-Free)	750 Tape & Reel
NCV8505D2T50G	5.0 V	D ² PAK-7 (Pb-Free)	50 Units / Rail
NCV8505D2T50R4G		D ² PAK-7 (Pb-Free)	750 Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

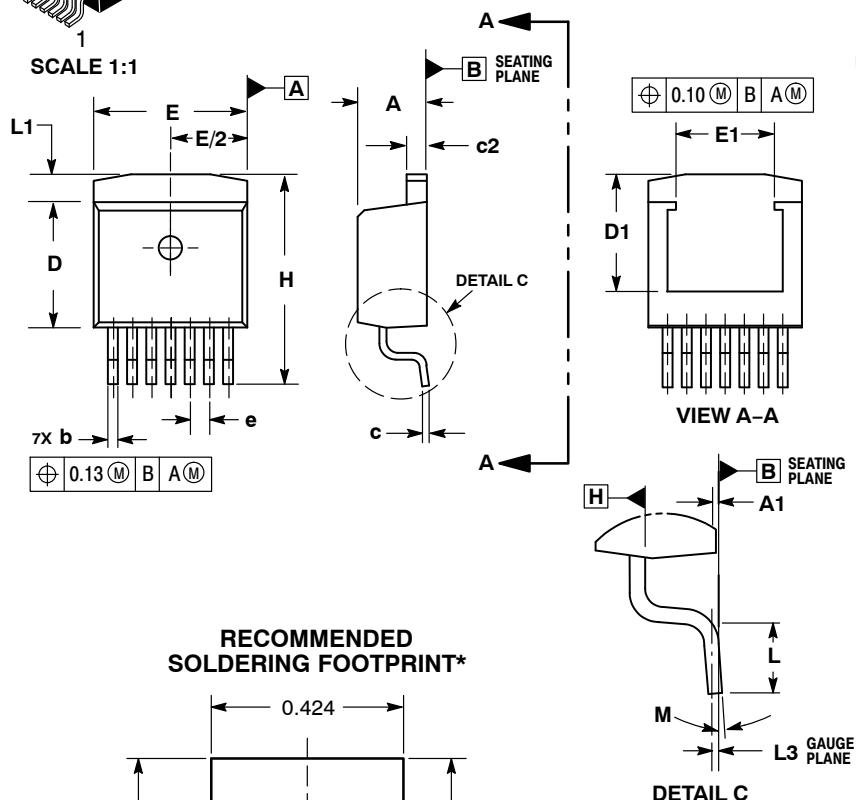
ON



D²PAK-7 (SHORT LEAD) CASE 936AB-01 ISSUE B

DATE 08 SEP 2009

SCALE 1:1

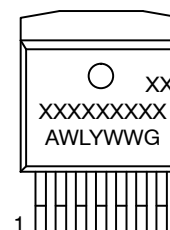


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.005 MAXIMUM PER SIDE. THESE DIMENSIONS TO BE MEASURED AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1. DIMENSIONS D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THE THERMAL PAD.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.170	0.180	4.32	4.57
A1	0.000	0.010	0.00	0.25
b	0.026	0.036	0.66	0.91
c	0.017	0.026	0.43	0.66
c2	0.045	0.055	1.14	1.40
D	0.325	0.368	8.25	9.53
D1	0.270	---	6.86	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.050 BSC		1.27 BSC	
H	0.539	0.579	13.69	14.71
L	0.058	0.078	1.47	1.98
L1	---	0.066	---	1.68
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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