RClamp0542ZA

Femto Farad RailClamp®
2-Line, 300fF ESD Protection

PROTECTION PRODUCTS

Description

RClamp®0542ZA is an ultra low capacitance ESD protection device designed to protect two high-speed lines in an 0201 footprint. This revolutionary package design reduces board space requirements by more than 50% over existing single line solutions. RClamp0542ZA is a three pin device with identical low capacitance TVS diodes connected to each pin. Any two pins may be connected to high-speed lines, while the third pin is connected to ground. This gives the designer maximum flexibility in pcb routing. Each line has a maximum capacitance of only 0.30pF resulting in a typical corner frequency of 12GHz.

RClamp0542ZA is in a 3-pin SLP0603P3X3F package. It measures 0.62 x 0.32 mm with a nominal height of only 0.25mm. Leads are finished with lead-free NiAu. The combination of small size and high ESD surge capability makes them ideal for use in portable applications such as cellular phones, digital cameras, and tablets.

Features

- High ESD withstand voltage
  - IEC 61000-4-2 (ESD) 17kV (air), 12kV (contact)
- Very small PCB area
- Protects two high-speed data lines
- Working voltage: 5V
- Low reverse leakage current: <1nA typ at VR=5V
- Low capacitance: 0.30pF maximum
- Dynamic resistance: 1.17 Ohms (Typ)
- Solid-state silicon-avalanche technology

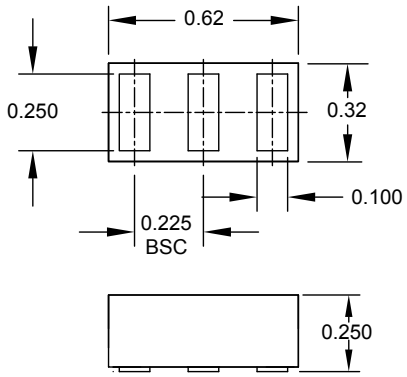
Mechanical Characteristics

- SLP0603P3X3F package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: 0.62 x 0.32 x 0.25 mm
- Lead Finish: NiAu
- Marking : Marking code
- Packaging : Tape and Reel

Applications

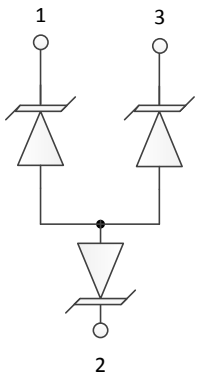
- High-Speed Lines
- MIPI / MDDI
- USB 3.0
- HDMI
- MHL
- eDP

Nominal Dimensions



Nominal Dimensions in mm

Functional Schematic



Device Schematic

Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20µs)	P_{PK}	40	W
Peak Pulse Current (tp = 8/20µs)	I_{PP}	2	A
ESD per IEC 61000-4-2 (Air)(1) ESD per IEC 61000-4-2 (Contact)(1)	V_{ESD}	±17 ±12	kV
Operating Temperature	T_J	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

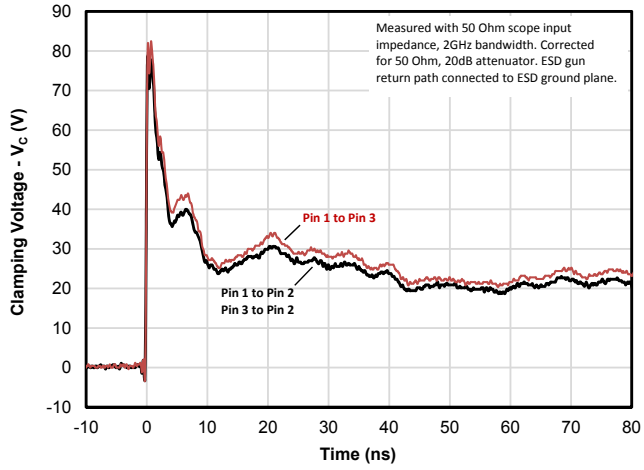
Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V_{RWM}	-40°C to 85°C Between any two pins				5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 10mA, Between any two pins	-40°C to 85°C	6.5	9.5	11.5	V
Reverse Leakage Current	I_R	V_{RWM} = 5V	T = 25°C		0.01	0.050	µA
			T = 85°C		0.05	0.250	µA
Clamping Voltage	V_C	I_{PP} = 2A, tp = 8/20µs, Between any two pins			12	20	V
ESD Clamping Voltage[2]	V_C	I_{PP} = 4A, tp = 0.2/100ns (TLP) Pin 1 to 2, Pin 3 to 2			16		V
ESD Clamping Voltage[2]	V_C	I_{PP} = 16A, tp = 0.2/100ns (TLP) Pin 1 to 2, Pin 3 to 2			30		V
Dynamic Resistance[2, 3]	R_{DYN}	tp = 0.2/100ns (TLP) Pin 1 to 2, Pin 3 to 2			1.17		Ohms
Cut-Off Frequency	f_C	Insertion Loss (S21) = -3dB			12		GHz
Junction Capacitance	C_J	V_R = 0V, f = 1MHz Between any two pins	T = 25°C		0.27	0.30	pF
Change in Capacitance over VR	ΔC_{jVR}	VR = 0 - 5V, f = 1MHz				0.030	pF

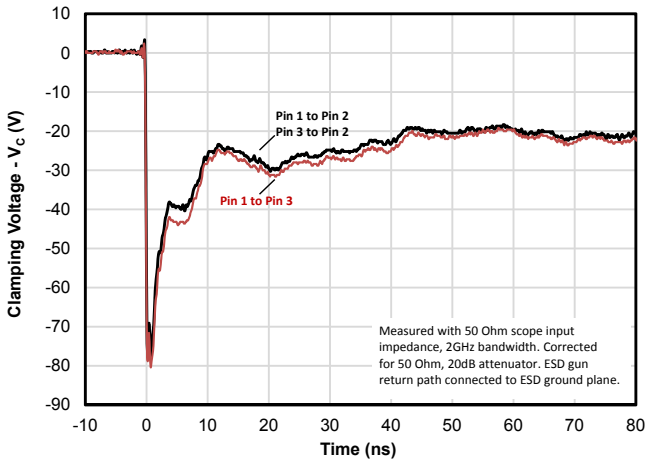
Notes:
(1): ESD Gun return path to Ground Reference Plane (GRP)
(2): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t_1 = 70ns to t_2 = 90ns.
(3): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A

Typical Characteristics

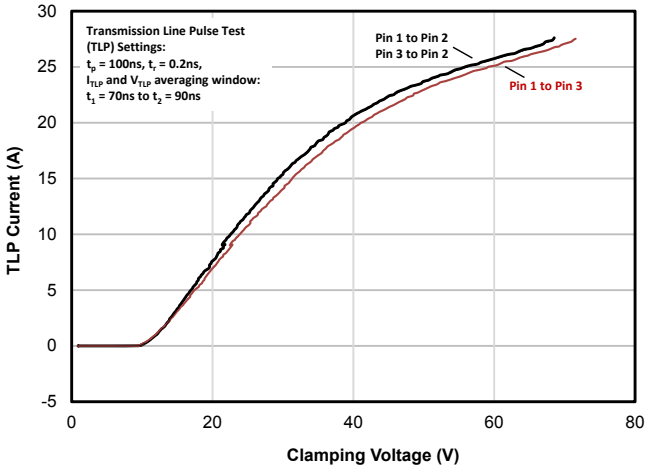
ESD Clamping (+8kV Contact per IEC 61000-4-2)



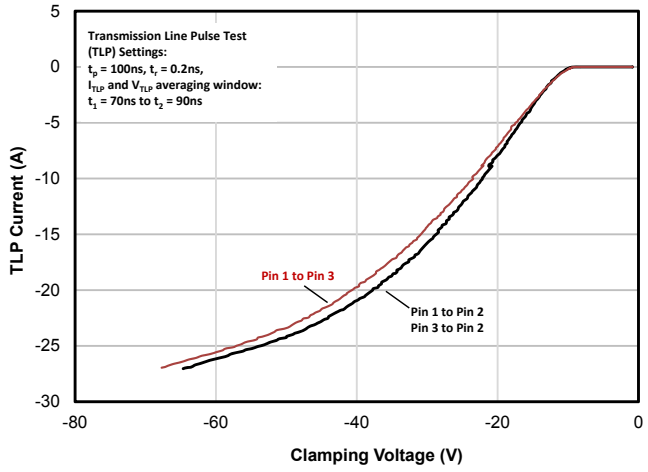
ESD Clamping (-8kV Contact per IEC 61000-4-2)



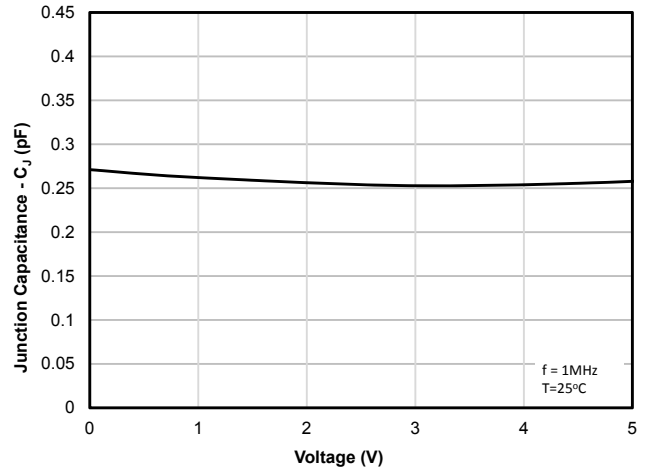
TLP IV Curve (Positive Pulse)



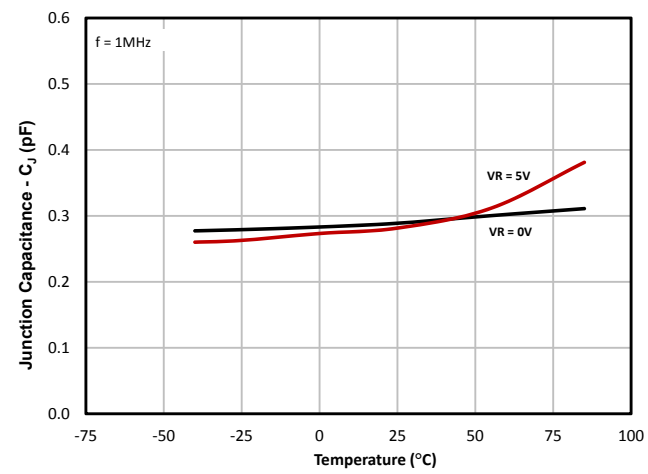
TLP IV Curve (Negative Pulse)



Capacitance vs. Reverse Voltage

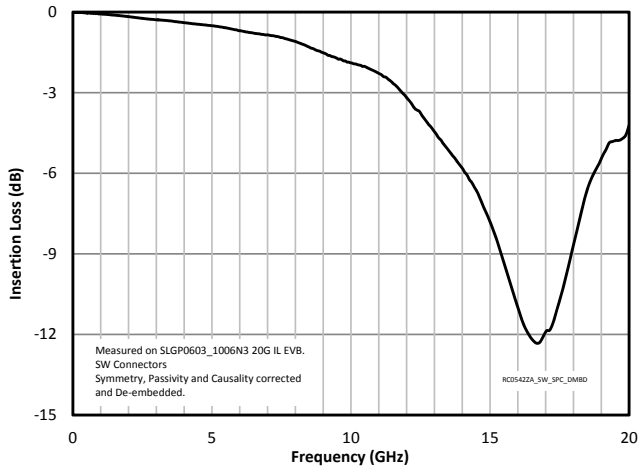


Capacitance vs. Temperature

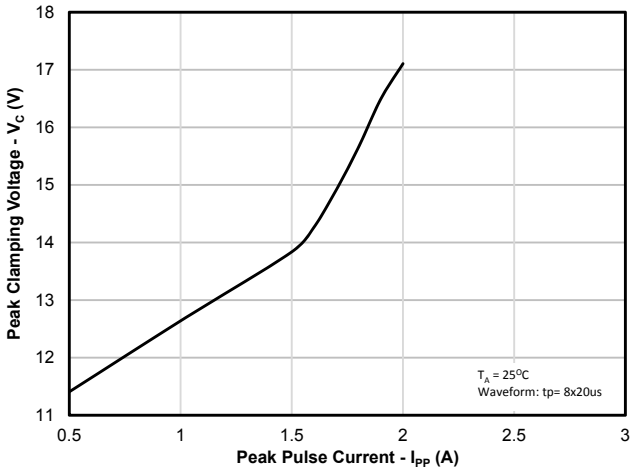


Typical Characteristics (Continued)

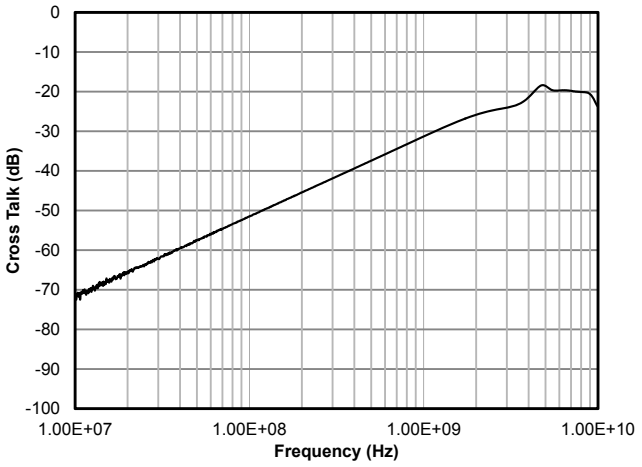
Insertion Loss - S21



Clamping Voltage vs. Peak Pulse Current (tp=8/20us)



Analog Crosstalk



Applications Information

Assembly Guidelines

The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Semtech's recommended mounting pattern is based on the following design guidelines:

Land Pattern

The recommended land pattern follows IPC standards and is designed for maximum solder coverage. Detailed dimensions are shown elsewhere in this document.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W)/ (2 * (L + W) * T)

Where:
L = Aperture Length
W = Aperture Width
T = Stencil Thickness

The outer pads are designed to have an area ratio of 0.71. The minimum recommended area ratio is 0.66 to achieve good solder paste transfer. In addition to increasing the area ratio, the increased width of the pads aid in self-centering the package during reflow soldering. During reflow, the solder will tend to "pull" the package outward on each side, thus aiding in centering the device. Some device "tilt" may be observed and is normal. Tilting will not affect the electrical performance. Pad length may be slightly reduced in order to minimize device tilt, however this will also reduce the area ratio as described above.

The center pad opening is minimized in order to reduce the chance of solder bridging. While the area ratio is slightly less than optimal, increasing the pad size would reduce the gap between the pads thus increasing the chance of solder bridging. Note however that the package is fully encapsulated and is not conductive to any of the pins.

Semtech recommends the stencil have a rectangular aperture with rounded corners for consistent solder release. The stencil should be laser cut with electropolished finish. A stencil thickness of 0.075mm (0.003") is recommended.

Recommended Mounting Pattern

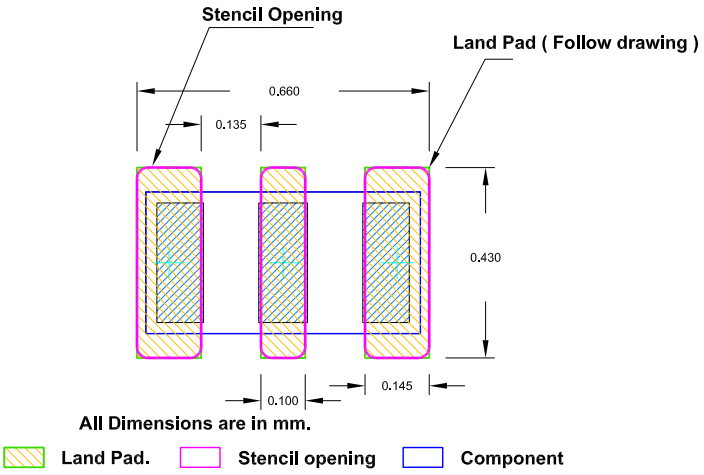
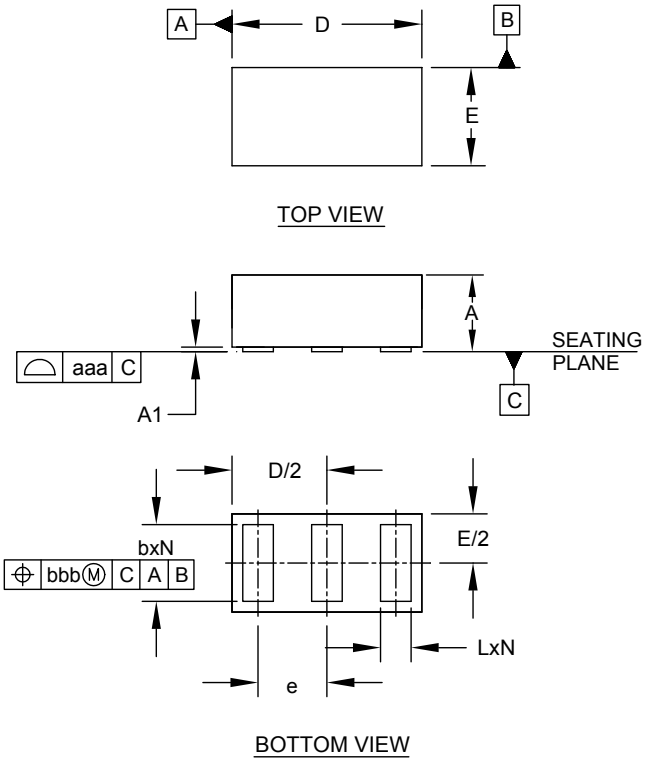


Table 1 - Recommended Assembly Guidelines	
Assembly Parameter	**Recommendation**
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with rounded corners
Solder Stencil Thickness	0.075mm (0.003")
Solder Paste Type	Type 4 size sphere or smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Solder Mask Defined (Preferred) or Non-Solder Mask Defined
PCB Pad Finish	OSP or NiAu

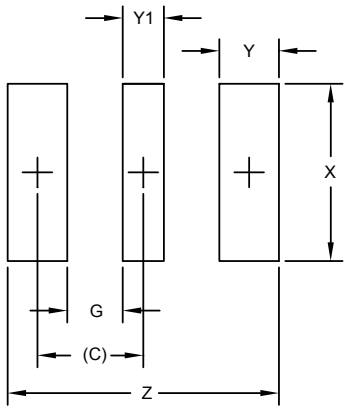
Outline Drawing - SLP0603P3X3F



DIMENSIONS			
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.225	0.250	0.275
A1	0.005	0.015	0.050
b	0.230	0.250	0.270
D	0.580	0.62	0.650
E	0.280	0.32	0.350
e	0.225 BSC		
L	0.080	0.100	0.120
N	3		
aaa	0.08		
bbb	0.10		

NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).

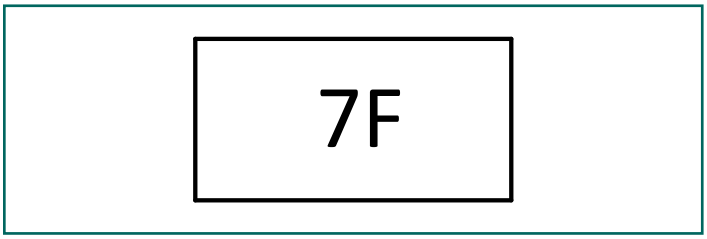
Land Pattern - SLP0603P3X3F



DIMENSIONS	
DIM	MILLIMETERS
C	(0.258)
G	0.135
X	0.430
Y	0.145
Y1	0.100
Z	0.660

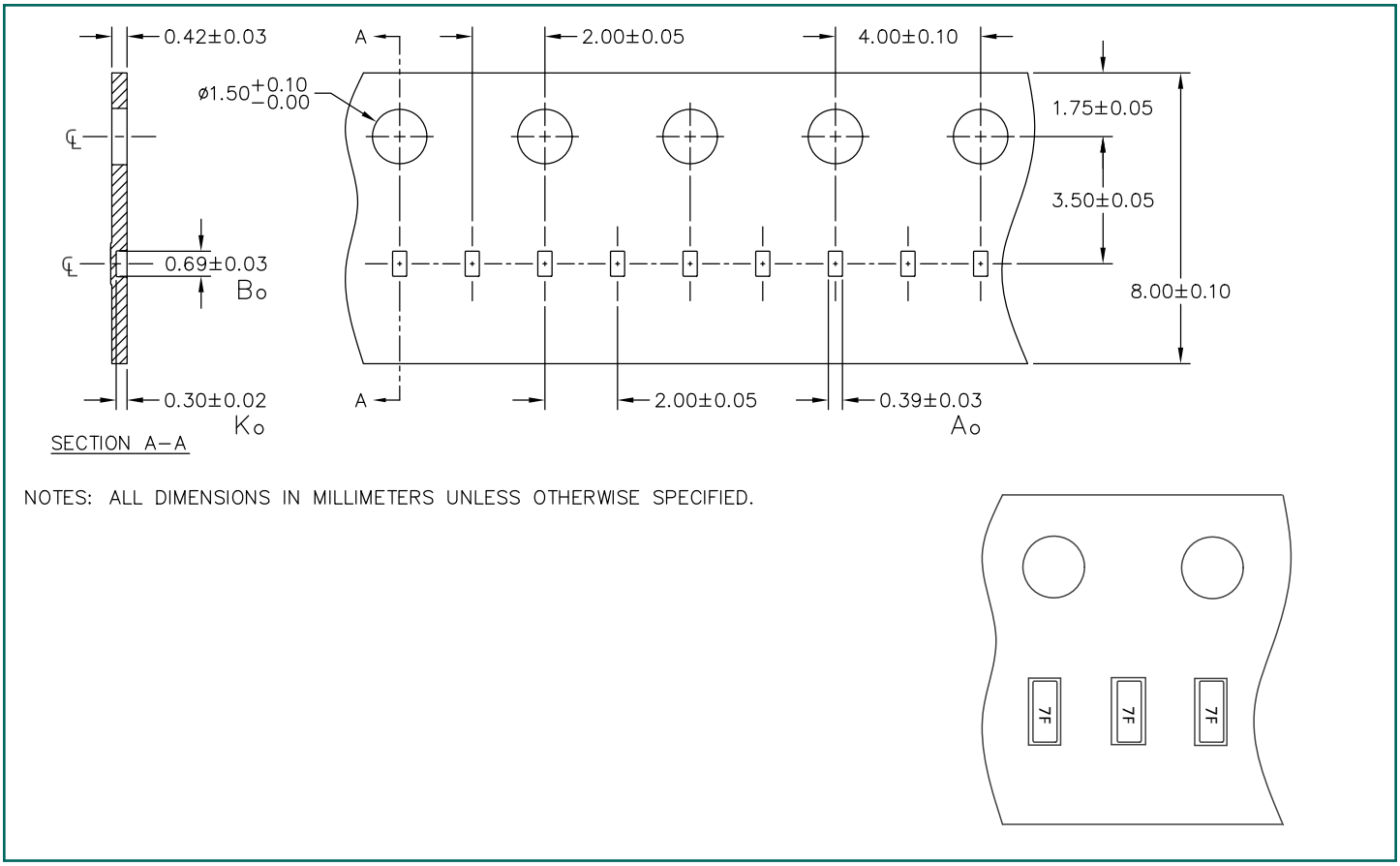
NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code



Notes: Device is electrically symmetrical

Tape and Reel Specification



Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp0542ZATFT	15000	7 Inch
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Contact Information

Semtech Corporation
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111, Fax: (805) 498-3804
www.semtech.com