2019

YT8010 Datasheet

100BASE-T1 PHY FOR AUTOMOTIVE ETHERNET

REV V0.1

裕太车通
MotorComm

Revision History

Revision	Release Date	Summary
0.1		Draft
1.0		Update register table

Table of Content

内容

1. GENERAL DESCRIPTION

The MotorComm YT8010 is a single pair Ethernet physical layer transceiver (PHY) which implements the Ethernet physical layer portion of the 100BASE-T1 standard as defined by the IEEE 802.3bw task force. Ideally suited for a wide range of automotive applications, it is manufactured using a standard digital CMOS process and contains all the active circuitry required to implement the physical layer functions to transmit and receive data on a single balanced twisted pair.

Based on cutting-edge DSP technology, combing adaptive equalizers, echo canceller, phaselocked, ADCs, phase-locked loops, line drivers, encoders/decoders, echo cancelers and all other required support circuitry at a 100Mbps data rate to achieve robust performance and exceed automotive electromagnetic interference (EMI) requirements in noisy environments with very low power dissipation.

The YT8010 is designed to be fully compliant with RGMII, RMII and MII interface specifications, allowing compatibility with industry-standard Ethernet media access controllers (MACs) and switch controllers.

The YT8010 delivers the most comprehensive automotive technology solution required by OEM and Tier 1 suppliers, meeting AEC-Q100 Grade 1 temperature range.

TARGET APPLICATIONS

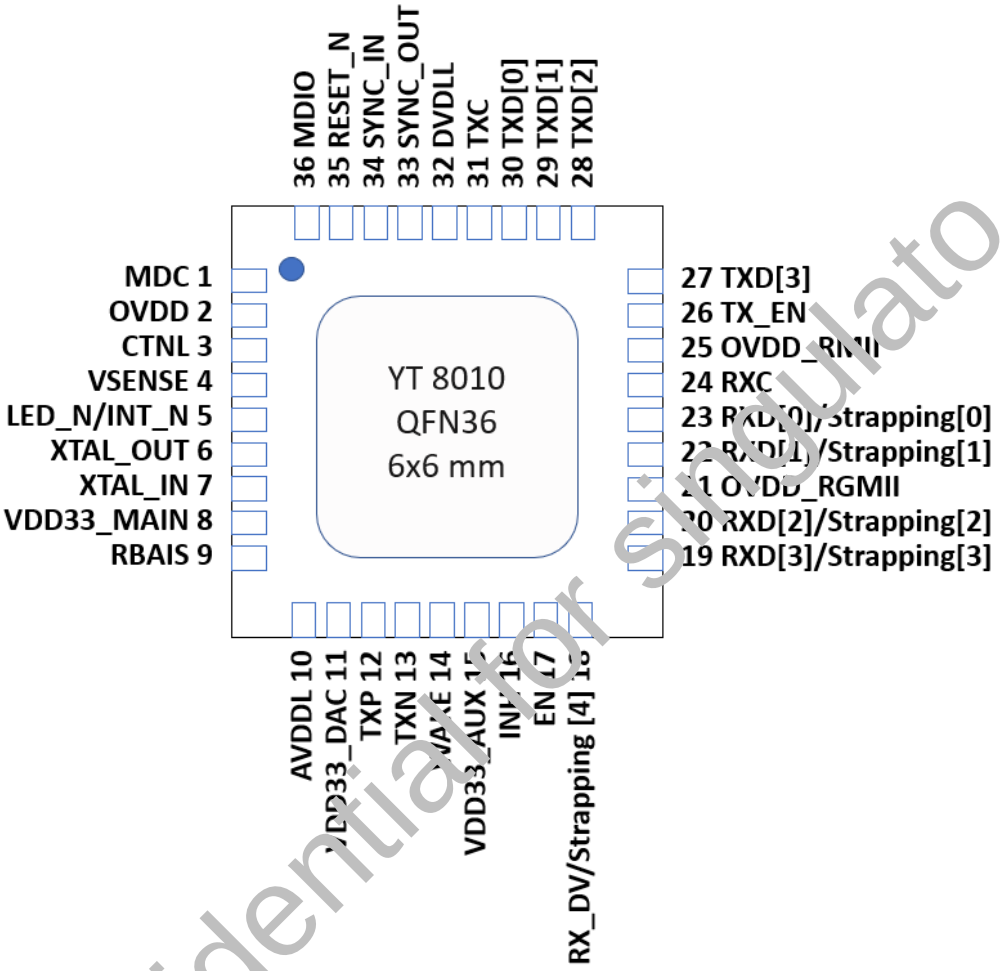
- Automotive infotainment systems
- Automotive diagnostics
- Advanced driver assist systems
- Body electronics

2. FEATURE

- 100BASE-T1 Transceiver
  - 100BASE-T1 IEEE 802.3bw standards
  - Full duplex
  - Rapid linkup time
- Support auto cable detection and working mode selection.
- MII/RMII/RGMII support
- RMII/RGMII interface EMI enhancement
- Support latency accommodation of RGMII clock
- Support IEEE 802.1AS
- Support Remote Wake up 3.3V analog supply.
- Advanced low-power management with local wake-up support
- Automotive Cable Diagnostics support
- Integrated LDO regulator allowing a single supply
- Internal/external/remote loopback mode for diagnosis
- MDI pins protected against ESD to 6kV HBM and 6kV IEC61000-4-2
- Jumbo frame support up to 16 kB
- Polarity detection and auto/manual correction
- Integrated twisted pair termination resistors
- AEC-Q100 Grade 1 (-40~125°C)
- Trace matched output impedance
- Integrated low-pass filter
- Support over Temperature warning.
- Robust cable ESD tolerance
- Package QFN 36, 6x6mm

3 PIN ASSIGMENT

YT8010 QFN36 6X6MM



PIN DESCRIPTIONS

- I = Input
- = Output
- I/O = Bidirectional
- OD = Open-drain output
- OT = Tristateable signal
- B = Bias
- PU = Internal pull-up
- PD = Internal pull-down
- SOR = Sample on reset
- CS = Continuously sampled
- ST = Schmitt trigger
- XT = Crystal inputs/outputs pin type
- D = Digital pin type
- G = RGMII pin type
- A = Analog pin type

Pin No.	Symbol	Type	Description
1	MDC	I; ST	Management Data Clock. Only need to be effect during mdio operation
2	OVDD	PWR, IO	2.5V or 3.3V for non-RGMII digital pads. When 2.5V is selected, RESET, MDIO, and LED pins are not 3.3V tolerant.
3	VCNTL	Ana	Vcontrol. Output point of an internal error amplifier. This pin shall be connected to the base of an external PNP power transistor.
4	VSENSE	Ana	Vsense. Sensing point of the external power transistor. This pin shall be connected to the external 1.2V power.
5	LED_N/INT_N	O,od	LED_N/INT_N Dual function pin. This pin is a dual function pin. It is active low unless programmed through MDIO.
6	XTAL_OUT	O/XT	25 MHz Crystal Oscillator Output Pin. A continuous 25 MHz reference clock must be supplied to the chip by connecting a 25 MHz crystal between these two pins or by driving XTAL_IN with an external 25 MHz clock. When using a crystal, connect a loading capacitor from each pin to GND. When using an oscillator, leave XTAL_OUT unconnected.
7	XTAL_IN	I/XT	25 MHz Crystal Oscillator Input Pin.

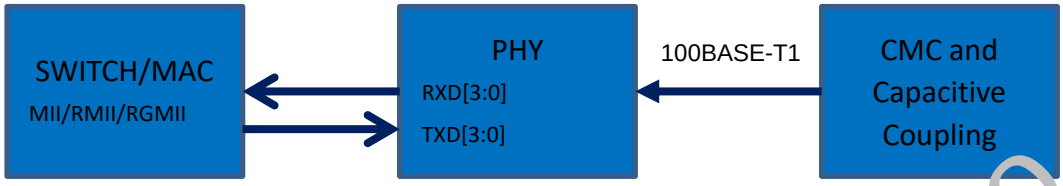
8	VDD33_MAIN	PWR, I	3.3V power for the main core.
9	RBIAS	Ana	Bias Resistor. A 2.4 kΩ±1% resistor is connected between the RBIAS pin and GND
10	AVDDL	PWR, I	1.2V power for the analog.
11	VDD33_DAC	PWR, I	3.3V power for the DAC.
12	TXP	Ana	Transmit/Receive Pairs . Differential data from copper media is transmitted and received on the single TRD± signal pair. There are 50Ω internal terminations on each pin. Since this device incorporates voltage driven DAC, it does not require a center-tap supply.
13	TXN	Ana	
14	WAKE	I,pd	WAKE. Active-high. When in sleep mode, transitioning the WAKE pin from low to high will cause the PHY to exit the sleep mode.
15	VDD33_AUX	PWR, I	3.3V power for the auxiliary domain. This pin supplies power to the passive signal detect circuitry and must remain powered with 3.3V.
16	INH	O	Inhibit. Output to be connected to the LDO supplying power to the PHY. When entering sleep mode, INH will be pulled low and will disable the LDO. When exit sleep mode, INH will be pulled high and will enable the LDO
17	EN	I,pd	EN. This pin is used in conjunction with INH to enable sleep mode or to provide a local wakeup from sleep mode
18	RX_DV/ Strapping[4]	IO,pd	Receive Data Valid. Active-high. RX_DV indicates that a receive frame is in progress and that the data present on the RXD output pins is valid. Strapping[4]. Used as power on strapping[4] bit when reset is active.
19	RXD[3]/ Strapping[3]	IO,pd	Receive Data Outputs. Byte-wide receive data output synchronous with the receive clock. RXD[3] is the most significant bit. Strapping[3]. Used as power on strapping[3] bit when reset is active.
20	RXD[2]/ Strapping[2]	IO,pd	Receive Data Outputs. Byte-wide receive data output synchronous with the receive clock. Strapping[2]. Used as power on strapping[2] bit when reset is active.

21	OVDD_RGMII	PWR, I	2.5V or 3.3V for RGMII IO. This pin is internally shorted with OVDD_RMII.
22	RXD[1]/ Strapping[1]	IO,pd	Receive Data Outputs. Byte-wide receive data output synchronous with the receive clock. Strapping[1]. Used as power on strapping[1] bit when reset is active.
23	RXD[0]/ Strapping[0]	IO,pd	Receive Data Outputs. Byte-wide receive data output synchronous with the receive clock. RXD[0] is the less significant bit. Strapping[0]. Used as power on strapping[0] bit when reset is active.
24	RXC	IO,pu	Receive Clock. 2.5M/25M output or input. This clock is used to synchronize the receive data outputs RXD[3:0]. The direction and frequency depend on MII mode and link mode.
25	OVDD_RMII	PWR, I	2.5V or 3.3V for RGMII IO. This pin is internally shorted with OVDD_RGMII.
26	TX_EN	I,ST	Transmit Enable. Active-high. When TX_EN is asserted, the data on the TXD pins is encoded and transmitted.
27	TXD[3]	I,pd	Transmit Data Input. Data is input synchronously with TXC clock.
28	TXD[2]	I,pd	Transmit Data Input. Data is input synchronously with TXC clock.
29	TXD[1]	I,pd	Transmit Data Input. Data is input synchronously with TXC clock.
30	TXD[0]	I,pd	Transmit Data Input. Data is input synchronously with TXC clock.
31	TXC	IO,pd	Transmit Clock. 2.5M/25M/50M output or input. This clock is used to synchronize the transmit data inputs TXD[3:0]. The direction and frequency depend on MII mode and link mode.
32	DVDDL	PWR, I	1.2V input for digital core
33	SYNC_IO	IO,pd	802.1AS Frame Sync event/sync pulse input or output
34	SYNC_IN	I, ST	802.1AS Frame Sync event/sync pulse input.
35	RESET_N	I,pu	RESET. Active-low, reset pin for chip.
36	MDIO	IO,pu	Management Data I/O. This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC.

4 FUNCTION DESCRIPTION

APPLICATION DIAGRAM

100BASE-T1 APPLICATION



MII INTERFACE

The Media Independent Interface (MII) is the digital data interface between the MAC and the physical layer that can be enabled when the device is functioning in 100BASE-T1 mode. The original MII transmit signals include TX_EN, TXC, TXD[3:0], and TX_ER. The receive signals include RX_DV, RXC, RXD[3:0], and RX_ER. The media status signals include CRS and COL. Due to pin-count limitations, the YT8010 supports a subset of MII signals. This subset includes all MII signals except TX_ER, RX_ER, CRS and COL.

RMII INTERFACE

Reduced media-independent interface (RMII) is a standard which was developed to reduce the number of signals required to connect a PHY to a MAC. If this interface is active, the number of data signal pins required to and from the MAC is reduced to half by clocking data on both the rising and falling edge of the transmit clock.

MANAGEMENT INTERFACE

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 25 MHz.

DAC

The digital-to-analog converter (DAC) transmits PAM3, MLT3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that reduces electromagnetic interference (EMI). The transmit DAC uses voltage driven output with internal terminations and hence does not require external components or magnetic supply for operation.

ADC

Each receive channel has its own analog-to-digital converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital data path.

ADAPTIVE EQUALIZER

The digital adaptive equalizer removes inter-symbol interference (ISI) created by the channel. The equalizer accepts sampled data from the analog-to-digital converter (ADC) on each channel and produces equalized data. The coefficients of the equalizer are adaptive to accommodate varying conditions of cable quality and cable length.

ECHO-CANCELLER

The echo impairment is caused on each channel because of the bidirectional transceiver in 100BASE-T1 mode. An echo canceller is added to remove this impairment from the ADC output. The echo canceler coefficients are adaptive to manage the varying echo impulse responses caused by different channels, transmitters, and environmental conditions.

CLOCK RECOVERY

The clock recovery block creates the transmit and receive clocks for 100BASE-T1. The two ends of the link perform loop timing. One end of the link is configured as the master, and the other is configured as the slave. The master transmit and receive clocks are locked to the 25 MHz crystal input. The slave transmit and receive clocks are locked to the incoming receive data stream. Loop timing allows for the cancellation of echo.

LINK MONITOR

Description about link status in different working mode.

In 100BASE-T1 mode, after receiver synchronizes to link partner's transmit signal and finishes local training process, local receive status will be good. Phy will monitor local receive status continuously. Local receive status should be good for at least 1.8us in 100BASE-T1 mode, then link monitor enters link pass status. Accordingly, if Local receive status is bad then link monitor enters link fail status immediately.

Link status can be read in mii reg address 0x1h, bit2.

POLARITY DETECTION AND AUTO CORRECTION

YT8010 can detect and correct two types of cable errors: swapping of pairs within the UTP cable and swapping of wires within a pair.

5 OPERATIONAL DESCRIPTION

RESET

YT8010 have a hardware reset pin(RESET_N) which is low active. RESET_N should be active for at least 5us to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up including wakeup from sleep mode.

RESET_N is also used as enable for power on strapping. During RESET_N is active, YT8010 latches input value on RX_DV and RXD[3:0] as strapping[4:0]. Strapping[4:0] is used as configuration information which provides flexibility in application without mdio access.

YT8010 also provides two software reset control registers which are used to reset all internal logic except some mdio configuration registers. For detailed information about what register will be reset by software reset, please refer to register table. Configure bit 15 of it's mii register(address 0x0) or mii register(address 0x0) to 1 to enable software reset. These two bits are self-clear after reset process is done.

PHY ADDRESS

For YT8010, Strapping[4] is used to generate phy address. Phy address is Strapping[4]+1. For example, If strapping[4] is 1'b1, then phy address is 2.

YT8010 and YT8050 always response to phy address 0. It also has another broadcast phy address which is configurable through mdio. Bit[4:0] of extended register(address 0x0) is broadcast phy address and its default value is 5'b11111. Bit[5] of extended register(address 0x0) is enable control for broadcast phy address and its default value is 1'b1.

XMII INTERFACE

YT8010 support 4 kinds of MII related interfaces: MII, RMII, RGMII and REMII.

MII

The Media Independent Interface (MII) is the digital data interface between the MAC and the physical layer that can be enabled when the device is functioning in 100BASE-T1 mode. The original MII transmit signals include TX_EN, TXC, TXD[3:0], and TX_ER. The receive signals include RX_DV, RXC, RXD[3:0], and RX_ER. The media status signals include CRS and COL. Due to pin-count limitations, the YT8010 supports a subset of MII signals. This subset includes all MII signals except TX_ER, RX_ER, CRS and COL. For 100M application, TXC and RXC are 25MHz; for 10M application, TXC and RXC are 2.5MHz. TXC and RXC are output in this case.

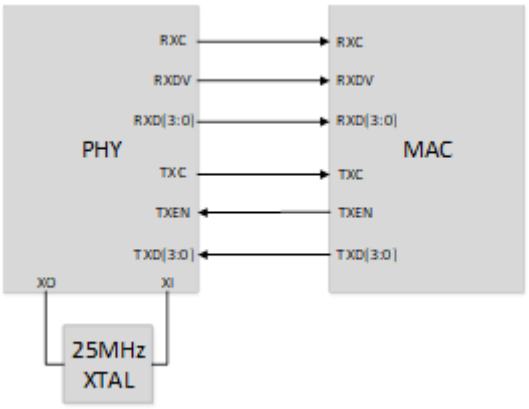


Figure . connection diagram of MII

RMII

Reduced media-independent interface (RMII) is a standard which was developed to reduce the number of signals required to connect a PHY to a MAC. If this interface is active, the number of data signal pins required to and from the MAC is reduced to half by doubling clock speed compared to MII. It has 7 signals: REF_CLK, TX_EN, TXD[1:0], RX_DV and RXD[1:0]. In YT8010/YT8050, we use TXC as REF_CLK. For 100M application, REF_CLK is 50MHz; for 10M application, REF_CLK is still 50MHz, data will be duplicated for 10 times in 20ns cycles. YT8010/ supports two types of connection method. 1. RMII1 mode: This is fully conforming to RMII standard. YT8010/YT8050 can use clock from TXC as reference clock for pll. In this case, 25MHz crystal at XI/XO is not needed. Configure bit 6 of extended register(address 0h50) to 1 to enable this feature. 2. RMII2 mode: TXC will be 50MHz output to MAC, this can save one 50MHz clock source.

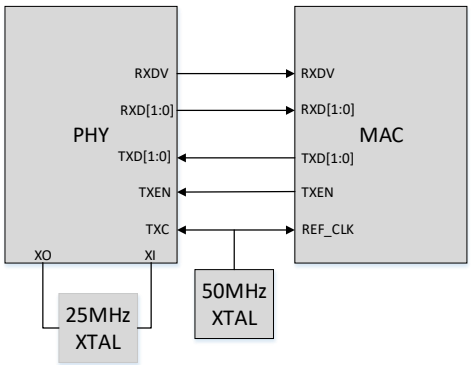


Figure .connection diagram of RMII1(with 25MHz and 50MHz clock)

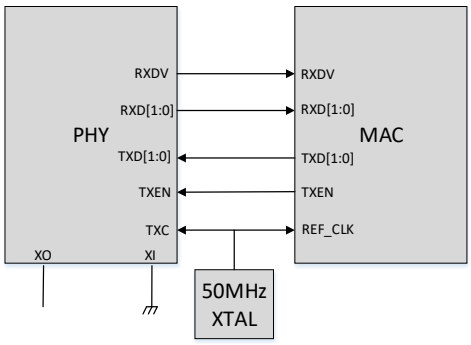


Figure .connection diagram of RMII1(with 50MHz clock only)

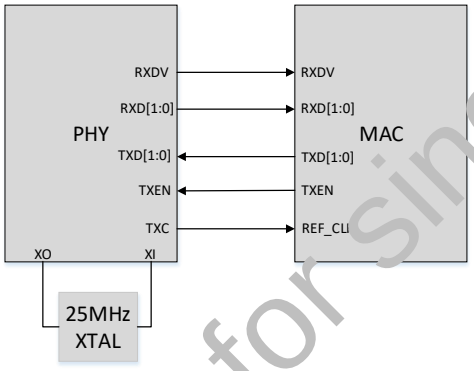


Figure .connection diagram of RMII2

RGMII

Reduced gigabit media independent interface is a subset of GMII which is used for gigabit Ethernet. For 100M/10M application, RGMII is similar to MII. The only difference is that tx_er/rx_er is transmitted by tx_en/rx_dv on the falling edge of clock. TXD[3:0] and RXD[3:0] will be duplicated on both rising and falling edge of clock. For 100M application, TXC and RXC are 25MHz; for 10M application, TXC and RXC are 2.5MHz.

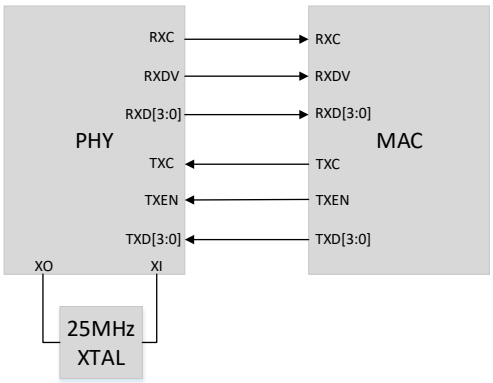


Figure .connection diagram of RGMII

REMII INTERFACE

Reverse media independent interface is the opposite of MII interface. The only difference is the direction of tx clock and rx clock. For MII, tx clock and rx clock are output; for REMII, tx clock and rx clock are input. REMII interface are used for back to back connection of two phys.

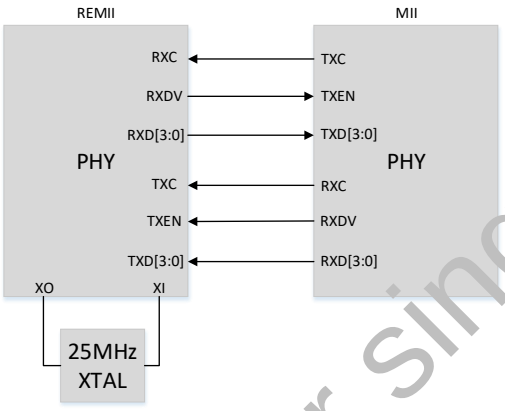


Figure .connection diagram of REMII

SQI

YT8010 provides a method to monitor quality of link.

By reading extended register mse(address 0h1005), we can obtain SNR during following steps.

a) Read register mse[14:0]

b) Calculate SNR = 10*log10(32768/(3*mse))

c) Average over 200 readings A= avg(SNR)

d) Rank the link quality

i. SQI = 5 when A > 23

ii. SQI = 4 when 18 < A < 23

iii. SQI = 3 when 15 < A < 18

iv. SQI = 2 when 15 < A < 18

v. SQI = 1 when 11 < A < 14

LOOPBACK MODE

There are three loopback modes in YT8010.

INTERNAL LOOPBACK

In Internal loopback mode, YT8010 feed transmit data to receive path in chip.

Configure bit 14 of mii register(address 0h0) to enable internal loopback mode. For 10Base-T and 100Base-Tx, YT8050 feeds digital dac data to adc directly. For HR10/HR100,

YT8010 feeds digital pcs transmit data to pcs receiver directly.

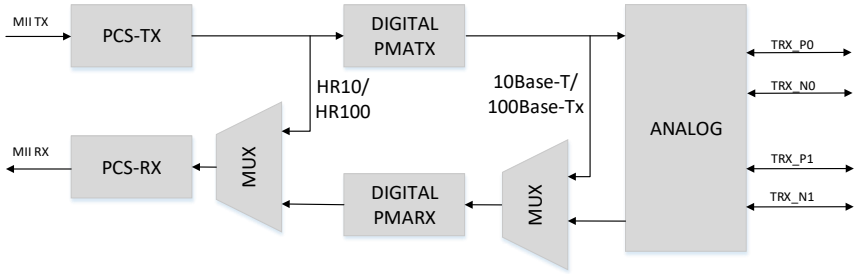


Figure . Internal loopback

EXTERNAL LOOPBACK

In external loopback mode, YT8010 feed transmit data to receive path out of chip. For 100 BASE-T1 configure bit 12 of extended register(address 0h4000) and just leave TRX_P0/N0 and TRX_P0/N0 unconnected.

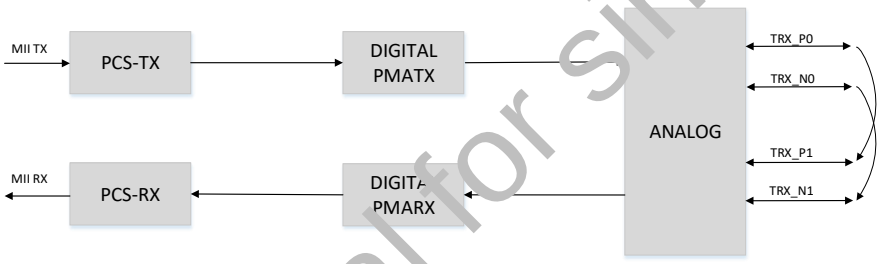


Figure . external loopback

REMOTE LOOPBACK

In remote loopback mode, YT8010 feed MII receive data to transmit path in chip. Configure bit 11 of extended register(address 0h4000) and for TRX interface, just connect to link partner normally.

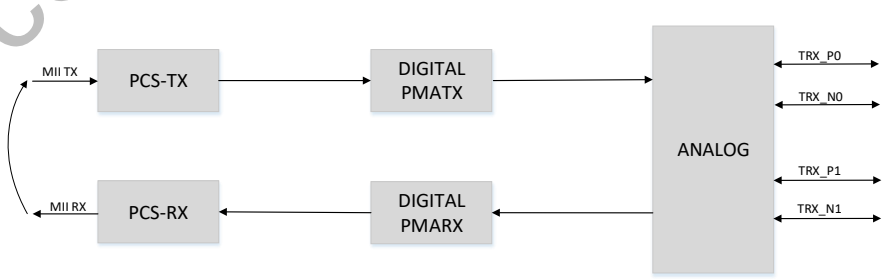


Figure . external loopback

MASTER-SLAVE CONFIGURATION

Master and slave configuration is from hardware strapping or in force mode, it comes from bit 3 of lds mii reg(address 0h0).

INTERRUPT

Interrupt shares same pin with LED.

Interrupt function can be selected by configuring bit 14 of extended register(address 0h4001). The polarity of interrupt is configurable by accessing bit 4 of mii reg(address 0h10).

Every interrupt has a corresponding mask bit and interrupt bit.

Please refer to mii register map(address 0h12, 0h13, 0h16 and 0h17) for detailed information.

POWER SAVING

YT8010 supports standby mode and sleep mode to save power.

In standby mode, PHY turn off analog ADC, DAC, and PLL. All digital logic is gated except MDIO register access. INH pin is high and power supply is still on. The link is down in standby mode, YT8010 can recover from standby mode rapidly. Write bit 11 of mii address 0x0h to 1'b1 to enter standby mode. To exit standby mode, write the same bit to 1'b0. In standby mode, the power consumption of YT8010 is less than mW.

In sleep mode, PHY turn off all power supply except always on 3.3v supply. The only working block is analog INH generation circle and power detect circle. In this mode, INH pin is low. There are three ways to enter sleep mode:

1. Pull down local EN pin from high.

2. Write bit12 of extended 0x1007 register.

3. Use TC10 standard to control remote phy to enter sleep mode.

There are also three ways to exit sleep mode:

1. Pull up local En pin from low.

2. Pull up local Wake pin from low.

3. Inject wake up signal which amplitude at txp/txn for more than 100us to wake up phy remotely.

Please refer to following chapter for detailed information about remote control. In sleep mode, the power consumption of YT8010 is lower than 50uw.

APPLICATION NOTES ABOUT SLEEP MODE

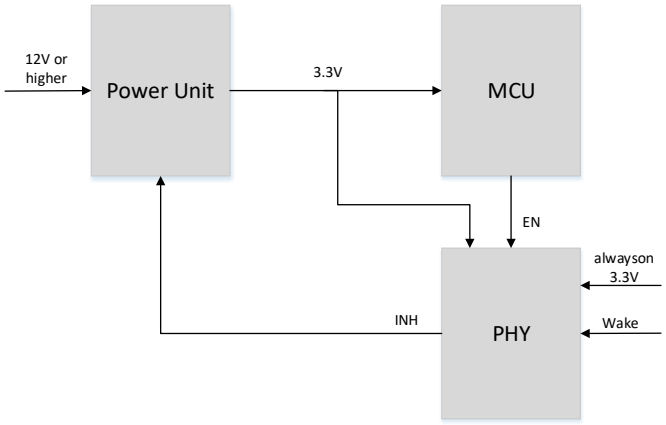


figure. Hardware connection description (MCU don't support Sleep and Wakeup function)

When MCU don't support sleep and wakeup function,YT8010 can take the responsibility of power control. If MCU decides to enter sleep mode,it can pull down EN pin or configure sleep_mode_en register through mdio, then INH goes down and power supply for MCU and phy will turn off except always on 3.3V power supply. The whole system can be wakeup remotely by injecting wakeup pulse on txp/txn or pulling up wake pin.

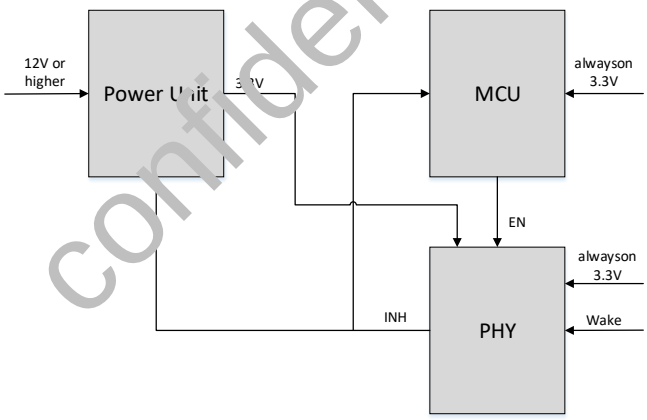


figure. Hardware connection description (MCU support Sleep and Wakeup function)

When MCU support sleep and wakeup function,INH pin only control the power supply of phy。If MCU decides to enter sleep mode， it can pull down En pin or configure sleep_mode_en register through mdio, then INH goes down and power supply for phy will

turn off except always on 3.3V power supply. MCU can pull up En/Wake pin to wakeup phy or phy will be wakeup remotely and send out a wake interrupt to MCU.

Following is an example of INH control application. Only AVDD_PPD is connected to always on 3.3V power and other power pins are controlled by INH pin.

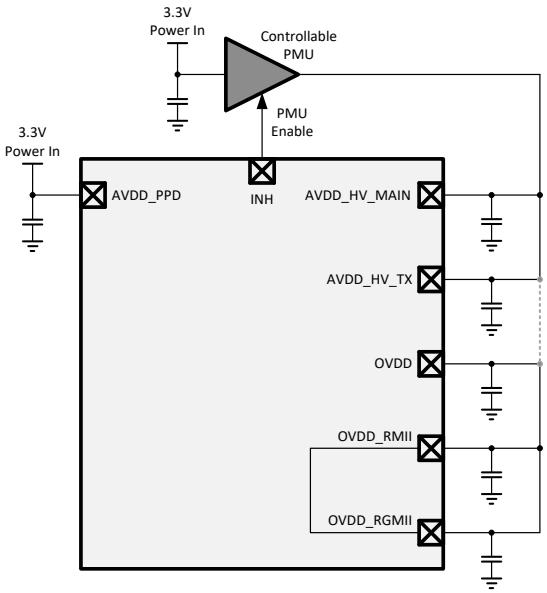


Figure. Power solution for INH control

SLEEP NEGOTIATION PROCESS

Following figure gives the state transition in sleep negotiation process。

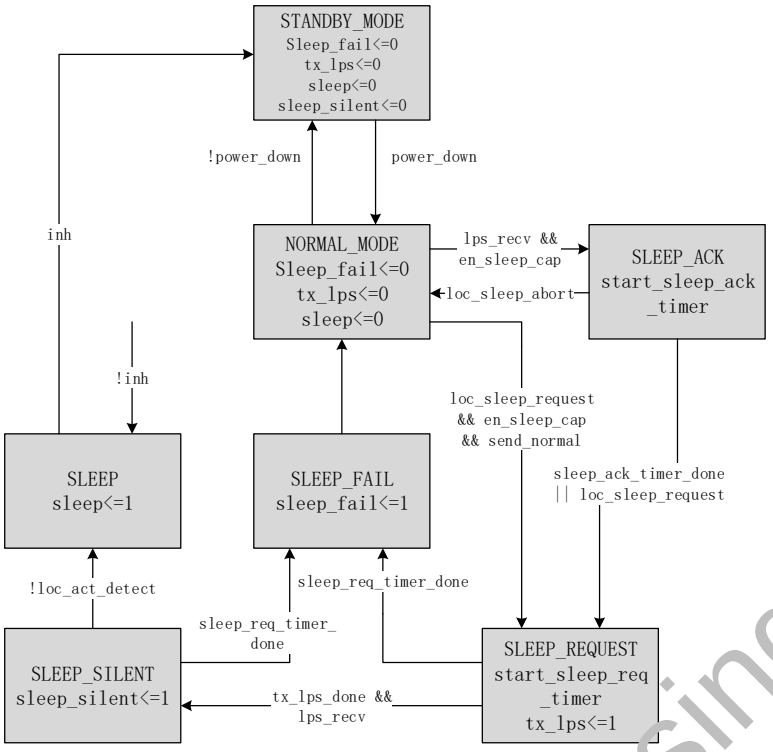


Figure. State diagram in sleep negotiation process

After YT8010 is power up，it enters standby mode。Power down register control the Translation between Standby mode and Normal mode。Default value of Power down register is zero，phy will enter normal mode directly without MCU。

Phy can start sleep negotiation process after link is set up between two phys.

Initiator configures loc_sleep_request register to start sleep negotiation process. Then Initiator enter SLEEP_REQUEST state and send LPS pattern and enable sleep_req_timer(16ms)。Responder receive LPS pattern and enter SLEEP_ACK state, enable sleep_ack_timer(8ms) and send out interrupt to MCU to inform that sleep request is received. In SLEEP_ACK state, phy wait response from MCU。MCU can accept the sleep request by configuring loc_sleep_request or reject by configuring loc_sleep_abort. If there is no response from MCU before sleep_ack_timer done, Responder will think sleep request is accepted and enter SLEEP_REQUEST state. If Responder rejects sleep request, Initiator will enter SLEEP_FAIL state after sleep_req_timer done and sleep negotiation process is done. If Responder accepts sleep request, Responder will send LPS pattern to inform initiator. After received LPS pattern from Responder, Initiator enters SLEEP_SILENT state and stops sending any signal on txp/txn and keeps checking signal energy on txp/txn. After the signal is gone, Initiator enters SLEEP_MODE state. In the meanwhile, Responser enters SLEEP_SILENT state after LPS pattern is sent and keeps checking signal energy

on txp/txn. After the signal is gone, Responder enters SLEEP_MODE state and sleep negotiation process is done.

Following figures give out the process of sleep negotiation.

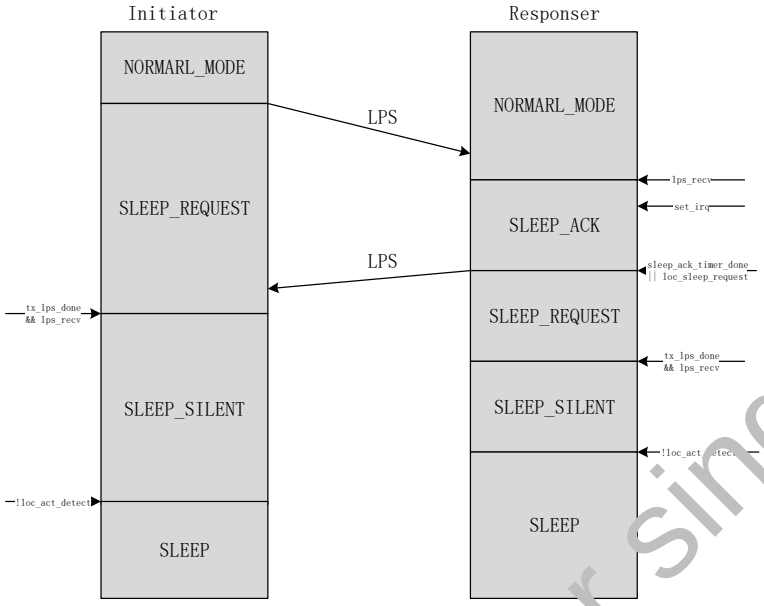


figure. Process of successful sleep negotiation

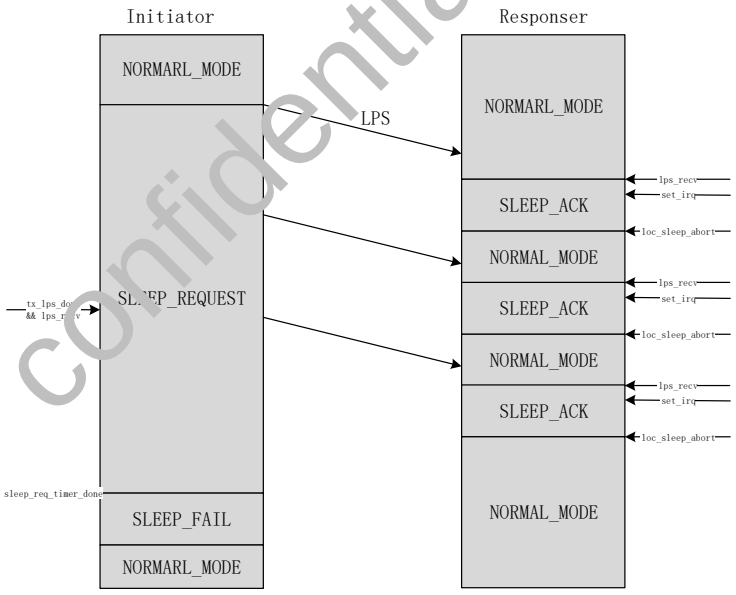


figure. Process of failed sleep negotiation

REMOTE WAKEUP

YT8010 can send wakeup pulse to wakeup link partner remotely if link partner support remote wakeup. YT8010 can also wakeup by wake up pulse sent by link partner.

To send out wakeup pulse to link partner, configure link_control to 0 and loc_wake_req to 1 in NORMARL_MODE. YT8010 will send 1ms wakeup pulse(IDLE symbol) to wake up link_partner。

If link is already setup， configure loc_wake_req to 1, YT8010 will send 128bits wake up request to link partner. YT8010 will send an interrupt to inform MCU after received wake up request from link partner.

6 REGISTER OVERVIEW

MII MANAGEMENT INTERFACE CLAUSE 22 REGISTER PROGRAMMING

The YT8010 transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification.

The MII management interface registers are written and read serially, using the MDIO and MDC pins.

A clock of up to 25 MHz must drive the MDC pin of the YT8010. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

MII REGISTERS

MII REGISTER 00H: BASIC CONTROL REGISTER

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	1’b0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically. 0: Normal operation 1: PHY reset
14	Loopback	RW SWC	1’b0	External loopback control 1’b0: disable loopback 1’b1: enable loopback

13	Speed_Selection(LSB)	RW	1’b1	LSB of speed_selection[1:0]. Link speed can be selected via either the Auto-Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto-Negotiation is disabled by clearing bit 0.12 to zero. Bit6 bit13 1 1 = Reserved 1 0 = 1000Mb/s 0 1 = 100Mb/s 0 0 = 10Mb/s
12	Autoneg_En	RW	1’b1	1: to enable auto-negotiation; 0: auto-negotiation is disabled.
11	Power_down	RW SWC	1’b0	1 = Power down 0 = Normal operation When the port is switched from power down to normal operation, software reset and Auto-Negotiation are performed even bit[15] RESET and bit[9] RESTART_AUTO_NEGOTIATION are not set by the user.
10	Isolate	RW SWC	1’b0	Isolate phy from MII/GMII/RGMII: PHY will not respond to RGMII TXD/TX_CTL, and present high impedance on RXD/RX_CTL. 1’b0: Normal mode 1’b1: Isolate mode
9	Re_Autoneg	RW SWS SC	1’b0	Auto-Negotiation automatically restarts after hardware or software reset regardelss of bit[9] RESTART. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Duplex_Mode	RW	1’b1	The duplex mode can be selected via either the Auto-Negotiation process or manual duplex selection. Manual duplex selection is allowed

				when Auto-Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0. 1 = Full Duplex 0 = Half Duplex
7	Collision_Test	RW SWC	1'b0	Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted. 1 = Enable COL signal test 0 = Disable COL signal test
6	Speed_ Selection(MSB)	RW	1'b1	See bit13.
5:0	Reserved	RO	5'b0	Reserved. Write as 0, ignore on read

MII REGISTER 01H: BASIC STATUS REGISTER

Bit	Symbol	Access	Default	Description
15	100Base-T4	RO	1'b0	PHY doesn't support 100BASE-T4
14	100Base-X_Fd	RO	1'b1	PHY supports 100BASE-X_FD
13	100Base-X_Hd	RO	1'b1	PHY supports 100BASE-X_HD
12	10Mbps_Fd	RO	1'b1	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	1'b1	PHY supports 10Mbps_Hd
10	100Base-T2_Fd	RO	1'b0	PHY doesn't support 100Base-T2_Fd
9	100Base-T2_Hd	RO	1'b0	PHY doesn't support 100Base-T2_Hd
8	Extended_Status	RO	1'b1	Whether support extended status register in 0Fh 0: Not supported 1: Supported

7	Unidirect_Ability	RO	1’b0	1’b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established 1’b1: PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	1’b1	1’b0: PHY will not accept management frames with preamble suppressed 1’b1: PHY will accept management frames with preamble suppressed
5	Autoneg_Complete	RO SWC	1’b0	1’b0: Auto-negotiation process not completed 1’b1: Auto-negotiation process completed
4	Remote_Fault	RO RC SWC LH	1’b0	1’b0: no remote fault condition detected 1’b1: remote fault condition detected
3	Autoneg_Ability	RO	1’b1	1’b0: PHY not able to perform Auto-negotiation 1’b1: PHY able to perform Auto-negotiation
2	Link_Status	RO LL SWC	1’b0	Link status 1’b0: Link is down 1’b1: Link is up
1	Jabber_Detect	RO RC LH SWC	1’b0	10Baset jabber detected 1’b0: no jabber condition detected 1’b1: Jabber condition detected
0	Extended_Capability	RO	1’b1	To indicate whether support extended registers, to access from address register 1Eh and data register 1Fh 1’b0: Not supported 1’b1: Supported

MII REGISTER 02H: PHY IDENTIFICATION REGISTER1

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	16'b0	Bits 3 to 18 of the Organizationally Unique Identifier

MII REGISTER 03H: PHY IDENTIFICATION REGISTER2

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	6'b0	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	6'h10	For motor phy, 33, for combo phy, 10
3:0	Revision_No	RO	4'h1	4 bits manufacturer's revision number

MII REGISTER 04H: AUTO-NEGOTIATION ADVERTISEMENT

Bit	Symbol	Access	Default	Description
15	Next_Page	RW	1'b0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down If 1000BASE-T is advertised, the required next pages are automatically transmitted. This bit must be set to 0 if no additional next page is needed. 1 = Advertise 0 = Not advertised

14	Ack	RO	1'b0	Always 0.
13	Remote_Fault	RW	1'b0	1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
12	Extended_Next_Page	RW	1'b1	Extended next page enable control bit 1 = Local device supports transmission of extended next pages 0 = Local device does not support transmission of extended next pages.
11	Asymmetric_Pause	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Asymmetric Pause 0 = No asymmetric Pause
10	Pause	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = MAC PAUSE implemented

				0 = MAC PAUSE not implemented
9	100BASE-T4	RO	1'b0	1 = Able to perform 100BASE-T4 0 = Not able to perform 100BASE-T4 Always 0
8	100BASE-TX_Full_Duplex	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
7	100BASE-TX_Half_Duplex	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised

6	10BASE-Te_Full_Duplex	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
5	10BASE-Te_Half_Duplex	RW	1'b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down 1 = Advertise 0 = Not advertised
4:0	Selector_Field	RW	5'b00001	Selector Field mode. 00001 = IEEE 802.3

MII REGISTER 05H: AUTO-NEGOTIATION LINK PARTNER ABILITY

Bit	Symbol	Access	Default	Description

15	1000Base-X_Fd	RO SWC	1'b0	Received Code Word Bit 15 1 = Link partner is capable of next page 0 = Link partner is not capable of next page
14	ACK	RO SWC	1'b0	Acknowledge. Received Code Word Bit 14 1 = Link partner has received link code word 0 = Link partner has not received link code word
13	REMOTE_FAULT	RO SWC	1'b0	Remote Fault. Received Code Word Bit 13 1 = Link partner has detected remote fault 0 = Link partner has not detected remote fault
12	RESERVED	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 12
11	ASYMMETRIC_PAUSE	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
10	PAUSE	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 10 1 = Link partner supports pause operation 0 = Link partner does not support pause operation
9	100BASE-T4	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 9 1 = Link partner supports 100BASE-T4 0 = Link partner does not support100BASE-T4
8	100BASE-TX_FULL_DUPLEX	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 8 1 = Link partner supports 100BASE-TX full-duplex

				0 = Link partner does not support 100BASE-TX full-duplex
7	100BASE-TX_HALF_DUPLEX	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 7 1 = Link partner supports 100BASE-TX half-duplex 0 = Link partner does not support 100BASE-TX half-duplex
6	10BASE-Te_FULL_DUPLEX	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 6 1 = Link partner supports 10BASE-Te full-duplex 0 = Link partner does not support 10BASE-Te full-duplex
5	10BASE-Te_HALF_DUPLEX	RO SWC	1'b0	Technology Ability Field. Received Code Word Bit 5 1 = Link partner supports 10BASE-Te half-duplex 0 = Link partner does not support 10BASE-Te half-duplex
4:0	SELECTOR_FIELD	RO SWC	5'h0	Selector Field Received Code Word Bit 4:0

MII REGISTER 06H: AUTO-NEGOTIATION EXPANSION REGISTER

Bit	Symbol	Access	Default	Description
15:5	Reserved	RO	11'h0	Always 0
4	Parallel_Detection_fault	RO RC LH SWC	1'b0	1 = Fault is detected 0 = No fault is detected
3	Link_partner_next_page able	RO LH SWC	1'b0	1 = Link partner supports Next page

				0 = Link partner does not support next page
2	Local_Next_Page_able	RO	1’b1	1 = Local Device supports Next Page 0 = Local Device does not Next Page
1	Page_received	RO RC LH	1’b0	1 = A new page is received 0 = No new page is received
0	Link_Partner_Auto_negotiation_able	RO	1’b0	1 = Link partner supports auto-negotiation 0 = Link partner does not support auto-negotiation

MII REGISTER 07H: AUTO-NEGOTIATION NEXT PAGE REGISTER

Bit	Symbol	Access	Default	Description
15	Next_Page	RW	1’b0	Transmit Code Word Bit 15 1 = The page is not the last page 0 = The page is the last page
14	Reserved	RO	1’b0	Transmit Code Word Bit 14
13	Message_page_mode	RW	1’b1	Transmit Code Word Bit 13 1 = Message Page 0 = Unformatted Page
12	Ack2	RW	1’b0	Transmit Code Word Bit 12 1 = Comply with message 0 = Cannot comply with message
11	Toggle	RO	1’b0	Transmit Code Word Bit 11 1 = This bit in the previously exchanged Code Word is logic 0 0 = The Toggle bit in the previously exchanged Code Word is logic 1

10:0	Message_Unformatte D_Field	RW	11'h1	Transmit Code Word Bits [10:0]. These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

MII REGISTER 08H: AUTO-NEGOTIATION LINK PARTNER RECEIVED NEXT PAGE REGISTER

Bit	Symbol	Access	Default	Description
15	Next_Page	RO	1'b0	Received Code Word Bit 15 1 = This page is not the last page 0 = This page is the last page
14	Reserved	RO	1'b0	Received Code Word Bit 14
13	Message_page_mode	RO	1'b0	Received Code Word Bit 13 1 = Message Page 0 = Unformatted Page
12	Ack2	RO	1'b0	Received Code Word Bit 12 1 = Comply with message 0 = Cannot comply with message
11	Toggle	RO	1'b0	Received Code Word Bit 11 1 = This bit in the previously exchanged Code Word is logic 0 0 = The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message_Unformatte D_Field	RO	11'b0	Received Code Word Bit 10:0 These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

MII REGISTER 0AH: MASTER-SLAVE STATUS REGISTER

Bit	Symbol	Access	Default	Description

15	Master_Slave_Configuration_Fault	RO RC SWC LH	1'b0	This register bit will clear on read, rising of MII 0.12 and rising of AN complete. 1 = Master/Slave configuration fault detected 0 = No fault detected
14	Master_Slave_Configuration_Resolution	RO	1'b0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Local PHY configuration resolved to Master 0 = Local PHY configuration resolved to Slave
13	Local_Receiver_Status	RO	1'b0	1 = Local Receiver OK 0 = Local Receiver not OK
12	Remote_Receiver_Status	RO	1'b0	1 = Remote Receiver OK 0 = Remote Receiver not OK
11	Link Partner_1000Base-T_Full_Duplex_Capability	RO	1'b0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Link Partner supports 1000BASE-T half duplex 0 = Link Partner does not support 1000BASE-T half duplex
10	Link_Partner_1000 Base-T_Half_Duplex_Capability	RO	1'b0	This bit is not valid unless register 0x1 bit5 is 1. 1 = Link Partner supports 1000Base-T full duplex 0 = Link Partner does not support 1000Base-T full duplex
9:8	Reserved	RO	2'b0	Always 0
7:0	Idle_Error_Count	RO SC	8'b0	MSB of Idle Error Counter. The register indicates the idle error count since the last read operation performed to this register. The counter pegs at 11111111 and does not roll over.

MII REGISTER 0DH: MMD ACCESS CONTROL REGISTER

Bit	Symbol	Access	Default	Description
15:14	Function	RW	2'b0	00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes

				11 = Data, post increment on writes only
13:5	Reserved	RO	9'b0	Always 0
4:0	DEVAD	RW	5'b0	MMD register device address. 00001 = MMD1 00011 = MMD3 00111 = MMD7

MII REGISTER 0EH: MMD ACCESS DATA REGISTER

Bit	Symbol	Access	Default	Description
15:0	Address_data	RW	16'b0	If register 0xD bits [15:14] are 00, this register is used as MMD DEVAD address register. Otherwise, this register is used as MMD DEVAD data register as indicated by its address register.

MII REGISTER 0FH: EXTENDED STATUS REGISTER

Bit	Symbol	Access	Default	Description
15	1000Base-X_Fd	RO	1'b0	PHY not able to support 1000Base-X_Fd
14	1000Base-X_Hd	RO	1'b0	PHY not able to support 1000Base-X_Hd
13	1000Base-T_Fd	RO	1'b0	PHY not able to support 1000Base-T_Fd
12	1000Base-T_Hd	RO	1'b0	PHY not able to support 1000Base-T_Hd
11:8	Reserved	RO	1'b0	Reserved
7	100Base-T1	RO	1'b1	PHY able to support 100Base-T1
6	1000Base-T1	RO	1'b0	PHY not able to support 1000Base-T1
5:0	Reserved	RO	6'b0	Reserved

MII REGISTER 10H: PHY SPECIFIC FUNCTION CONTROL REGISTER

Bit	Symbol	Access	Default	Description
15:7	Reserved	RO	9'b0	Always 0.
6:5	Cross_md	RW	2'b11	Changes made to these bits disrupt normal operation, thus a software reset is mandatory after the change. And the configuration does not take effect until software reset. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
4	Int_polar_sel	RW	1'b0	To control the polarity of interrupt PINs. 0 =when used as interrupt, INTn_LED is active LOW; 1 = when used as interrupt, INTn_LED is active HIGH.
3	Crs_on_tx	RW	1'b0	This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode: 1 = Assert CRS on transmitting or receiving 0 = Never assert CRS on transmitting, only assert it on receiving.
2	En_sqe_test	RW	1'b0	1 = SQE test enabled 0 = SQE test disabled Note: SQE Test is automatically disabled in full-duplex mode regardless the setting in this bit.
1	En_pol_inv	RW	1'b1	If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te. 1 = Polarity Reversal Enabled 0 = Polarity Reversal Disabled

0	Dis_jab	RW	1’b0	Jabber takes effect only in 10BASE-Te half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function

MII REGISTER 11H: PHY SPECIFIC STATUS REGISTER

Bit	Symbol	Access	Default	Description
15:14	Speed_mode	RO	2’b00	These status bits are valid only when any bit in bit9:7 and bit3:2 is 1. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	1’b0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
12	Page_Received_real-time	RO	1’b0	1 = Page received 0 = Page not received
11	Speed_and_Duplex_Resolved	RO	1’b0	When Auto-Negotiation is disabled, this bit is set to 1 for force speed mode. 1 = Resolved 0 = Not resolved
10	Link_status_real-time	RO	1’b0	1 = Link up 0 = Link down
9	En_fe_100	RO	1’b0	
8	En_fe_10	RO	1’b0	
7	Lds_en_autoneg	RO	1’b0	

6	MDI_Crossover_Status	RO	1'b0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. The bit value depends on register 0x10 "PHY specific function control register" bits6~bit5 configurations. Register 0x10 configurations take effect after software reset. 1 = MDIX 0 = MDI
5	Wirespeed_downgrade	RO	1'b0	1 = Downgrade 0 = No Downgrade
4	Reserved	RO	1'b0	Always 0.
3	En_ae_100	RO	1'b0	
2	En_ae_10	RO	1'b0	
1	Polarity_Real_Time	RO	1'b0	1 = Reverted polarity 0 = Normal polarity
0	Jabber_Real_Time	RO	1'b0	1 = Jabber is asserted. 0 = No jabber

MII REGISTER 12H: INTERRUPT MASK REGISTER

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation_Error_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
14	Speed_Changed_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
13	Duplex_changed_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
12	Page_Received_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
11	Link_Failed_int_mask	RW	1'b0	1 = Interrupt enable

				0 = Interrupt disable
10	Link_Succeed_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
9	IEEE1588_Misc_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
8	IEEE1588_Rx PTP_message_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
7	IEEE1588_Tx PTP_message_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
6	WOL_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
5	Wirespeed_downgraded_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
4:2	Reserved	RW	3'b0	No used.
1	Polarity_changed_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
0	Jabber_Happened_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable

MII REGISTER 13H: INTERRUPT STATUS REGISTER

Bit	Symbol	Access	Default	Description
15	Auto-Negotiation_Error_INT	RO RC	1'b0	Error can take place when any of the following happens: • MASTER/SLAVE does not resolve correctly • Parallel detect fault • No common HCD • Link does not come up after negotiation is complete • Selector Field is not equal

				• flp_receive_idle=true while Autoneg Arbitration FSM is in NEXT PAGE WAIT state 1 = Auto-Negotiation Error takes place 0 = No Auto-Negotiation Error takes place
14	Speed_Changed_INT	RO RC	1'b0	1 = Speed changed 0 = Speed not changed
13	Duplex_changed_INT	RO RC	1'b0	1 = duplex changed 0 = duplex not changed
12	Page_Received_INT	RO RC	1'b0	1 = Page received 0 = Page not received
11	Link_Failed_INT	RO RC	1'b0	1 = Link down takes place 0 = No link down takes place
10	Link_Succeed_INT	RO RC	1'b0	1 = Link up takes place 0 = No link up takes place
9	IEEE1588_Misc_INT	RO RC	1'b0	1 = IEEE1588 module's MISC interrupt happened 0 = IEEE1588 module's MISC interrupt didn't happen
8	IEEE1588_Rx PTP_message_INT	RO RC	1'b0	1 = PHY received 1588 message 0 = PHY didn't receive 1588 message
7	IEEE1588_Tx PTP_message INT	RO RC	1'b0	1 = PHY transmitted 1588 message 0 = PHY didn't transmit 1588 message
6	WOL_INT	RO RC	1'b0	1 = PHY received WOL magic frame. 0 = PHY didn't receive WOL magic frame.
5	Wirespeed_downgraded_INT	RO RC	1'b0	1 = speed downgraded. 0 = Speed didn't downgrade.
4:2	Reserved	RO RC	3'b0	Not used.
1	Polarity_changed_INT	RO RC	1'b0	1 = PHY revered MDI polarity 0 = PHY didn't revert MDI polarity

0	Jabber_Happened _INT	RO RC	1’b0	1 = 10BaseT TX jabber happened 0 = 10BaseT TX jabber didn’t happen

MII REGISTER 14H: SPEED AUTO DOWNGRADE CONTROL REGISTER

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	4’b0	Always 0.
11	En_mdio_latch	RW	1’b1	1 = To latch MII/MMD register’s read out value during MDIO read. 0 = Do not latch MII/MMD register’s read out value during MDIO read
10	Start_autoneg	RW SC	1’b0	Set it to cause PHY to restart auto-negotiation.
9	Reverse_autoneg	RW	1’b0	1 = reverse the autoneg direction, 10Mb/s has 1st priority, then 100Mb/s and at last 1000Mb/s. 0 = normal autoneg direction.
8	Dis_giga	RW	1’b0	1 = disable advertise Giga ability in autoneg; 0 = don’t disable, so PHY advertises Giga ability based on MII register 0x9.
7	Reserved	RW	1’b0	Shall always be written to 0. Writing this bit requires a software reset to update.
6	Reserved	RW	1’b0	Shall always be written to 0. Writing this bit requires a software reset to update.
5	En_speed_downgrade	RW	1’b1	When this bit is set to 1, the PHY enables smart-speed function. Writing this bit requires a software reset to update.
4:2	Autoneg retry limit pre-downgrade	RW	3’b011	If these bits are set to 3, the PHY attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits.

1	Bp_autospd_timer	RW	1'b0	1 = the wirespeed downgrade FSM will bypass the timer used for link stability check; 0 = not bypass the timer, then links that established but hold for less than 2.5s would still be taken as failure, autoneg retry counter will increase by 1.
0	Reserved	RO	1'b0	Always 0.

MII REGISTER 15H: RX ERROR COUNTER REGISTER

Bit	Symbol	Access	Default	Description
15:0	Rx_err_counter	RO	16'b0	This counter increase by 1 at the 1st rising of RX_ER when RX_DV is 1. The counter will hold at maximum 16'hFFFF and not roll over. If speed mode is 2'b01, it counts for fe_100 RX_ER. Else, it's 0.

MII REGISTER 16H: INTERRUPT MASK REGISTER 2

Bit	Symbol	Access	Default	Description
15:9	Reserved	RO	7'b0	Always 0.
8	Det_lds_pattern_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
7	Link_status_change_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
6	Loc_rcvr_status_change_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
5	Rem_rcvr_status_change_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
4	Training_failed_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable
3	LPS_recv_int_mask	RW	1'b0	1 = Interrupt enable 0 = Interrupt disable

2	Wake_recv_int_mask	RW	1’b0	1 = Interrupt enable 0 = Interrupt disable
1	Sleep_fail_int_mask	RW	1’b0	1 = Interrupt enable 0 = Interrupt disable
0	Over_heat_int_mask	RW	1’b0	1 = Interrupt enable 0 = Interrupt disable

MII REGISTER 17H: INTERRUPT STATUS REGISTER

Bit	Symbol	Access	Default	Description
15:9	Reserved	RO	7’b0	Reserved
8	Det_lds_pattern_int	RO RC	1’b0	
7	Link_status_change_int	RO RC	1’b0	
6	Loc_rcvr_status_change_int	RO RC	1’b0	
5	Rem_rcvr_status_change_int	RO RC	1’b0	
4	Training_failed_int	RO RC	1’b0	
3	LPS_recv_int	RO RC	1’b0	
2	Wake_recv_int	RO RC	1’b0	
1	Sleep_fail_int	RO RC	1’b0	
0	Over_heat_int	RO RC	1’b0	

MII REGISTER 1EH: DEBUG REGISTER’S ADDRESS OFFSET REGISTER

Bit	Symbol	Access	Default	Description
15:0	Extended_Register_Address _Offset	RW	16’h0	It’s the address offset of the extended register that will be Write or Read

MII REGISTER 1FH: DEBUG REGISTER’S DATA REGISTER

Bit	Symbol	Access	Default	Description
15:0	Extended_Register_Datas	RW	16’b0	It’s the data to be written to the extended register indicated by the address offset in

				register 0x1E, or the data read out from that debug register.

7 TIMING AND AC CHARACTERISTICS

8 POWER REQUIREMENTS

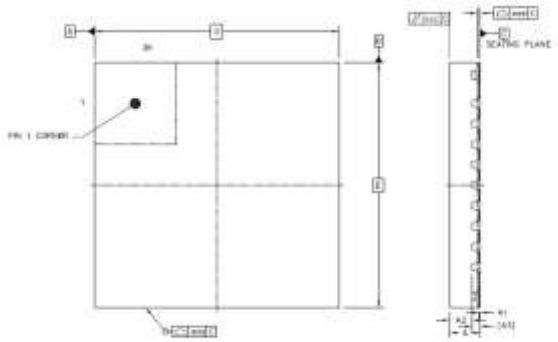
9 MECHANICAL AND THERMAL

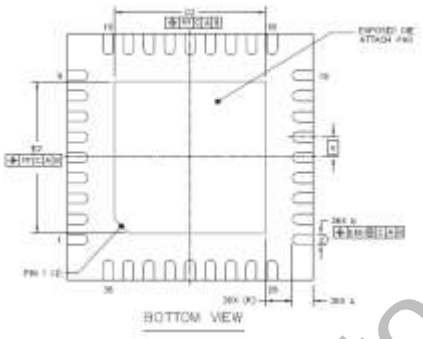
ROHS-COMPLIANT PACKAGING

Motor-comm offers an RoHS package that is compliant with RoHS

RoHS-compliant parts have the letter G added to the top line of the part marking.

MECHANICAL INFORMATION





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	----	0.55	----
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		6 BSC	
	Y	E		6 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	3.6	3.7	3.8
	Y	E2	3.6	3.7	3.8
LEAD LENGTH		L	0.4	0.5	0.6
LEAD TIP TO EXPOSED PAD EDGE		K		0.65 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

10 ORDERING INFORMATION

Part Number	Package	Status
YT8010XXXX	QFN36 6x6mm	
YT8010XXXX	QFN36 6x6mm	