REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29					
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Phu H. Nguyen

APPROVED BY
Thomas M. Hess

DRAWING APPROVAL DATE
09-10-01

REVISION LEVEL

MICROCIRCUIT, DIGITAL, LOW VOLTAGE CMOS, 3.3-V HIGH PERFORMANCE CLOCK SYNCHRONIZER AND JITTER CLEANER, MONOLITHIC SILICON

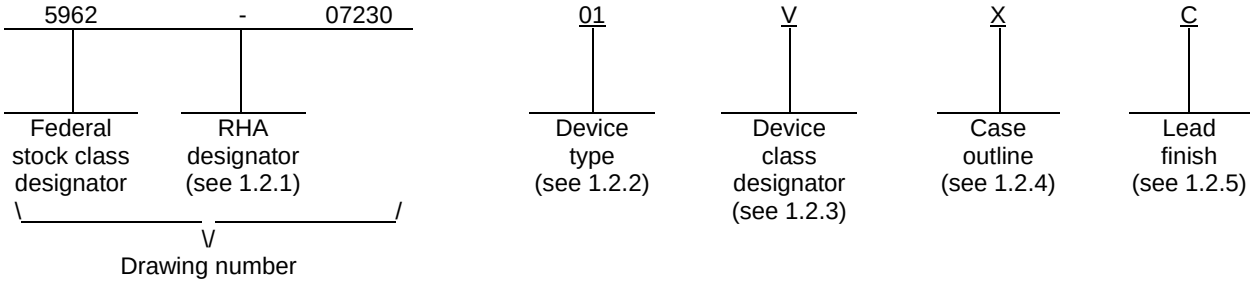
SIZE	CAGE CODE	
A	**67268**	**5962-07230**

SHEET 1 OF 29

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	CDCM7005M	3.3-V High performance clock synchronizer and jitter cleaner

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1.	52	Quad flat pack

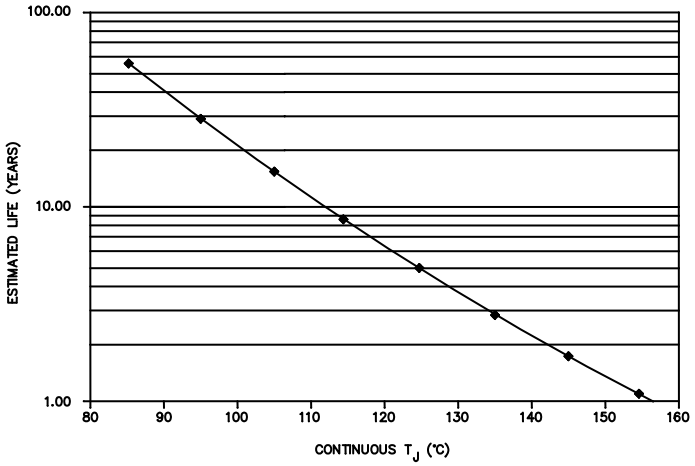
1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC}, A_{VCC}, V_{CC_CP}) ..... -0.5 V to 4.6 V 2/
Input voltage range (V_I) ..... -0.5 V to V_{CC} + 0.5 V 3/
Output voltage range (V_O) ..... -0.5 V to V_{CC} + 0.5 V 3/
Input current (I_{IN}) (V_{IN} < 0 V, V_{IN} > V_{CC}) ..... ±20 mA
Output current for LVPECL/LVCMOS outputs (I_O) (0 V < V_O < V_{CC}) ..... ±50 mA
Storage temperature range (T_{stg}) ..... -65°C to +150°C
Maximum junction temperature (T_J) ..... +125°C
Thermal resistance, junction-to-ambient ($R_{\theta JA}$) ..... 21.813°C/W 4/ 5/
Thermal resistance, junction-to-case ($R_{\theta JC}$) ..... 0.849°C/W 4/ 6/

1.4 Recommended operating conditions.

Supply voltage range:
V_{CC}, A_{VCC} ..... 3 V to 3.6 V
V_{CC_CP} ..... 2.3 V to V_{CC}
Maximum low-level input voltage, LVCMOS (V_{IL}) ..... 0.3 x V_{CC} 7/
Minimum high-level input voltage, LVCMOS (V_{IH}) ..... 0.7 x V_{CC} 7/
Maximum high-level output current, LVCMOS (I_{OH}) ..... -8 mA 8/
Maximum low-level output current, LVCMOS (I_{OL}) ..... 8 mA 8/
Input voltage range, LVCMOS (V_I) ..... 0 V to 3.6 V
Input amplitude range, LVPECL (V_{INPP}) ..... 0.5 V to 1.3 V 9/
Common-mode input voltage range, LVPECL (V_{IC}) ..... 1 V to V_{CC} – 0.3 V
Operating case temperature range (T_C) ..... -55°C to +125°C



OPERATING LIFE DERATING CHART

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those under recommended operating conditions are not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. See operating life derating chart above.
2/ All supply voltages have to be supplied at the same time.
3/ The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
4/ Connected to GND with nine thermal vias (0.3 mm diameter).
5/ Board mounted, per JESD51-5.
6 Per MIL-STD-883 method 1012.
7/ V_{IL} and V_{IH} are required to maintain ac specifications; the actual device function tolerates a smaller input level of 1 V, if an ac-coupling to V_{CC}/2 is provided.
8/ Includes all status pins.
9/ V_{INPP} minimum and maximum are required to maintain ac specifications; the actual device function tolerates a minimum V_{INPP} of 150 mV.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of documents are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JESD51-5 - Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms

(Applications for copies should be addressed to the Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834 or online at http://www.jedec.org.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms and load circuit. The timing waveforms and load circuit shall be as specified on figures 4 - 14.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Overall Device Characteristics							
Supply current (I_{CC} over frequency) 2/	I_{CC_LVPECL}	f_{VCXO} = 200 MHz, f_{REF_IN} = 25 MHz, PFD = 195.3125 kHZ, I_{CP} = 2 mA, All outputs are LVPECL and Div-by-8. For load, see figure 5.	1, 2, 3	All		260	mA
	I_{CC_LVCMOS}	f_{VCXO} = 200 MHz, f_{REF_IN} = 25 MHz, PFD = 195.3125 kHZ, I_{CP} = 2 mA, All outputs are LVCMOS and Div-by-8. Load = 10 pF.	1, 2, 3	All		160	mA
Power-down current	I_{CCPD}	f_{IN} = 0 MHz, V_{CC} = 3.6 V, AV_{CC} = 3.6 V, V_{CC_CP} = 3.6V, V_I = 0 V or V_{CC}	1, 2, 3	All		300	µA
High-impedance state output current for Yx outputs	I_{OZ}	V_O = 0 V or V_{CC} – 0.8 V	1, 2, 3	All		±40	µA
		V_O = 0 V or V_{CC}				±100	
Voltage on I_REF_CP (external current path for accurate charge pump current)	$V_{I\_REF\_CP}$	12 kΩ to GND at pin 49.	1, 2, 3	All	1.114	1.326	V
Output reference voltage	V_{BB}	V_{CC} = 3 V to 3.6 V; I_{BB} = -0.2 mA	1, 2, 3	All	V_{CC} – 1.446	V_{CC} – 1.090	V
Output capacitance for Yx	C_O	V_{CC} = 3.3 V, V_O = 0 V or V_{CC}	4	All	3 TYP 3/		pF
Input capacitance at PRI_REF and SEC_REF	C_I	V_I = 0 V or V_{CC}	4	All	3.6 TYP 3/		pF
Input capacitance at CTRL_LE, CTRL_CLOCK, and CTRL_DATA		V_I = 0 V or V_{CC}			3 TYP 3/		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
LVCMOS Device Characteristics							
Output frequency 4/ 5/ 6/	f_{clk}	Load = 5 pF to GND, 1 kΩ to V_{CC}, 1 kΩ to GND	9, 10, 11	All	240 TYP 3/		MHz
LVCMOS input clamp voltage	V_{IK}	V_{CC} = 3 V, I_I = -18 mA	1, 2, 3	All		-1.2	V
LVCMOS input current for CTRL_LE, CTRL_CLOCK and CTRL_DATA	I_I	V_I = 0 V or V_{CC}, V_{CC} = 3.6 V	1, 2, 3	All		±5	µA
LVCMOS input current for PD, RESET, HOLD REF_SEL, PRI_REF, and SEC_REF 7/	I_{IH}	V_I = V_{CC}, V_{CC} = 3.6 V	1, 2, 3	All		5	µA
LVCMOS input current for PD, RESET, HOLD REF_SEL, PRI_REF, and SEC_REF 7/	I_{IL}	V_I = 0 V, V_{CC} = 3.6 V	1, 2, 3	All	-15	-35	µA
High-level output voltage for LVCMOS outputs	V_{OH}	V_{CC} = 3 V to 3.6 V, I_{OH} = -100 µA	1, 2, 3	All	V_{CC} – 0.1		V
		V_{CC} = 3 V, I_{OH} = -6 mA			2.4		
		V_{CC} = 3 V, I_{OH} = -12 mA			2		
Low-level output voltage for LVCMOS outputs	V_{OL}	V_{CC} = 3 V to 3.6 V, I_{OL} = 100 µA	1, 2, 3	All		0.1	V
		V_{CC} = 3 V, I_{OL} = 6 mA				0.5	
		V_{CC} = 3 V, I_{OL} = 12 mA				0.8	
High-level output current	I_{OH}	V_{CC} = 3.3 V, V_O = 1.65 V	1, 2, 3	All	-50	-20	mA
Low-level output current	I_{OL}	V_{CC} = 3.3 V, V_O = 1.65 V	1, 2, 3	All	20	50	mA
Phase offset (REF_IN to Y output) 8/	t_{pho}	VREF_IN = V_{CC}/2, Y = V_{CC}/2 See figure 8, Load = 10 pF	9, 10, 11	All	2.7 TYP 3/		ns
LVCMOS pulse skew 9/	$t_{sk(p)}$	Crosspoint to V_{CC}/2 load. See figure 10.	9, 10, 11	All	160 TYP 3/		ps
Propagation delay from VCXO_IN to Yx 9/	$t_{pd(LH)}$, $t_{pd(HL)}$	Crosspoint to V_{CC}/2, Load = 10 pF, See figure 10 (PLL bypass mode).	9, 10, 11	All	2.8 TYP 3/		ns
LVCMOS single-ended output skew 9/ 10/	$t_{sk(o)}$	All outputs have the same divider ratio.	9, 10, 11	All	80 TYP 3/		ps
		Outputs have different divider ratios.			80 TYP 3/		
Duty cycle, LVCMOS		V_{CC}/2 to V_{CC}/2	9, 10, 11	All	49%	51%	
Output rise/fall slew rate	$t_{slew-rate}$	20% to 80% of swing For load, see figure 10.	9, 10, 11	All	3.5 TYP 3/		V/ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
LVPECL Device Characteristics							
Output frequency 5/ 11/	f_{clk}	For load, see figure 5.	9, 10, 11	All	2000 TYP 3/		MHz
LVPECL input current	I_I	V_I = 0 V or V_{CC}	1, 2, 3	All		±20	µA
LVPECL high-level output voltage	V_{OH}	For load, see figure 5.	1, 2, 3	All	V_{CC} – 1.18	V_{CC} – 0.81	V
LVPECL low-level output voltage	V_{OL}	For load, see figure 5.	1, 2, 3	All	V_{CC} – 2	V_{CC} – 1.55	V
Differential output voltage	$\|V_{OD}\|$	See figure 12. For load, see figure 5.	1, 2, 3	All	500		mV
Phase offset (REF_IN to Y output) 10/	t_{pho}	VREF_IN = V_{CC}/2 to cross point of Y. See figure 8.	9, 10, 11	All	250 TYP 3/		ps
Propagation delay time, VXCO_IN to Yx 9/	$t_{pd(LH)}$, $t_{pd(HL)}$	Cross point-to-cross point. For load, see figure 5.	9, 10, 11	All	615 TYP 3/		ps
LVPECL pulse skew 9/	$t_{sk(p)}$	Cross point-to-cross point. For load, see figure 5.	9, 10, 11	All	15 TYP 3/		ps
LVPECL output skew 10/	$t_{sk(o)}$	All outputs have the same divider ratio. For load, see figure 5.	9, 10, 11	All	20 TYP 3/		ps
		Outputs have different divider ratios. For load, see figure 5.			50 TYP 3/		
Rise and fall time	t_r / t_f	20% to 80% of V_{OUTPP} See figure 12.	9, 10, 11	All	170 TYP 3/		ps
Input capacitance at VXCO_IN, VXCO_IN	C_I		4	All	2.5 TYP 3/		pF
LVCMOS-to-LVPECL Device Characteristics							
Output skew between LVCMOS and LVPECL outputs 9/ 12/	$t_{sk(P\_C)}$	Cross point to V_{CC}/2. For load, see figure 5 and figure 10.	9, 10, 11	All		3.2	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
PLL Analog Lock Device Characteristics							
High-level output current	I_{OH}	V_{CC} = 3.6 V, V_O = 1.8 V	1, 2, 3	All	-150	-80	µA
Low-level output current	I_{OL}	V_{CC} = 3.6 V, V_O = 1.8 V	1, 2, 3	All	80	150	µA
High-impedance state output current for PLL LOCK output 13/	$I_{OZH\ LOCK}$	V_O = 3.6 V ($\overline{PD}$ is set low)	1, 2, 3	All		65	µA
High-impedance state output current for PLL LOCK output 13/	$I_{OZL\ LOCK}$	V_O = 0 V ($\overline{PD}$ is set low)	1, 2, 3	All		±5	µA
Positive input threshold voltage	V_{IT+}	V_{CC} = 3 V to 3.6 V	1, 2, 3	All	(V_{CC} x 0.55) TYP 3/		V
Negative input threshold voltage	V_{IT-}	V_{CC} = 3 V to 3.6 V	1, 2, 3	All	(V_{CC} x 0.35) TYP 3/		V
Phase Detector Device Characteristics							
Maximum charge pump frequency	f_{CPmax}	Default PFD pulse width delay	9, 10, 11	All	100 TYP 3/		MHz
Charge Pump Device Characteristics							
Charge pump sink/source current range 14/	I_{CP}	V_{CP} = 0.5 V_{CC_CP}	1, 2, 3	All	±0.2	±3.9	mA
Charge pump three-state current	I_{CP3St}	0.5 V < V_{CP} < V_{CC_CP} – 0.5 V	1	All	-10	10	nA
			2, 3		-50	50	
ICP absolute accuracy	I_{CPA}	V_{CP} = 0.5 V_{CC_CP}, internal reference resistor, SPI default settings	1, 2, 3	All	-20%	20%	
		V_{CP} = 0.5 V_{CC_CP}, external reference resistor 12 kΩ (1%) at I_REF_CP, SPI default settings			5% TYP 3/		
Sink/source current matching	I_{CPM}	0.5 V < V_{CP} < V_{CC_CP} – 0.5 V, SPI default settings	1, 2, 3	All	-7%	7%	
ICP vs VCP matching	I_{VCPM}	0.5 V < V_{CP} < V_{CC_CP} – 0.5 V	1, 2, 3	All	-10%	10%	
PRI_REF/SEC_REF_IN Timing Requirements							
LVCMOS primary or secondary reference clock frequency 15/ 16/	f_{REF_IN}		9, 10, 11	All	0	200	MHz
Rise and fall time of PRI_REF or SEC_REF signals from 20% to 80% of V_{CC}	t_r / t_f		9, 10, 11	All		4	ns
Duty cycle of PRI_REF or SEC_REF at V_{CC}/2	dutyREF		9, 10, 11	All	40%	60%	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
VCXO_IN, $\overline{\text{VCXO\_IN}}$ Timing Requirements							
VCXO clock frequency 17/	f_{VCXO_IN}		9, 10, 11	All	2000 TYP 3/		MHz
Rise and fall time 20% to 80% of V_{INPP} at 80 MHz to 800 MHz 18/	t_r / t_f		9, 10, 11	All		3	ns
Duty cycle of VCXO clock	dutyVCXO		9, 10, 11	All	40%	60%	
SPI/Control Timing Requirements							
CTRL_CLK frequency	f_{CTRL_CLK}	See figure 14.	9, 10, 11	All		20	MHz
CTRL_DATA to CTRL_CLK setup time	t_{su1}		9, 10, 11	All	10		ns
CTRL_DATA to CTRL_CLK hold time	t_{h2}		9, 10, 11	All	10		ns
CTRL_CLK high duration	t_3		9, 10, 11	All	25		ns
CTRL_CLK low duration	t_4		9, 10, 11	All	25		ns
CTRL_LE to CTRL_CLK setup time	t_{su5}		9, 10, 11	All	10		ns
CTRL_CLK to CTRL_LE setup time	t_{su6}		9, 10, 11	All	10		ns
CTRL_LE pulse width	t_7		9, 10, 11	All	20		ns
Rise and fall time of CTRL_DATA, CTRL_CLK, and CTRL_LE signals from 20% to 80% of V_{CC}	t_r / t_f		9, 10, 11	All		4	ns
$\overline{\text{PD}}$, $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$, REF_SEL Timing Requirements							
Rise and fall time of the $\overline{\text{PD}}$, $\overline{\text{RESET}}$, $\overline{\text{HOLD}}$, and REF_SEL signals from 20% to 80% of V_{CC}	t_r / t_f		9, 10, 11	All		4	ns

See footnotes on next sheet.

TABLE I. Electrical performance characteristics - Continued.

1/ Tested over recommended operating free-air temperature range at recommended ranges of supply voltage and load.

2/ See figure 4-1 through figure 4-4.

3/ All typical values are at V_{CC} = 3.3 V, temperature (T_C) = +25°C.

4/ f_{clk} can be up to 400 MHz in the typical operating mode (+25°C / 3.3 V V_{CC}).

5/ Operating the LVCMOS or LVPECL output above the maximum frequency will not cause a malfunction to the device, but the output signal swing may no longer meet the output specification.

6/ See figure 6 and figure 7.

7/ These inputs have an internal 150 kΩ pull-up resistor.

8/ This is valid only for the same frequency of REF_IN clock and Y output clock. It can be adjusted by the SPI controller (reference delay M and VCXO delay N).

9/ See figure 9.

10/ The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.

11/ See figure 11.

12/ The phase of LVCMOS is lagging in reference to the phase of LVPECL.

13/ Lock output has an 80 kΩ pull-down resistor.

14/ Defined by SPI settings.

15/ At Reference Clock less than 2 MHz, the device stays in normal operation mode but the frequency detection circuitry resets the STATUS_REF signal to low. In this case, the status of the STATUS_REF is no longer relevant.

16/ f_{REF_IN} can be up to 250 MHz in typical operating mode (+25°C / 3.3 V V_{CC}).

17/ If the Feedback Clock (derived from VCXO input) is less than 2 MHz, the device stays in normal operation mode but the frequency detection circuitry resets the STATUS_VCXO signal and PLL_LOCK signal to low. Both status signals are no longer relevant. This affects the HOLD-over function as well, as the PLL_LOCK signal is no longer valid.

18/ use a square-wave for lower frequencies (< 80 MHz).

Case X

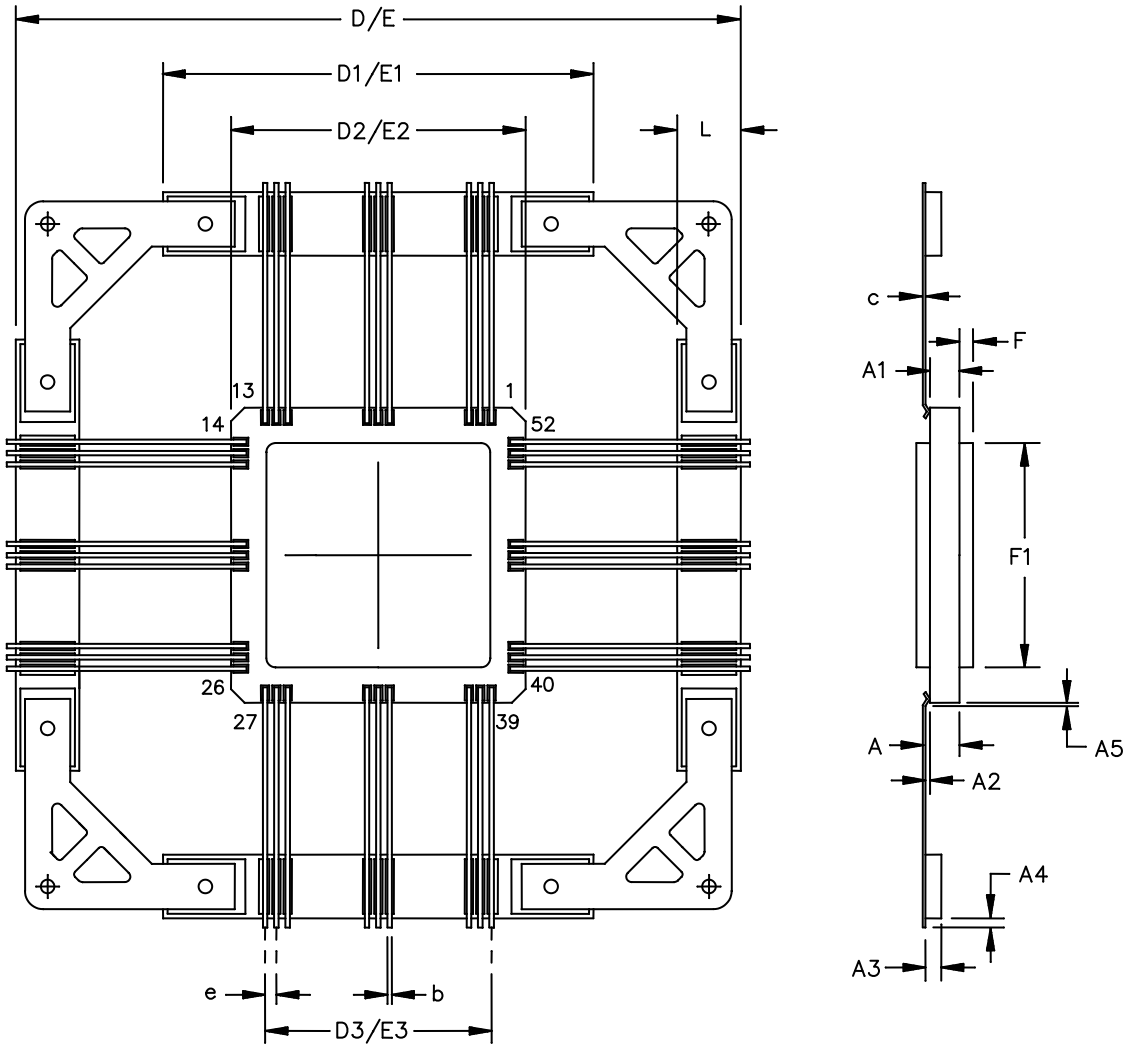


FIGURE 1. Case outline.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-07230
		REVISION LEVEL	SHEET 12

Case X

Dimensions	Inches		Millimeters	
	Min	Max	Min	Max
A	---	0.105	---	2.68
A1	---	0.090	---	2.29
A2	0.002	0.014	0.05	0.36
A3	0.030	0.040	0.76	1.02
A4	---	0.020	---	0.51
A5	---	0.018	---	0.46
b	0.006	0.010	0.15	0.25
c	0.004	0.008	0.10	0.20
D/E	1.584	1.616	40.23	41.05
D1/E1	0.940	0.960	23.88	24.38
D2/E2	0.542	0.558	13.77	14.17
D3/E3	0.300 BSC		7.62 BSC	
e	0.025 NOM		0.64 NOM	
F	0.030 NOM		0.76 NOM	
F1	0.394 NOM		10.00 NOM	
L	0.125	0.145	3.18	3.68

NOTES:

1. All linear dimensions are in inches (millimeters equivalents are for reference only).
2. This package is a ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
3. This package is hermetically sealed with a metal lid.
4. The leads are gold plated and can be solder dipped.
5. All leads are not shown for clarity purposes.
6. Lid and heatsink are connected to GND leads.

FIGURE 1. Case outline - Continued.

Device type:	All		
Case outline:	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	27	$\overline{PD}$
2	CTRL_DATA	28	V_{CC}
3	AV_{CC}	29	Y1A
4	CTRL_CLK	30	Y1B
5	CTRL_LE	31	V_{CC}
6	AV_{CC}	32	V_{CC}
7	GND	33	Y2A
8	CP_OUT	34	Y2B
9	AV_{CC}	35	V_{CC}
10	VCC_SP	36	V_{CC}
11	GND	37	Y3A
12	REF_SEL	38	Y3B
13	GND	39	V_{CC}
14	PRI_REF	40	$\overline{RESET}$ or $\overline{HOLD}$
15	SEC_REF	41	V_{CC}
16	AV_{CC}	42	Y4A
17	AV_{CC}	43	Y4B
18	V_{BB}	44	V_{CC}
19	V_{CC}	45	GND
20	$\overline{VCXO\_IN}$	46	V_{CC}
21	VCXO_IN	47	V_{CC}
22	V_{CC}	48	V_{CC}
23	V_{CC}	49	STATUS_VCXO or I_REF_CP
24	Y0A	50	STATUS_REF or PRI_SEC_CLK
25	Y0B	51	GND
26	V_{CC}	52	PLL_LOCK

FIGURE 2. Terminal connections.

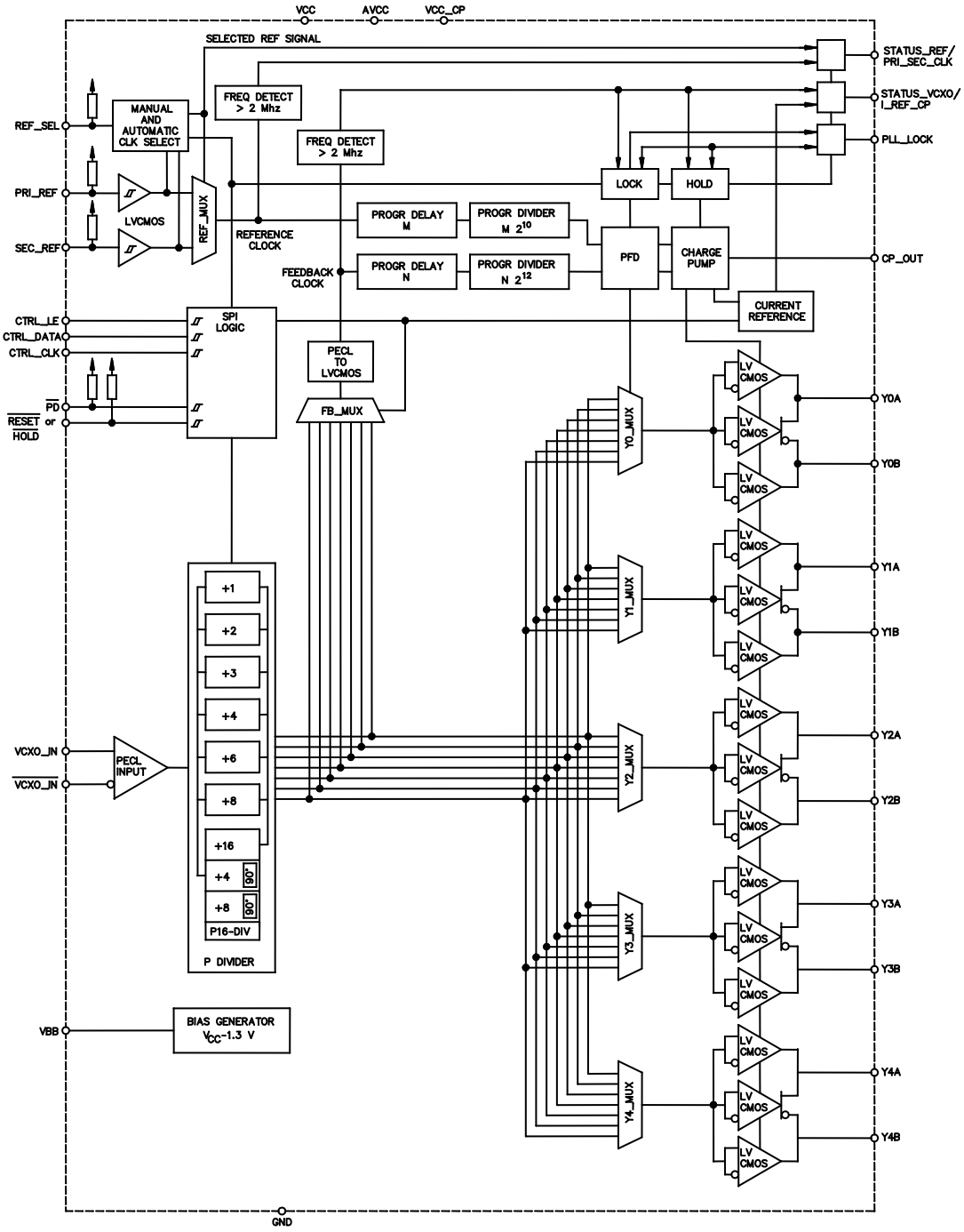
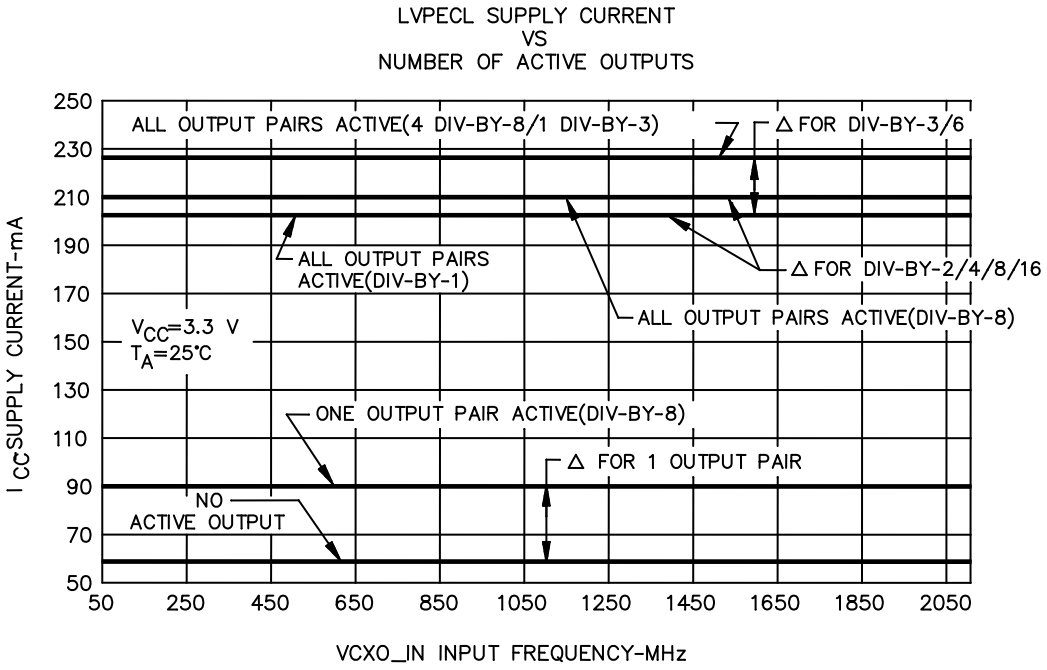


FIGURE 3. Functional block diagram.



NOTE: If div-by-2/4/8/16 is activated for one or more outputs, 'Δ for div-by-2/4/8/16' has to be added to I_{CC} of div-by-1. If div-by-3 or div-by-6 is activated, 'Δ for div-by-2/4/8/16' and 'Δ for div-by-3/6' has to be added to I_{CC} of div-by-1.

FIGURE 4-1. Timing waveforms and load circuits.

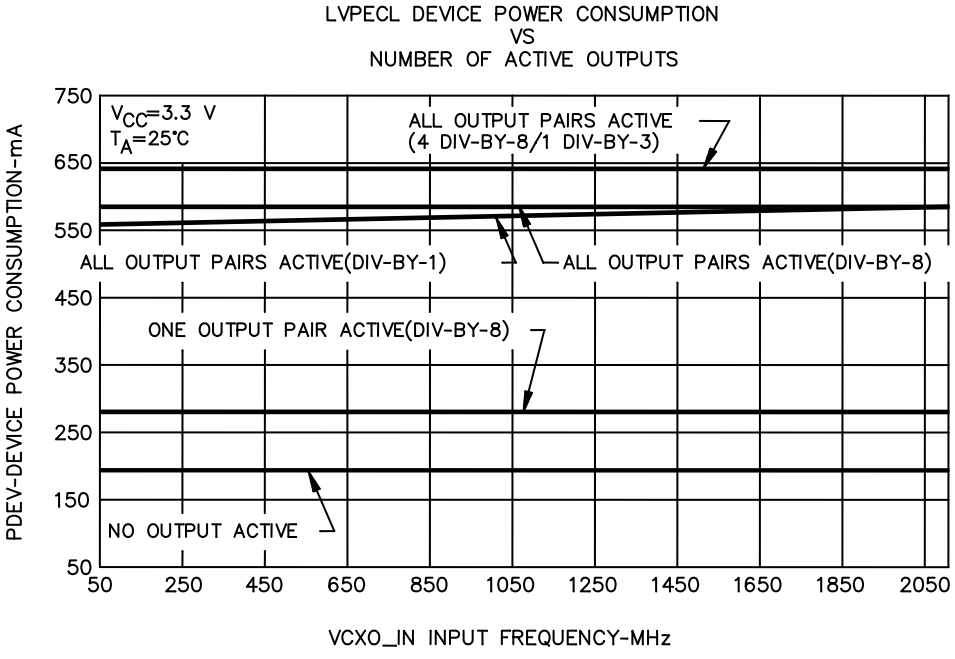
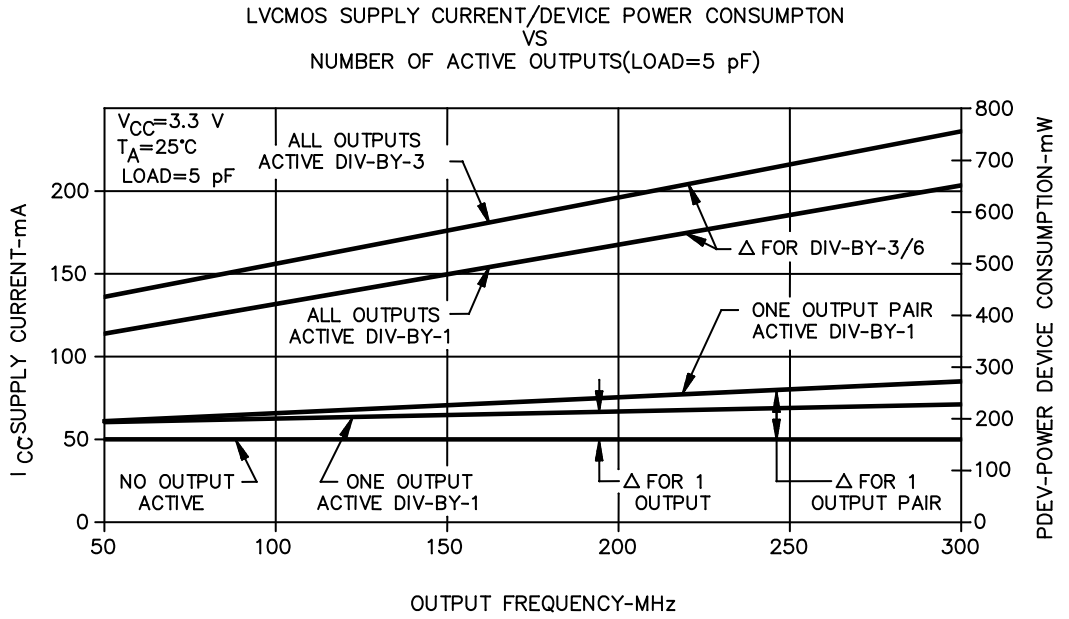
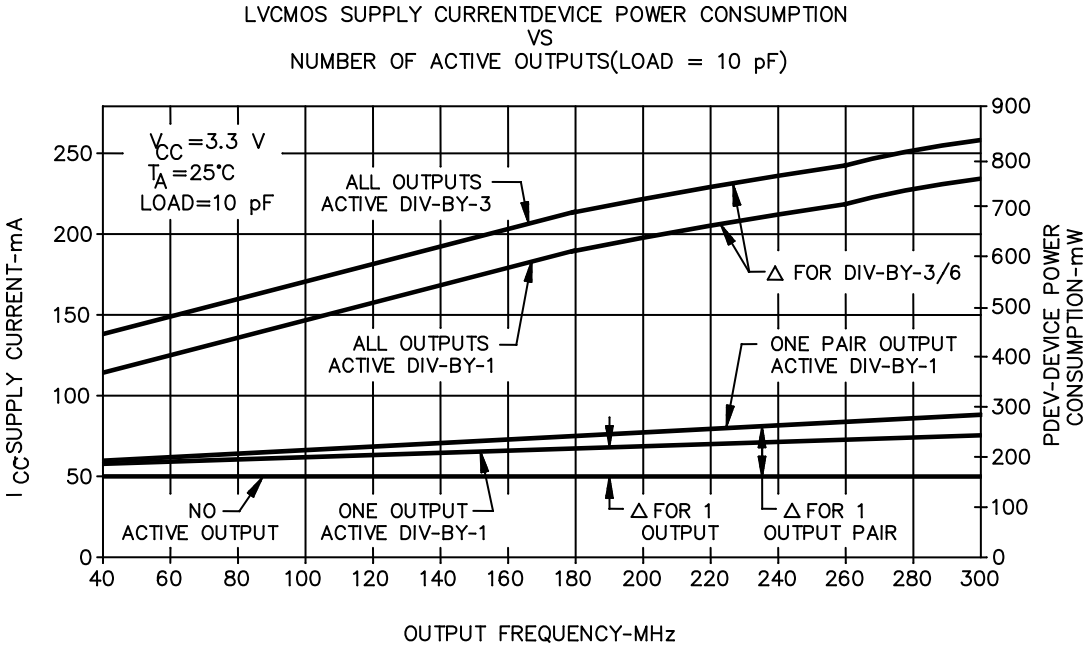


FIGURE 4-2. Timing waveforms and load circuits.



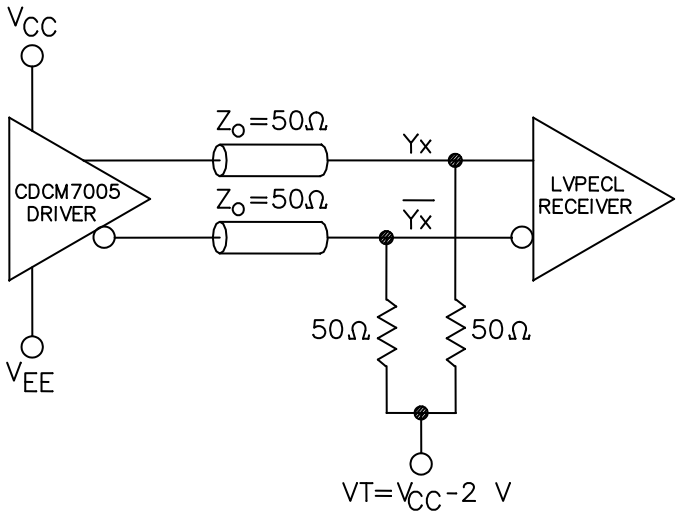
NOTE: To estimate I_{CC} with different P-divider settings use 'Δ for div-by-2/4/8/16' and 'Δ for div-by-3/6' of figure 4-1.

FIGURE 4-3. Timing waveforms and load circuits.



NOTE: To estimate I_{CC} with different P-divider settings use 'Δ for div-by-2/4/8/16' and 'Δ for div-by-3/6 of figure 4-1.

FIGURE 4-4. Timing waveforms and load circuits.



LVPECL Output Loading During device Test

FIGURE 5. Timing waveforms and load circuits.

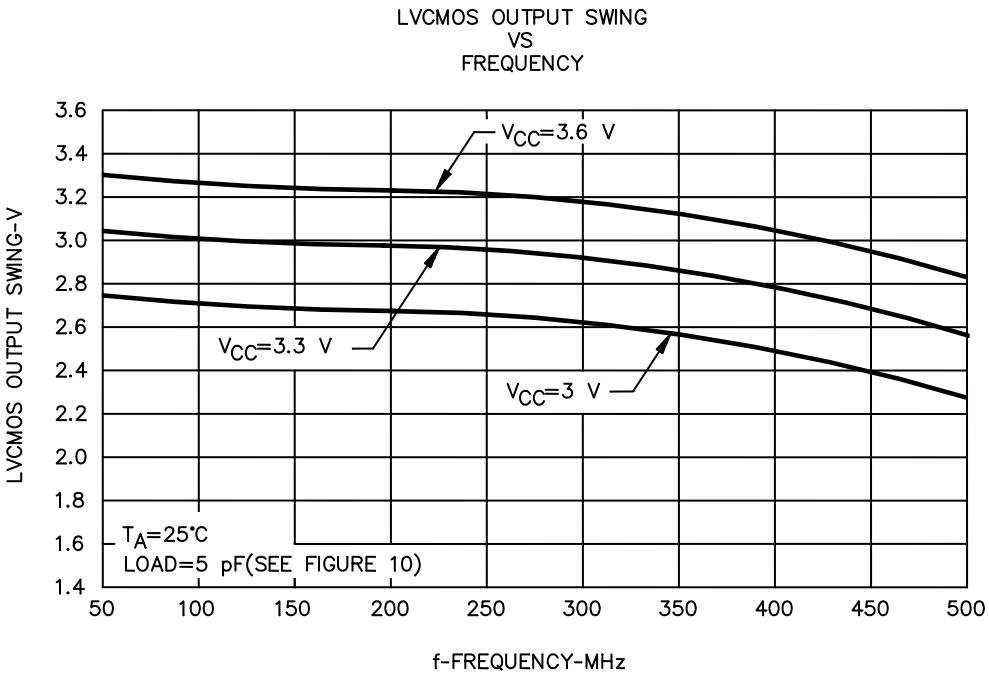


FIGURE 6. Timing waveforms and load circuits.

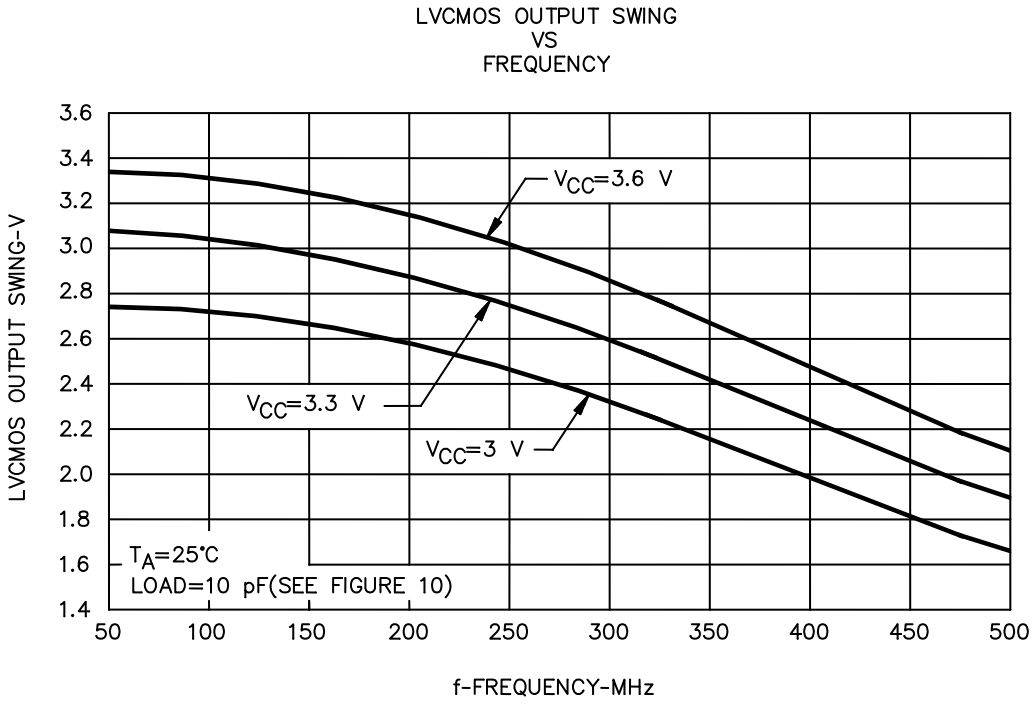


FIGURE 7. Timing waveforms and load circuits.

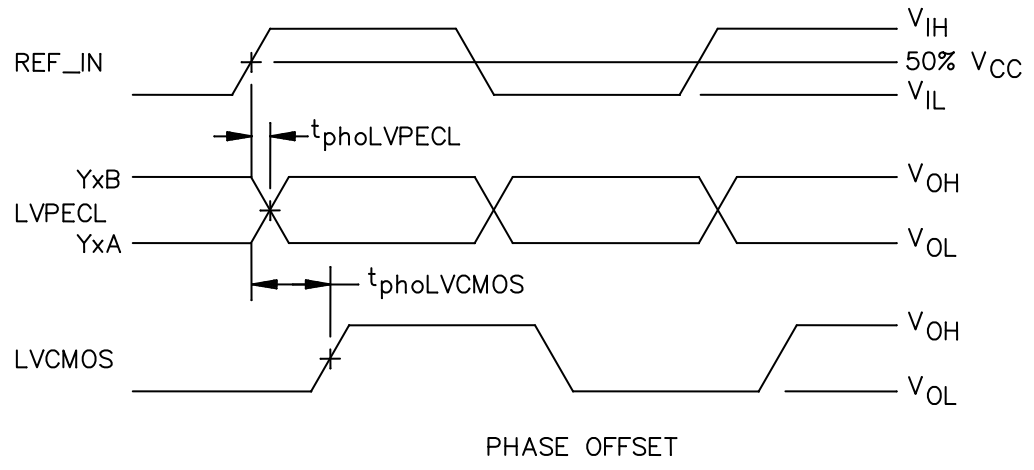
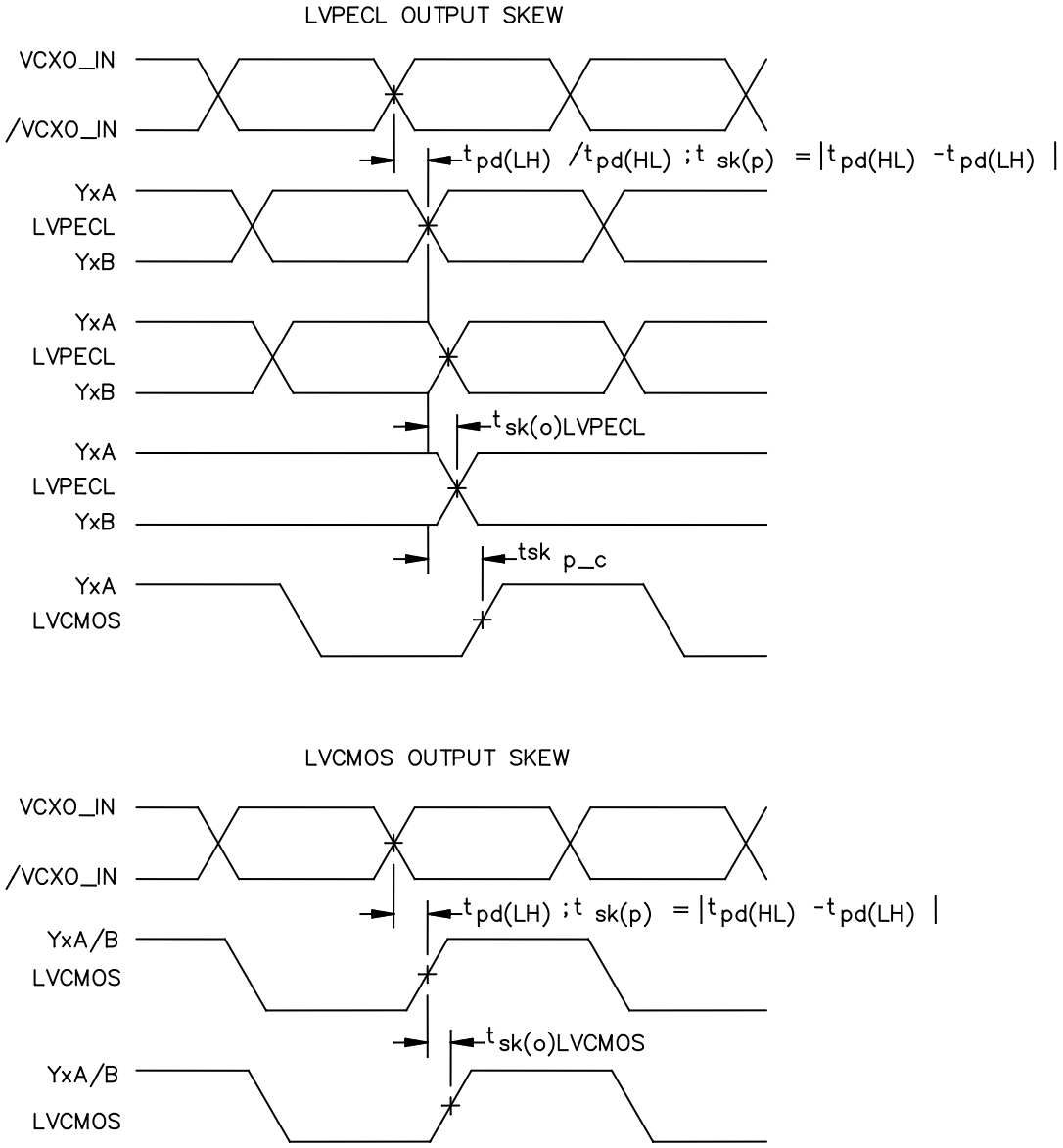


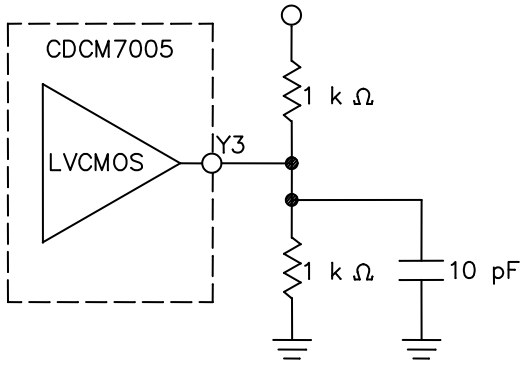
FIGURE 8. Timing waveforms and load circuits.



NOTES:

1. Output skew, $t_{sk(o)}$, is calculated as the greater of:
   The difference between the fastest and the slowest t_{pd}(LH)n (n = 0…4).
   The difference between the fastest and the slowest t_{pd}(HL)n (n = 0…4).
2. Pulse skew, $t_{sk(p)}$, is calculated as the magnitude of the absolute time difference between the high-to-low (t_{pd}(HL)) and the low-to-high (t_{pd}(LH)) propagation delays when a single switching input causes one to more outputs to switch, $t_{sk(p)} = | t_{pd}(HL) – t_{pd}(LH) |$. Pulse skew is sometimes referred to as pulse width distortion or duty cycle skew.

FIGURE 9. Timing waveforms and load circuits.



LVCMOS OUTPUT LOADING DURING DEVICE TEST

FIGURE 10. Timing waveforms and load circuits.

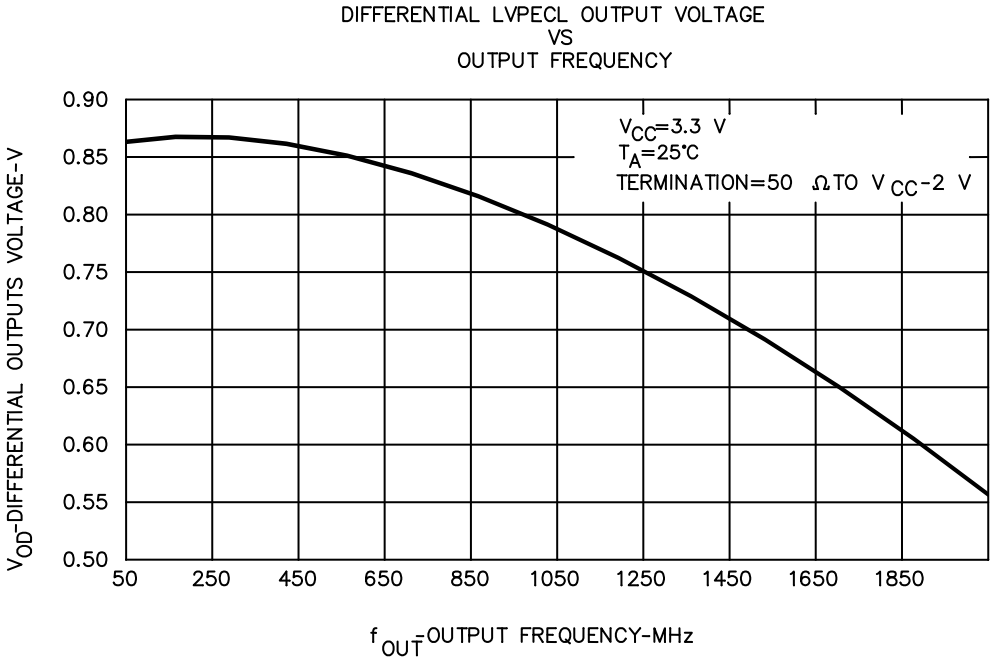


FIGURE 11. Timing waveforms and load circuits.

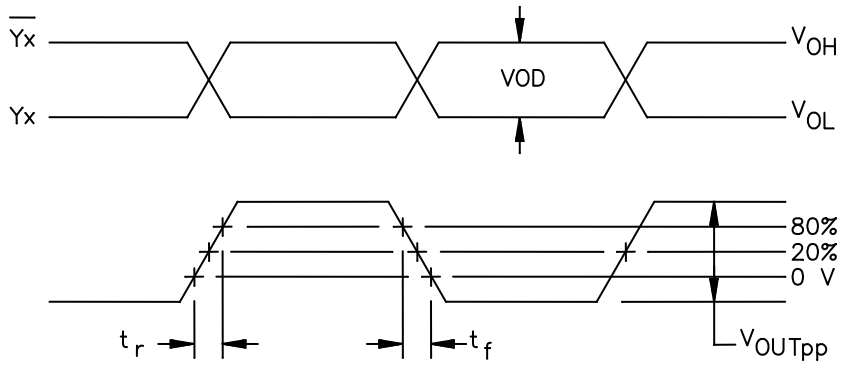


FIGURE 12. Timing waveforms and load circuits.

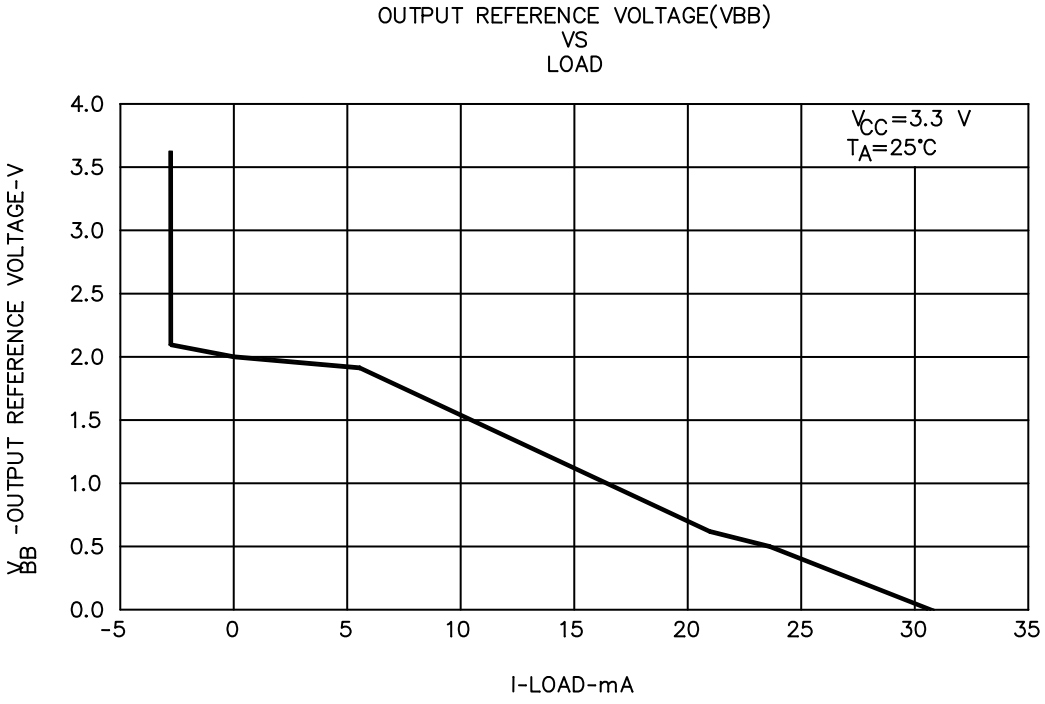
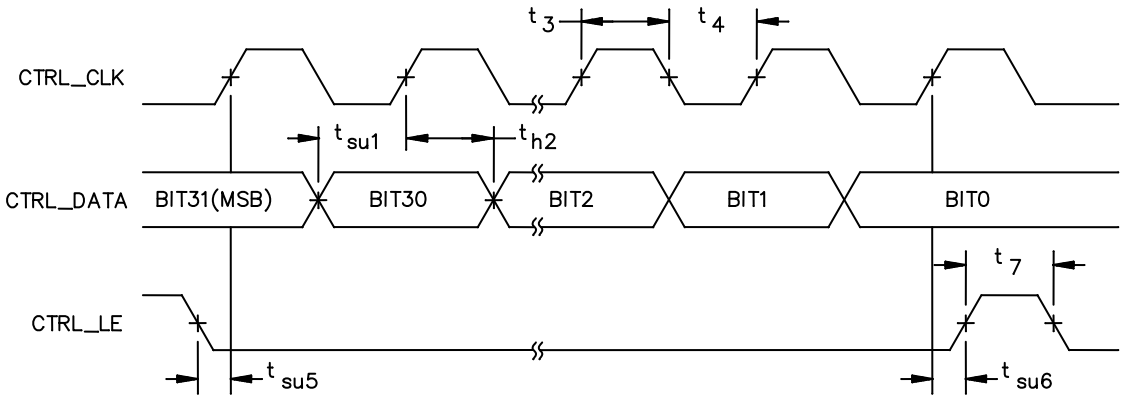


FIGURE 13. Timing waveforms and load circuits.



TIMING DIAGRAM SPI CONTROL INTERFACE

FIGURE 14. Timing waveforms and load circuits.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits as specified in table IIB herein shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test delta parameters (+25°C).

Parameter	Symbol	Delta Limits
Supply current (LVPECL)	$I_{CC\ LVPECL}$	±10 mA
Supply current (LVCMOS)	$I_{CC\ LVCMOS}$	±10 mA
Power-down current	I_{CCPD}	±25 µA
LVCMOS input current	I_{IH}	±500 nA
LVCMOS input current	I_{IL}	±750 nA
High-level output voltage for LVCMOS outputs (V_{CC} = 3 V, I_{OH} = -6 mA)	V_{OH}	±25 mV
Low-level output voltage for LVCMOS outputs (V_{CC} = 3 V, I_{OL} = 6 mA)	V_{OL}	±25 mV
Differential output voltage (LVPECL)	$\|V_{OD}\|$	±55 mV

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Pin descriptions.

Terminal		I/O	Description
Name	Pin number		
V_{CC}	19, 22, 23, 36, 28, 31, 32, 35, 36, 39, 41, 44, 46, 47, 48	Power	3.3 V power supply. There is no internal connection between V_{CC} and AV_{CC}. It is recommended that AV_{CC} use its own supply filter.
GND	Thermal pad, and pins: 1, 7, 11, 13, 45, 51	Ground	Ground.
AV_{CC}	3, 6, 9, 16, 17	Analog Power	3.3 V analog power supply. There is no internal connection between V_{CC} and AV_{CC}. It is recommended that AV_{CC} use its own supply filter.
V_{CC_CP}	10	Power	This is the charge pump power supply pin used to have the same supply as the external VCO. It can be set from 2.3 V to 3.6 V.
CTRL_LE	5	I	LVCMOS input, control latch enable for serial programmable interface (SPI), with hysteresis.
CTRL_CLK	4	I	LVCMOS input, serial control clock input for SPI, with hysteresis.
CTRL_DATA	2	I	LVCMOS input, serial control data input for SPI, with hysteresis.
$\overline{PD}$	27	I	LVCMOS input, asynchronous power down (PD) signal. This pin is active low and can be activated externally or by the corresponding bit in the SPI register (in case of logic high, the SPI setting is valid). Switches the device into power-down mode. Resets M-Divider and N-Divider, 3-states charge pump, STATUS_REF, or PRI_SEC_CLK pin, STATUS_VCXO or I_REF_CP pin, PLL_LOCK pin, V_{BB} pin and all Yx outputs. Sets the SPI register to default value; has internal 150 kΩ pullup resistor.
$\overline{RESET}$ or $\overline{HOLD}$	40	I	This LVCMOS input can be programmed (SPI) to act as $\overline{HOLD}$ or $\overline{RESET}$. $\overline{RESET}$ is the default function. This pin is active low and can be activated externally or via the corresponding bit in the SPI register. In case of $\overline{RESET}$, the charge pump (CP) is switched to 3-state and all counters (N, M, and P) are reset to zero (the initial divider settings are maintained in SPI registers). The LVPECL outputs are static low and high respectively and the LVCMOS outputs are all low or high if inverted. $\overline{RESET}$ is not edge triggered and should have a pulse duration of at least 5 ns. In case of $\overline{HOLD}$, the CP is switched in to 3-state mode only. After $\overline{HOLD}$ is released and with the next valid reference clock cycle the charge pump is switched back in to normal operation (CP stays in 3-state as long as no reference clock is valid). During $\overline{HOLD}$, the P divider and all outputs Yx are at normal operation. This mode allows an external control of the frequency hold-over mode. The input has an internal 150 kΩ pullup resistor.
VCXO_IN	21	I	VCXO LVPECL input.
$\overline{VCXO\_IN}$	20	I	Complementary VCXO LVPECL input.
PRI_REF	14	I	LVCMOS input for the primary reference clock, with an internal 150 kΩ pullup resistor and input hysteresis.
SEC_REF	15	I	LVCMOS input for the secondary reference clock, with an internal 150 kΩ pullup resistor and input hysteresis.

TABLE III. Pin descriptions - Continued.

Terminal		I/O	Description
Name	Pin number		
REF_SEL	12	I	LVCMOS reference clock selection input. In the manual mode the REF_SEL signal selects one of two input clocks: REF_SEL [1]: PRI_REF is selected; REF_SEL [0]: SEC_REF is selected; The input has an internal 150 kΩ pullup resistor.
CP_OUT	8	O	Charge pump output.
V_{BB}	18	O	Bias voltage output to be used to bias unused complementary input VXCO_IN for single ended signals. The output of V_{BB} is V_{CC} – 1.3 V. The output current is limited to about 1.5 mA.
STATUS_REF or PRI_SEC_CLK	50	O	This output can be programmed (SPI) to provide either the STATUS_REF or PRI_SEC_CLK information. This pin is set high if one of the STATUS conditions is valid. STATUS_REF is the default setting. In case of STATUS_REF, the LVCMOS output provides the Status of the Reference Clock. If a reference clock with a frequency above 2 MHZ is provided to PRI_REF or SEC_REF, STATUS_REF will be set high. In case of PRI_SEC_CLK, the LVCMOS output indicated whether the primary clock (high) or the secondary clock (low) is selected.
STATUS_VCXO or I_REF_CP	49	O	This LVCMOS output can be programmed (SPI) to provide either the STATUS_VCXO information or serve as a current path for the charge pump (CP). STATUS_VCXO is the default setting. In case of STATUS_VCXO, the LVCMOS output provides the status of the VCXO input (frequencies above 2 MHz are interpreted as valid clock; active high). In case of I_REF_CP, it provides the current path for the external reference resistor (12 kΩ ±1%) to support an accurate charge pump current, optional. Do not use a capacitor across this resistor to prevent noise coupling via this node. If the internal 12 kΩ is selected (default setting), this pin can be left open.

TABLE III. Pin descriptions - Continued.

Terminal		I/O	Description
Name	Pin number		
PLL_LOCK	52	I/O	LVCMOS output for PLL_LOCK information. This pin is set high if the PLL is in lock. This output can be programmed to be digital lock detect or analog lock detect. The PLL is locked (set high), if the rising edge of either PRI_REF or SEC_REF clock and VCXO_IN clock at the phase frequency detector (PFD) are inside the lock detect window for a predetermined number of successive clock cycles. The PLL is out-of-lock (set low), if the rising edge of either PRI_REF or SEC_REF clock and VCXO_IN clock at the PFD are outside the lock detect window or if a cycle-slip occurs. Both the lock detect window and the number of successive clock cycles are user definable (via SPI).
YOA:YOB Y1A:Y1B Y2A:Y2B Y3A:Y3B Y4A:Y4B	24, 25 29, 30 33, 34 37, 38 42, 43	O	The outputs are user definable and can be any combination of up to five LVPECL outputs or up to 10 LVCMOS outputs. The outputs are selectable via SPI (Word 1, Bit 2-6). The power-up setting is all outputs are LVPECL.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 09-10-01

Approved sources of supply for SMD 5962-07230 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0723001VXC	01295	CDCM7005MHFG-V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. Semiconductor Group 8505 Forest Ln. P.O. Box 660199 Dallas, TX 75243 Point of contact: U.S. Highway 75 South P.O. Box 84, M/S 853 Sherman, TX 75090-9493