TLC5958 具有预充电场效应晶体管 (FET)、LED 开路检测功能和显示数据存储器
且支持 32 路多路复用的 48 通道 16 位 ES-PWM LED 驱动器

1 特性

- 48 通道恒流灌电流输出
- 具有最大亮度控制 (BC)/最大颜色亮度控制 (CC) 数据的灌电流：
  - 5VCC 时为 25mA
  - 3.3VCC 时为 20mA
- 全局亮度控制 (BC)：3 位（8 步长）
- 每个颜色组的颜色亮度控制 (CC)：9 位（512 步长），三组
- 使用多路复用增强型光谱 (ES) PWM 进行灰度 (GS) 控制：16 位
- 支持 32 路多路复用的 48K 位灰度数据存储器
- LED 电源电压高达 10V
- Vcc = 3.0V 至 5.5V
- 恒流精度
  - 通道之间 = ±1%（典型值），±3%（最大值）
  - 器件之间 = ±1%（典型值），±2%（最大值）
- 数据传输速率：25MHz
- 灰度时钟频率：33MHz
- LED 开路检测 (LOD)
- 热关断 (TSD)
- I_{REF} 电阻器短路保护 (ISP)
- 可快速恢复的节能模式 (PSM)
- 延迟开关可防止浪涌电流
- 预充电 FET 可避免重影现象
- 工作温度范围：-40°C 至 +85°C

2 应用范围

- 采用多路复用系统的 LED视频显示屏
- 采用多路复用系统的 LED 信号板
- 高刷新率、高密度的 LED 面板

3 说明

TLC5958 是一款 48 通道恒流灌电流驱动器，适用于占空比为 1 至 32 的多路复用系统。 每个通道都具有单独可调的 65536 步长脉宽调制 (PWM) 灰度 (GS)。

采用 48K 位显示存储器以提升视觉刷新率，同时降低 GS 数据写入频率。

输出通道分为三组，每组含 16 个通道。 各组都具有 512 步长颜色亮度控制 (CC) 功能。 全部 48 通道的最大电流值可通过 8 步长全局亮度控制 (BC) 功能设置。 CC 和 BC 可用于调节 LED 驱动器之间的亮度偏差。 可通过一个串行接口端口访问 GS、CC 和 BC 数据。

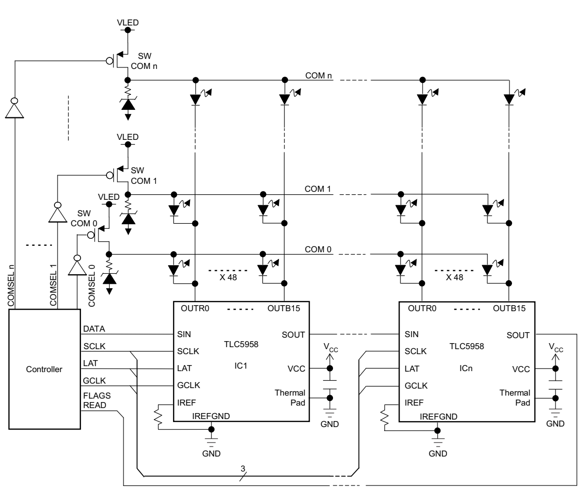
如需应用手册：*《使用 TLC5958 构建高密度、高刷新率多路复用 LED 面板》*，请通过电子邮件发送请求。

器件信息(1)

部件号	封装	封装尺寸（标称值）
TLC5958	VQFN (56)	8.00mm x 8.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

4 典型应用电路（多个菊花链 TLC5958）



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5 修订历史记录

Changes from Original (May 2014) to Revision A	**Page**
• 已删除 已删除产品预览条 - 设置为生产数据；通改	1

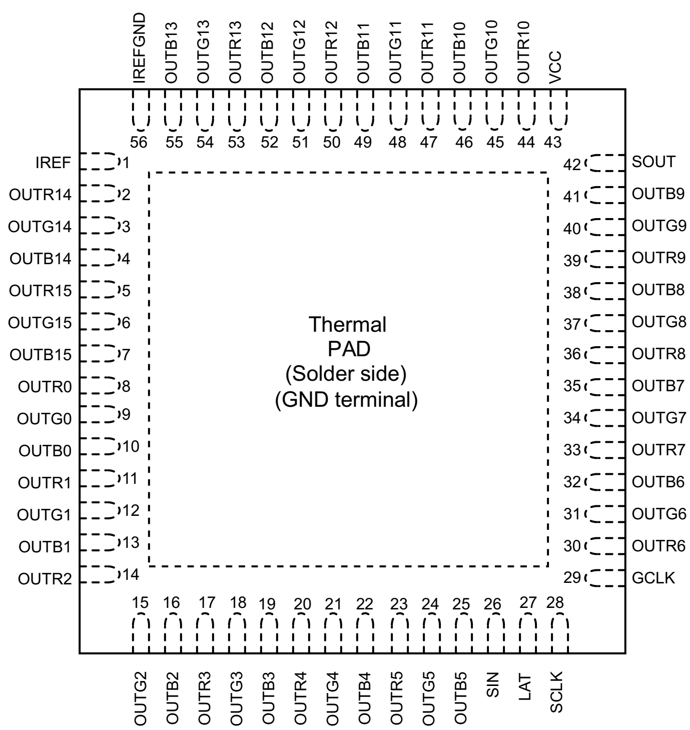
6 说明（继续）

TLC5958 有一个错误标志：LED 开路检测 (LOD)，可通过串行接口端口读取。 TLC5958 还具有节电模式，可在全部输出关闭后将总流耗设为 0.8mA（典型值）。

7 Pin Configuration and Functions

56 Pin

RTQ
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GCLK	29	I	Grayscale(GS) pulse width modulation (PWM) reference clock control for OUTXn. Each GCLK rising edge increase the GS counter by1 for PWM control.
GND	ThermalPad	–	Power ground. The thermal pad must be soldered to GND on PCB.
IREF	1	–	Maximum constant-current value setting. The OUTR0 to OUTB15 maximum constant output current are set to the desired values by connecting an external resistor between IREF and IREFGND. See equation 1 for more detail. The external resistor should be placed close to the device.
IREFGND	56	–	Analog ground. Dedicated ground pin for the external IREF resistor. This pin should be connected to analog ground trace which is connected to power ground near the common GND point of board.
LAT	27	I	The LAT falling edge latches the data from the common shift register into the GS data memory or Function control(FC) register FC1 or FC2.
OUTR0-R15	8, 11, 14, 17, 20, 23, 30, 33, 36, 39, 44, 47, 50, 53 ,2, 5	O	Constant current output for RED LED. Multiple outputs can be tied together to increase the constant current capability. Different voltages can be applied to each output. These outputs are turned on-off by GCLK signal and the data in GS data memory.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
OUTG0-G15	9, 12, 15, 18, 21, 24, 31, 34, 37, 40, 45, 48, 51, 54, 3, 6	O	Constant current output for GREEN LED. Multiple outputs can be tied together to increase the constant current capability. Different voltages can be applied to each output. These outputs are turned on-off by GCLK signal and the data in GS data memory.
OUTB0-B15	10, 13, 16, 19, 22, 25, 32, 35, 38, 41, 46, 49, 52, 55, 4, 7	O	Constant current output for BLUE LED. Multiple outputs can be tied together to increase the constant current capability. Different voltages can be applied to each output. These outputs are turned on-off by GCLK signal and the data in GS data memory.
SCLK	28	I	Serial data shift clock. Data present on SIN are shifted to the 48-bit common shift register LSB with the SCLK rising edge. Data in the shift register are shifted towards the MSB at each SCLK rising edge. The common shift register MSB appears on SOUT.
SIN	26	I	Serial data input of the 48-bit common shift register. When SIN is high level, the LSB is set to '1' for only one SCLK input rising edge. If two SCLK rising edges are input while SIN is high, then the 48-bit shift register LSB and LSB+1 are set to '1'. When SIN is low, the LSB is set to '0' at the SCLK input rising edge.
SOUT	42	O	Serial data output of the 48-bit common shift register. SOUT is connected to the MSB of the register.
VCC	43	–	Power-supply voltage.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER			MIN	MAX	UNIT
V_{CC} (2)	Supply voltage	VCC	0.3	6.0	V
I_{OUT}	Output current (dc)	OUTx0 to OUTx15, x=R, G, B		30	mA
V_{IN} (2)	Input voltage	SIN, SCLK, LAT, GCLK, IREF	–0.3	V_{CC}+0.3	V
V_{OUT} (2)	Output voltage	SOUT	–0.3	V_{CC}+0.3	V
		OUTx0 to OUTx15, x=R, G, B	–0.3	11	
$T_{J(MAX)}$	Operating junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to device ground terminal.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–55	150	°C
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (2)	0	4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (3)	0	1000	

(1) Electrostatic discharge (ESD) measures device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

At T_A = –40°C to +85°C, unless otherwise noted

			MIN	NOM	MAX	UNIT
DC CHARACTERISTICS, VCC=3V to 5.5V						
V_{CC}	Supply voltage		3		5.5	V
V_O	Voltage applied to output	OUTx0 to OUTx15, x=R, G, B			10	V
V_{IH}	High level input voltage	SIN,SCLK,LAT,GCLK	0.7×VCC		VCC	V
V_{IL}	Low level input voltage	SIN,SCLK,LAT,GCLK	GND		0.3×VCC	V
I_{OH}	High level output current	SOUT			-2	mA
I_{OL}	Low level output current	SOUT			2	mA
I_{OLC}	Constant output sink current	OUTx0 to OUTx15, x=R, G, B, 3V ≤ VCC ≤ 3.6V			20	mA
		OUTx0 to OUTx15, x=R, G, B, 4V < VCC ≤ 5.5V			25	
T_A	Operating free air temperature		–40		85	°C
T_J	Operation junction temperature		-40		125	°C

Recommended Operating Conditions (continued)

At T_A = –40°C to +85°C, unless otherwise noted

			MIN	NOM	MAX	UNIT
AC CHARACTERISTICS, VCC=3V to 5.5V [(1)]						
$F_{CLK(SCLK)}$	Data shift clock frequency	SCLK			25	MHz
$F_{CLK(GCLK)}$	Grayscale control clock frequency	GCLK			33	MHz
t_{WH0}	Pulse duration	SCLK	10			ns
t_{WL0}		SCLK	10			
t_{WH1}		GCLK	15			
t_{WL1}		GCLK	10			
t_{SU0}	Setup time	SIN - SCLK↑	2			ns
t_{SU1}		LAT↑ - SCLK↑	3			
t_{SU2}		LAT↓ - SCLK↑	5			
		LAT↓ - SCLK↑, for READSID, READFC1, and READFC2	50			
t_{SU3}		LAT↓ (Vsync command) - GCLK↑	2500			
t_{SU4}		The last LAT↓ for no all ‘0’ data latching to resume normal mode – GCLK↑, PSAVE_ENA bit = ‘1b’	50			µS
t_{SU5}		The last GCLK↑ - the 1st GCLK↑ of next line	20			ns
t_{H0}	Hold time	SCLK↑ - SIN	2			ns
t_{H1}		SCLK↑ - LAT↑	2			
t_{H2}		SCLK↑ - LAT↓	13			

(1) Specified by design

8.4 Thermal Information

THERMAL METRIC [(1)]		TLC5958 RTQ 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	27.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	5.5	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	5.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

At V_{CC}= 3.0V to 5.5V and T_A= –40°C to 85°C, VLED=5.0V, Typical values are at V_{CC}= 3.3V, T_A= 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output voltage	High	I_{OH} = -2mA at SOUT	V_{CC}–0.4		V_{CC}	V
V_{OL}		Low	I_{OL}= 2 mA at SOUT			0.4	V
V_{LOD0}	LED open detection threshold		LODVTH = 00b	0.06	0.11	0.16	V
V_{LOD1}			LODVTH = 01b	0.2	0.25	0.3	
V_{LOD2}			LODVTH = 10b	0.34	0.39	0.44	
V_{LOD3}			LODVTH = 11b	0.44	0.49	0.54	
V_{IREF}	Reference voltage output		R_{IREF} = 6.2 kΩ (1mA target), BC=0h, CCR/G/B=81h	1.19	1.209	1.228	V
I_{IN}	Input current (SIN, SCLK)		V_{IN} = V_{CC} or GND	–1		1	µA
I_{CC0}	Supply current (Vcc)		SIN/SCLK/LAT/GSCLK=GND, GSn=0000h, BC=0h, CCR/G/B=81h, VOUTn = Vcc, RIREF=OPEN		5.5	7	mA
I_{CC1}			SIN/SCLK/LAT/GSCK=GND, GSn=0000h, BC=4h, CCR/G/B=137h,VOUTn=Vcc, RIREF=7.5kΩ (Io=10mA target)		7	9	
I_{CC2}			SIN/SCLK/LAT=GND, GCLK=33MHz, T_{SU5} = 200nS, 8+8 mode, GSn=FFFFh, BC=4h, CCR/G/B=137h, VOUTn=Vcc-1V when channel on, VOUTn=Vcc when channel off. RIREF=7.5kΩ (Io=10mA target)		25	31	
I_{CC3}			SIN/SCLK/LAT=GND, GCLK=33MHz, TSU5=200nS, 8+8 mode, GSn=FFFFh, BC=7h, CCR/G/B=1F5h, VOUTn=Vcc-2.5V when channel on, VOUTn=Vcc when channel off. RIREF=7.5kΩ (Io=25mA target)		28	33	
I_{CC4}			In power save mode		0.9	1.5	
ΔI_{OLC0}	Constant current error (OUTx0-15, x=R/G/B)	Channel-to-channel (1)	All OUTn=on, BC=0h, CCR/G/B=81h, VOUTn=VOUTfix=1V, RIREF=6.2kΩ(1mA target), T_A = +25°C, at same color grouped output of OUTR0-15, OUTG0-15 and OUTB0-15		±1%	±3%	
ΔI_{OLC1}	Constant current error (OUTx0-15, x=R/G/B)	Device-to-device (2)	All OUTn=on, BC=0h, CCR/G/B=81h, VOUTn=VOUTfix=1V, RIREF=6.2kΩ(1mA target), T_A =+25°C, at same color grouped output of OUTR0-15, OUTG0-15 and OUTB0-15		±1%	±2%	
ΔI_{OLC2}	Line regulation (3)		VCC=3.0 to 5.5V, All OUTn=on, BC=0h, CCR/G/B=81h, VOUTn=VOUTfix=1V, RIREF=6.2kΩ (1mA target)		±1	±1.5	%/V
ΔI_{OLC3}	Load regulation (4)		All OUTn=on, BC=0h, CCR/G/B=81h, VOUTn=1 to 3V, VOUTfix=1V, RIREF=6.2kΩ (1mA target)		±1	±1.5	%/V

(1) The deviation of each outputs in same color group (OUTR0~15 or OUTG0~15 or OUTB0~15) from the average of same color group constant current. The deviation is calculated by the formula. (X=R or G or B, n=0~15)

$$\Delta(\%) = \left[\frac{IOUTXn}{\frac{(IOUTX0 + IOUTX1 + \ldots + IOUTX14 + IOUTX15)}{16}} - 1 \right] \times 100$$

(2) The deviation of the average of constant-current in each color group from the ideal constant-current value. (X = R or G or B) :

$$\Delta(\%) = \left[\frac{\frac{(IOUTX0 + IOUTX1 + \ldots + IOUTX15)}{16} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right] \times 100$$

Ideal current is calculated by the following equation:

$$\text{Ideal Output}(mA) = \text{Gain} \times \left[\frac{V_{IREF}}{R_{IREF}(\Omega)} \right] \times CCR(\text{or CCG, CCB})/511d, \ VIREF = 1.209V\ (\text{Typ}),$$

Refer to Table 1 for the Gain at chosen BC.

(3) Line regulation is calculated by the following equation. (X=R or G or B, n=0~15):

$$\Delta(\%V) = \left[\frac{(IOUTXn \text{ at } VCC = 5.5V) - (IOUTXn \text{ at } VCC = 3.0V)}{(IOUTXn \text{ at } VCC = 3.0V)} \right] \times \frac{100}{5.5V - 3V}$$

(4) Load regulation is calculated by the following equation. (X=R or G or B, n=0~15):

$$\Delta(\%V) = \left[\frac{(IOUTXn \text{ at } VOUTXn = 3V) - (IOUTXn \text{ at } VOUTXn = 1V)}{(IOUTXn \text{ at } VOUTXn = 1V)} \right] \times \frac{100}{3V - 1V}$$

Electrical Characteristics (continued)

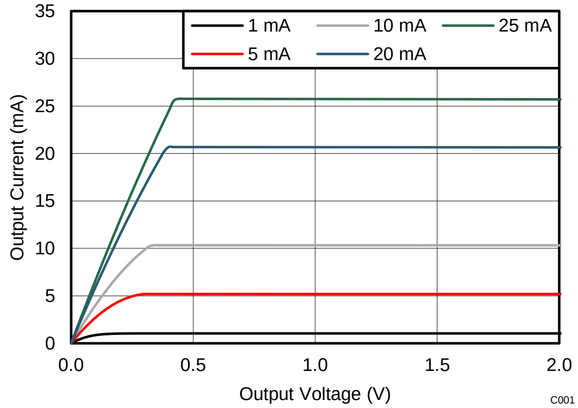
At V_{CC}= 3.0V to 5.5V and T_A= –40°C to 85°C, VLED=5.0V, Typical values are at V_{CC}= 3.3V, T_A= 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔI_{OLC4}	Constant current error (OUTx0-15, x=R/G/B)	Channel-to-channel[1]	All OUTn=on, BC=7h, CCR/G/B=1F7h, VOUTn=VOUTfix=1V, RIREF=7.5kΩ(25mA target), T_A =+25°C, at same color grouped output of OUTR0-15, OUTG0-15 & OUTB0-15		±1%	±3%	
ΔI_{OLC5}	Constant current error (OUTx0-15, x=R/G/B)	Device-to-device[2]	All OUTn=on, BC=7h, CCR/G/B=1F7h, VOUTn=VOUTfix=1V, RIREF=7.5kΩ(25mA target), T_A = +25°C, at same color grouped output of OUTR0-15, OUTG0-15 and OUTB0-15		±1%	±2%	
ΔI_{OLC6}	Line regulation[3]		VCC=3.0 to 5.5V, All OUTn=on, BC=7h, CCR/G/B=1F7h, VOUTn=VOUTfix=1V, RIREF=7.5Kohm (25mA target)		±1	±1.5	%/V
ΔI_{OLC7}	Load regulation[4]		All OUTn=on, BC=7h, CCR/G/B=1F7h, VOUTn=1 to 3V, VOUTfix=1V, RIREF=7.5kΩ (25mA target)		±1	±1.5	%/V
T_{TSD}	Thermal shutdown threshold[5]			160	170	180	°C
T_{HYS}	Thermal shutdown hysterisis				10		°C
$V_{ISP(in)}$	IREF resistor short protection threshold			0.135	0.19		V
$V_{ISP(out)}$	IREF resistor short-protection release threshold				0.325	0.375	V
R_{PDWN}	Pull-down resistor		LAT	250	500	750	kΩ
R_{PUP}	Pull-up resistor		GCLK	250	500	750	kΩ
V_{knee} [5]	Knee voltage (OUTX 0~15), X=R/G/B		All OUTn=on, BC=4h, CCR/G/B=137h, Riref=7.5kΩ. (Io=10mA target)		0.32	0.35	V

(5) Specified by design.

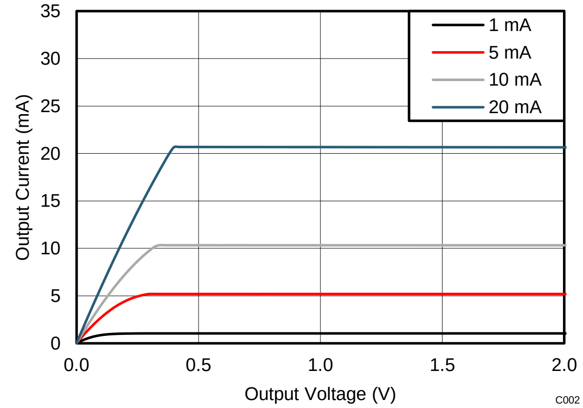
8.6 Typical Characteristics

V_{CC}= 3.3V and T_A= 25°C, unless otherwise noted.



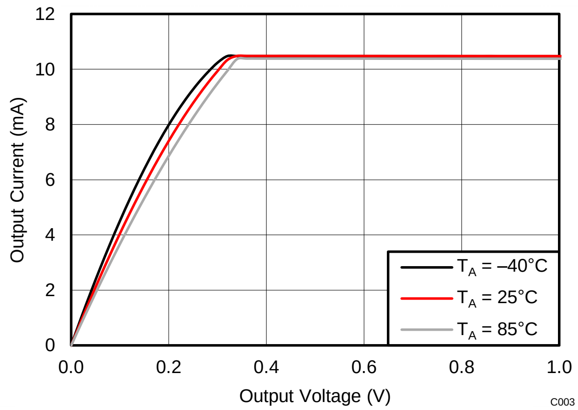
V_{CC} = 5V CCR/G/B=1FFh, BC=0

Figure 1. Output Current vs Output Voltage



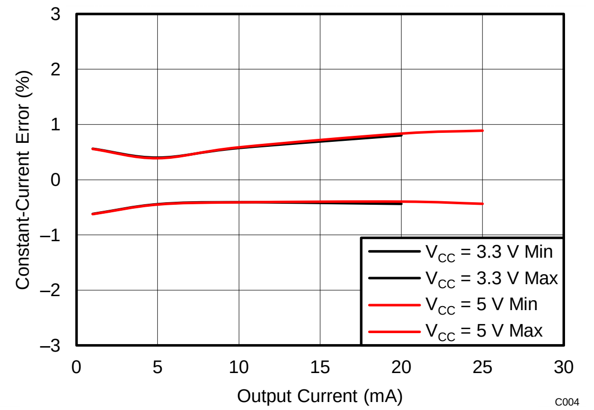
V_{CC} = 3.3V CCR/G/B=1FFh, BC=0

Figure 2. Output Current vs Output Voltage



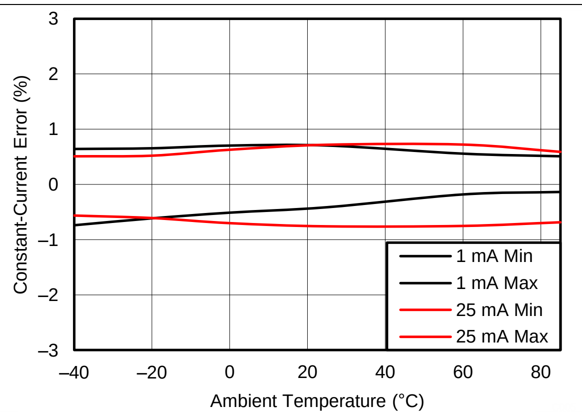
V_{CC} = 5V Temperature Changing CCR/G/B=1FFh, BC=0

Figure 3. Output Current vs Output Voltage



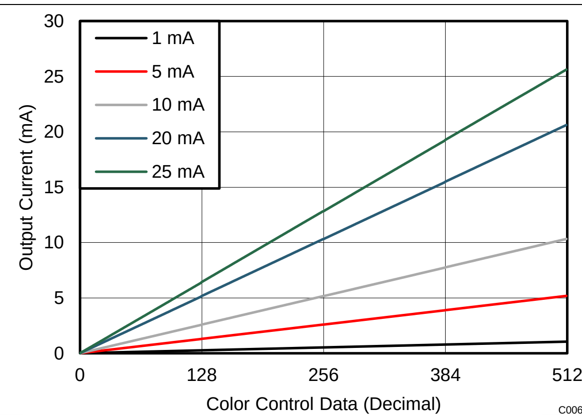
V_{OUTXn} = 0.8V CCR/G/B=1FFh, BC=0

Figure 4. Constant Current Error (CH-to-CH) vs Output Current



V_{CC} = 5V V_{OUTXn} = 0.8V CCR/G/B = 1FFh, BC = 0

Figure 5. Constant-Current Error (CH-to-CH) vs Temperature

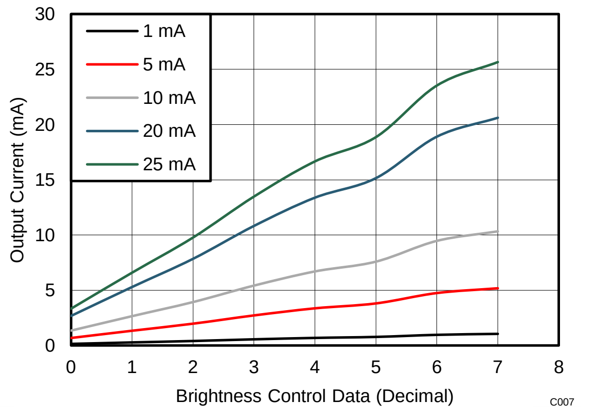


V_{CC} = 5V V_{OUTXn} = 0.8V BC = 7

Figure 6. Color Control (CC) vs Output Current

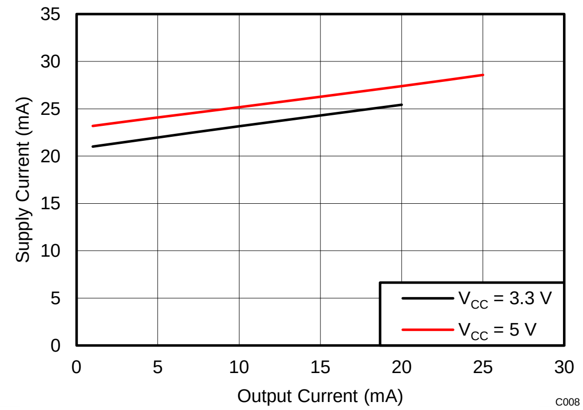
Typical Characteristics (continued)

V_{CC}= 3.3V and T_A= 25°C, unless otherwise noted.



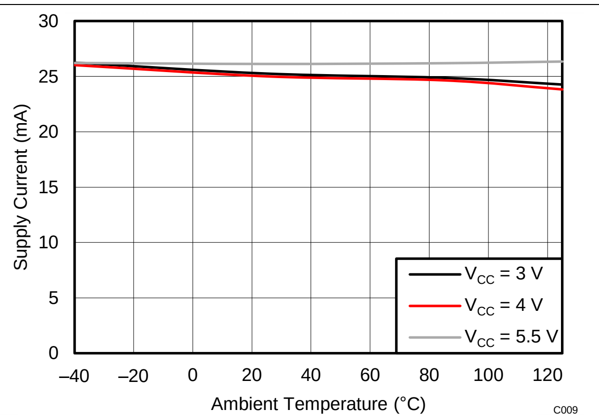
V_{CC} = 5V V_{OUTXn} = 0.8V   CCR/G/B = 1FFh

Figure 7. Brightness Control (BC) vs Output Current



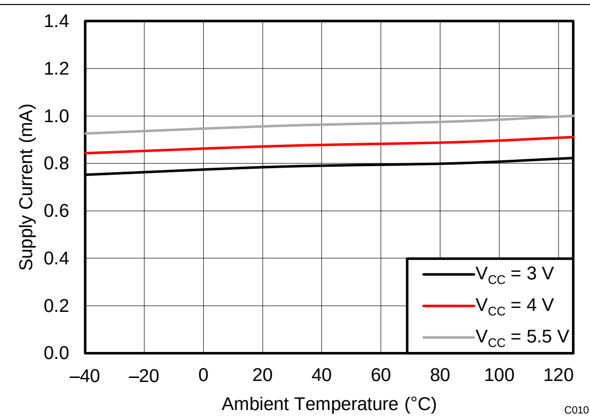
VOUTXn = 0.8V   GCLK = 33MHz, GSXn = FFFFh   CCR/G/B=1FFh, BC=0

Figure 8. Supply Current (Icc) vs Output Current



V_{OUTXn} = 0.8V   CCR/G/B = 137h, BC = 4, GCLK = 33MHz   GSXn = FFFFh, R_{IREF} = 7.5kΩ (10mA target)

Figure 9. Supply Current (Icc) vs Temperature



V_{OUTXn} = 0.8V   CCR/G/B = 137h, BC=4   GCLK=GND, GSXn=0h

Figure 10. Supply Current in Power Save Mode (Icc) vs Temperature

9 Parameter Measurement Information

9.1 Pin Equivalent Input and Output Schematic Diagrams

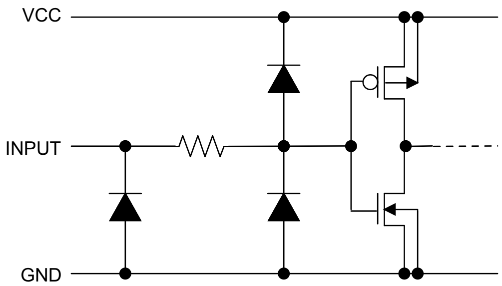


Figure 11. SIN, SCLK

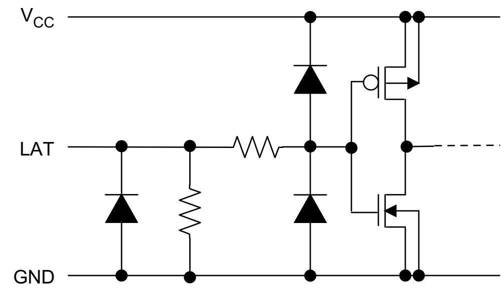


Figure 12. LAT

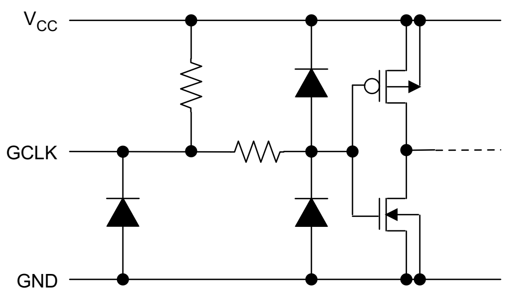


Figure 13. GCLK

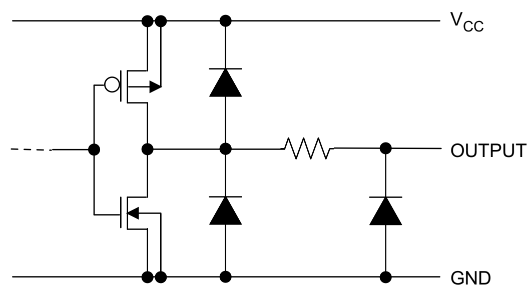


Figure 14. SOUT

(1) X=R or G or B, n=0~15

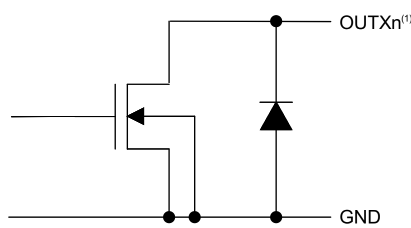


Figure 15. OUTR0/G0/B0 Through OUTR15/G15/B15

Pin Equivalent Input and Output Schematic Diagrams (continued)

9.1.1 Test Circuits

(1) CL includes measurement probe and jig capacitance.

(2) X=R or G or B, n=0~15

(1) CL includes measurement probe and jig capacitance.

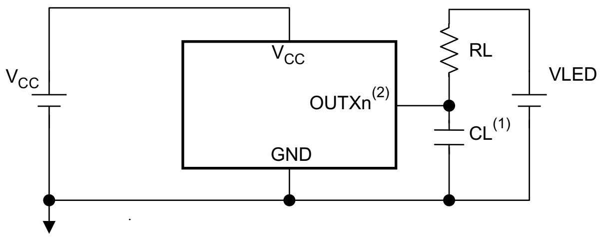


Figure 16. Rise Time and Fall Time Test Circuit for OUTXn

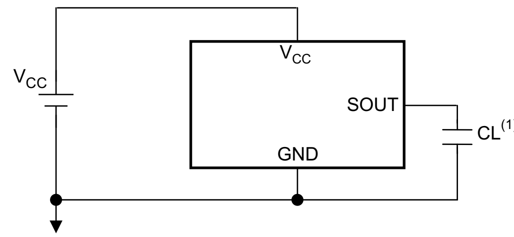


Figure 17. Rise Time and Fall Time Test Circuit for SOUT

(1) X=R or G or B, n=0~15

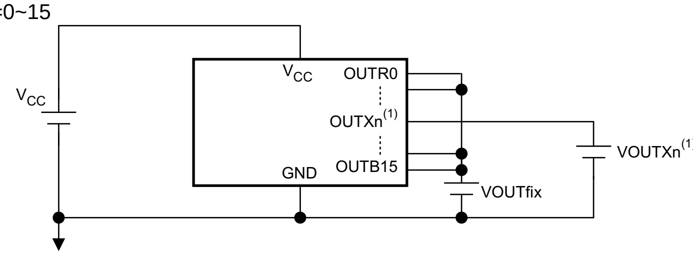
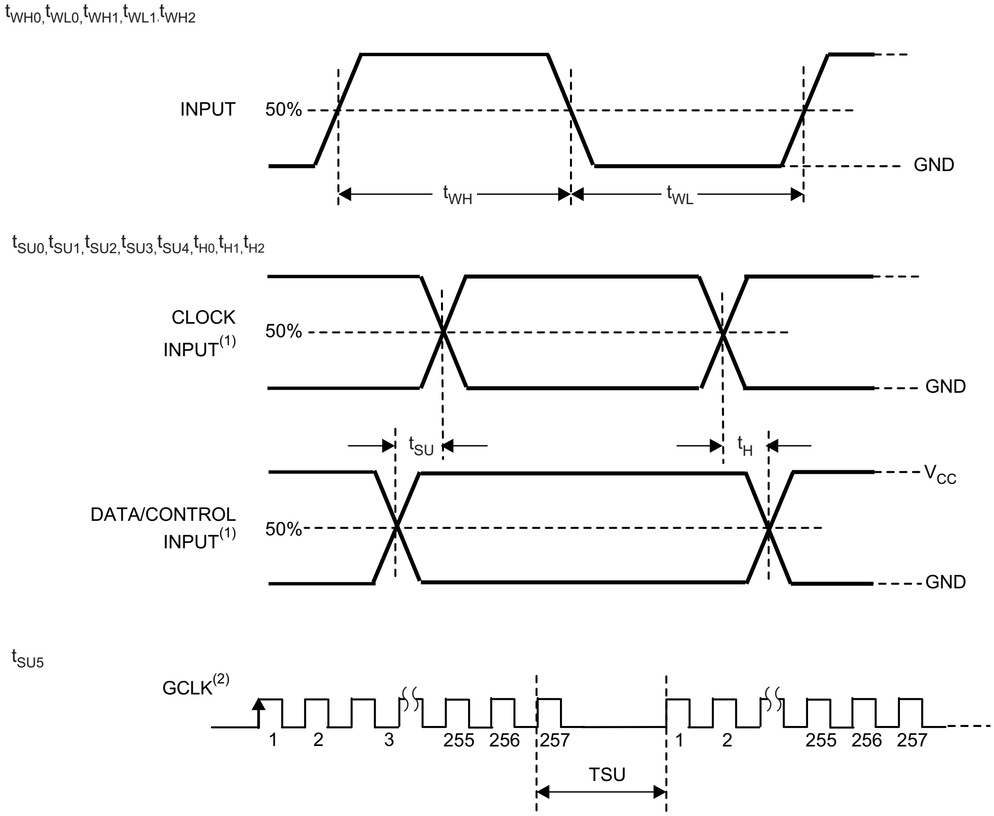


Figure 18. Constant Current Test Circuit for OUTXn

9.2 Timing Diagrams



(1) Input pulse rise and fall time is 1~3ns

(2) 8 + 8 mode (SEL_PWM=0)

Figure 19. Timing Diagrams

10 Detailed Description

10.1 Overview

The TLC5958 is a 48 channels constant-current sink driver for multiplexing system with 1 to 32 duty ratio. Each channel has an individually-adjustable, 65536-step, pulse width modulation (PWM) grayscale (GS).

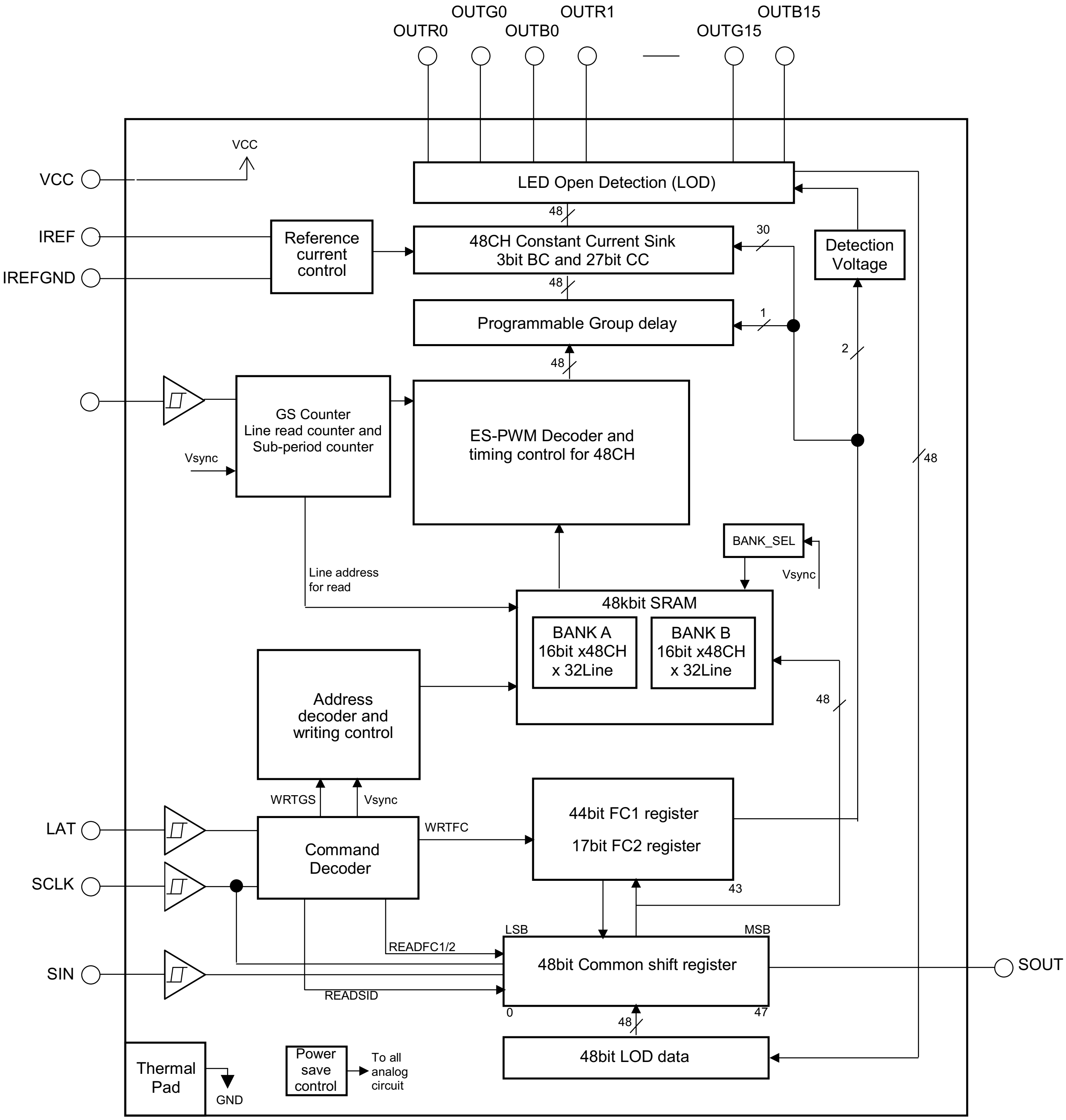
48K bit display memory is implemented to increase the visual refresh rate and to decrease the GS data writing frequency.

The TLC5958 support output current range from 1mA to 25mA, channel-to-channel accuracy is 3% max, device-to-device accuracy is 2% max in all current range. Besides, it implement Low Gray Scale Enhancement (LGSE™) technology to improve the display quality at low grayscale condition. These features make TLC5958 more suitable for high-density multiplexing application.

The output channels are grouped into three groups, each group has 16 channels. Each group has a 512-step color brightness control (CC) function. The maximum current value of all 48 channels can be set by 8-step global brightness control (BC) function. CC and BC can be used to adjust the brightness deviation between LED drivers. GS, CC, and BC data are accessible via a serial interface port.

The TLC5958 has one error flag: LED open detection (LOD), which can be read via a serial interface port. Besides, The TLC5958 also have Thermal shut down(TSD) and Iref resistor short protection(ISP), which make sure a higher system reliability. The TLC5958 also has a power-save mode that sets the total current consumption to 0.8mA (typ) when all outputs are off.

10.2 Functional Block Diagram



10.3 Device Functional Modes

After power on, all OUTXn of the TLC5958 are turned off. All the internal counters and function control registers (FC1/FC2) are initialized. The following list is a brief summary of the sequence to operate the TLC5958, to give users a general idea how the device works. After that, the function block related to each step is detailed in the following sections.

1. According to required LED current, choose BC & CC code, select the current programming resistor RIREF.
2. Send WRTFC command to set FC1/2 register value if the default value need be changed.
3. Write GS data of all lines (max 32 lines) into one of the two memory BANKs.
4. Send Vsync command, the BANK with the GS data written just now will be displayed.
5. Input GCLK continuously, 257GCLK (or 513GCLK) as a segment. Between the interval of two segments, supply voltage should be switched from one line to next line accordingly.
6. During the same period of step 5, GS data for next frame should be written into another BANK.
7. When the time of one frame ends, Vsync command should be input to swap the purpose of the two BANKs.

Repeat step 5 through 7.

10.3.1 Brightness Control (BC) Function

The TLC5958 is able to adjust the output current of all constant-current outputs simultaneously. This function is called global brightness control (BC). The global BC for all outputs is programmed with a 3-bit word, thus all output currents can be adjusted in 8 steps from 12.9% to 100% for a given current-programming resistor, R_{IREF} (See Table 2).

BC data can be set via the serial interface. When the BC data changes, the output current also changes immediately. When the device is powered on, the BC data in the function control (FC) register FC1 is set to 4h as the initial value.

10.3.2 Color Brightness Control (CC) Function

The TLC5958 is able to adjust the output current of each of the three color groups OUTR0-OUTR15, OUTG0-OUTG15, and OUTB0-OUTB15 separately. This function is called color brightness control (CC). For each color, it has 9-bit data latch CCR,CCG, or CCB in FC1 register . Thus, all color group output currents can be adjusted in 512 steps from 0% to 100% of the maximum output current, I_{OLCMax}. (See the next section for more detail about I_{OLCMax}). The CC data are entered via the serial interface. When the CC data change, the output current also changes immediately.

When the IC is powered on, the CC data are set to '100h'. Equation 1 calculates the actual output current.

$$Iout(mA) = IOLCMax(mA) \times (CCR/511d \text{ or } CCG/511d \text{ or } CCB/511d) \quad (1)$$

Where:

I_{OLCMax} = the maximum channel current for each channel, determined by BC data and R_{IREF} (See Equation 2)
CCR/G/B = the color brightness control value for each color group in the FC1 register (000h to 1FFh)

Table 1 shows the CC data versus the constant-current against I_{OLCMax}.

Device Functional Modes (continued)

Table 1. CC Data vs Current Ratio and Set Current Value

CC DATA (CCR or CCG or CCB)			RATIO OF OUTPUT CURRENT TO I_{olcMax}(%, typical)	OUTPUT CURRENT (mA, R_{IREF} = 7.41 kΩ)	
BINARY	DECIMAL	HEX		BC = 7h (IolcMax =25mA)	BC = 0h (IolcMax=3.2mA)
0 0000 0000	0	00	0	0	0
0 0000 0001	1	01	0.2	0.05	0.006
0 0000 0010	2	02	0.4	0.10	0.013
---	---	---	---	---	---
1 0000 0000 (Default)	256 (Default)	100 (Default)	50.1	12.52	1.621
---	---	---	---	---	---
1 1111 1101	509	1FD	99.6	24.90	3.222
1 1111 1110	510	1FE	99.8	24.95	3.229
1 1111 1111	511	1FF	100.0	25	3.235

10.3.3 Select R_{IREF} For a Given BC

The maximum output current per channel, I_{OLCMax}, is determined by resistor R_{IREF}, placed between the IREF and IREFGND pins, and the BC code in FC1 register. The voltage on IREF is typically 1.209V. R_{IREF} can be calculated by Equation 2.

$$Riref(k\Omega) = Viref(V) / IOLCMax(mA) \times Gain \quad (2)$$

Where:

V_{IREF} = the internal reference voltage on IREF (1.209V, typical)

I_{OLCMax} is the largest current for each output at CCR/G/B=1FFh.

Gain = the current gain at a selected BC code (See **Table 2**)

Table 2. Current Gain Versus BC Code

BC DATA		GAIN	RATIO OF GAIN / GAIN_MAX (AT MAX BC)
BINARY	HEX		
000 (recommend)	0 (recommend	20.4	12.9%
001	1	40.3	25.6%
010	2	59.7	52.4%
011	3	82.4	12.9%
100 (default)	4 (default)	101.8	64.7%
101	5	115.4	73.3%
110	6	144.3	91.7%
111	7	157.4	100%
NOTE: Recommend using a smaller BC code for better performance. For noise immunity purposes, suggest R_{IREF} < 60 kΩ			

10.3.4 Choosing BC/CC For a Different Application

BC is mainly used for global brightness adjustment between day and night. Suggested BC is 4h, which is in the middle of the range, thus, one can change brightness up and down flexibly.

CC can be used to fine tune the brightness in 512 steps, this is suitable for white balance adjustment between RGB color group. To get a pure white color, the general requirement for the luminous intensity ratio of R, G, B LED is 3:6:1. Depending on the characteristics of the LED (Electro-Optical conversion efficiency), the current ratio of R, G, B LED will be much different from this ratio. Usually, the Red LED needs the largest current. One can choose 511d (the max value) CC code for the color group that needs the largest initial current, then choose proper CC code for the other two color groups according to the current ratio requirement of the LED used.

10.3.4.1 Example 1: Red LED Current is 20mA, Green LED Needs 12mA, Blue LED needs 8mA

1. Red LED needs the largest current, so choose 511d for CCR
2. 511 x 12mA / 20mA = 306.6, thus choose 307d for CCG. With same method, choose 204d for CCB.
3. According to the required red LED current, choose 7h for BC.
4. According to Equation 2, R_{IREF} = 1.209V/20mA x 157.4 = 9.5 kΩ

In this example, we choose 7h for BC, instead of using the default 4h. This is because the Red LED current is 20mA, approaching the upper limit of current range. To prevent the constant output current from exceeding the upper limit in case a larger BC code is input accidently, we choose the maximum BC code here.

10.3.4.2 Example 2: Red LED Current is 5mA, Green LED Needs 2mA, Blue LED Needs 1mA.

1. Red LED needs the largest current, so choose 511d for CCR.
2. 511 x 2mA / 5mA = 204.4, thus choose 204d for CCG. With same method, choose 102d for CCB.
3. According to the required blue LED current, choose 0h for BC.
4. According to Equation 2, R_{IREF} = 1.209V / 5mA x 20.4 = 4.93 kΩ

In this example, we choose 0h for BC, instead of using the default 4h. This is because the Blue LED current is 1mA, is approaching the lower limit of current range. To prevent the constant output current from exceeding the lower limit in case a lower BC code is input accidently, we choose the minimum BC code here. In general, if LED current is in the middle of the range (i.e, 10mA), one can just use the default 4h as BC code.

10.3.5 LED Open Detection (LOD)

The LOD function detects faults caused by an open circuit in any LED string; or, a short from OUTXn to ground with low impedance. It does this by comparing the OUTXn voltage to the LOD detection threshold voltage level set by LODVLT in the FC1 register. If the OUTXn voltage is lower than the programmed voltage, the corresponding output LOD bit will be set to '1' to indicate a open LED. Otherwise, the output of that LOD bit is '0'. LOD data output by the detection circuit are valid only during the 'on' period of that OUTXn output channel. The LOD data are always '0' for outputs that are turned off.

10.3.6 Power Save Mode (PSM)

The power-save mode (PSM) is enabled by setting PSAVE_ENA (bit5 of FC2 register) to '1'. When power on, this bit default is '0'.

When this function is enabled, if the GS data received for next frame is all '0', IC will enter power save mode at the moment Vsync command input.

When the IC is in power-save mode, it resumes normal mode when it detects non-zero GS data input. In power-save mode all analog circuits such as constant current output and the LOD circuit are not operational; the device total current consumption, Icc, is below 1mA.

10.3.7 Internal Pre-Charge FET

The internal pre-charge FET can prevent ghosting of multiplexed LED modules. One cause of this phenomenon is the charging current for parasitic capacitance of the OUTXn through the LED when the supply voltage switches from one common line to the next common line.

To prevent this unwanted charging current, TLC5958 uses an internal FET to pull OUTXn up to VCC –1.4V during the common line switching period. Thus, no charging current flows through LED and ghosting is eliminated.

10.3.8 Thermal Shutdown (TSD)

The thermal shutdown (TSD) function turns off all IC constant-current outputs when the junction temperature (T_J) exceeds 170°C (typ). It resumes normal operation when T_J falls below 160°C (typ).

10.3.9 IREF Resistor Short Protection (ISP)

The Iref resistor short protection (ISP) function prevents unwanted large currents from flowing though the constant-current output when the Iref resistor is shorted accidently. The TLC5958 turns off all output channels when the Iref pin voltage is lower than 0.19V (typ). When the Iref pin voltage goes higher than 0.325V (typ), the TLC5958 resumes normal operation.

10.3.10 Noise Reduction

Large surge currents may flow through the IC and the board on which the device is mounted if all 48 LED channels turned on simultaneously at the 1st GCLK rising edge. This large surge current could induce detrimental noise and electromagnetic interference (EMI) into other circuits.

The TLC5958 separates the LED channels into 12 groups. Each group turns on sequentially with some delay between one group and the next group. By this operation, a soft-start feature provides for minimal inrush current.

11 Application and Implementation

Send request via email for Application Note: *Build High Density, High Refresh Rate, Multiplexing LED Panel with TLC5958*

12 Power Supply Recommendations

The V_{CC} power supply voltage should be decoupled by placing a 0.1 µF ceramic capacitor close to VCC pin and GND plane. Depending on panel size, several electrolytic capacitors must be placed on board equally distributed to get a well regulated LED supply voltage (VLED). VLED voltage ripple should be less than 5% of its nominal value. Furthermore, the VLED should be set to the voltage calculated by equation:

$$VLED > Vf + 0.4V \text{ (10mA constant current example)} \quad (3)$$

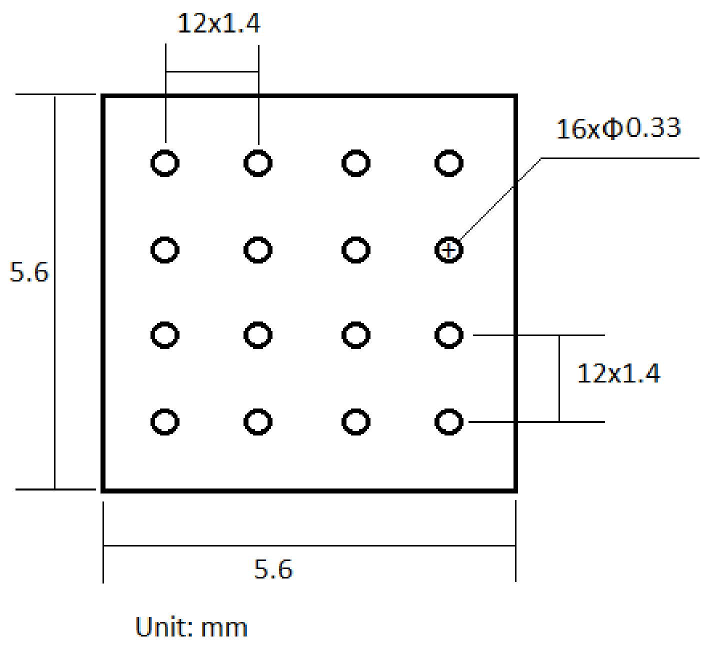
Where: Vf = maximum forward voltage of LED

13 Layout

13.1 Layout Guidelines

1. Place the decoupling capacitor near the VCC pin and GND plane.
2. Place the current programming resistor Riref close to IREF pin and IREFGND pin.
3. Route the GND pattern as widely as possible for large GND currents. Maximum GND current is approximately 1.2A
4. Routing between the LED cathode side and the device OUTXn pin should be as short and straight as possible to reduce wire inductance.
5. The PowerPAD™ must be connected to GND plane because the pad is used as power ground pin internally, there will be large current flow through this pad when all channels turn on. Furthermore, this pad should be connected to a heat sink layer by thermal via to reduce device temperature. One suggested thermal via pattern is shown as below. For more information about suggested thermal via pattern and via size, see " PowerPAD Thermally Enhanced Package", SLMA002G.

13.2 Layout Example



14 器件和文档支持

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14.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

14.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

15 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5958RTQR	ACTIVE	QFN	RTQ	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5958	Samples
TLC5958RTQT	ACTIVE	QFN	RTQ	56	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	TLC5958	Samples

(1) The marketing status values are defined as follows:
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LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
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(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
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Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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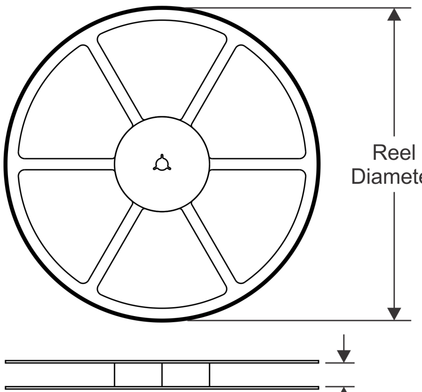
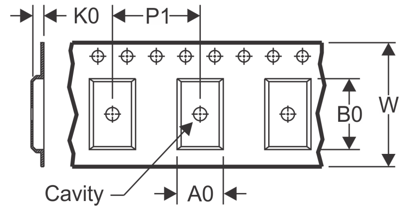
TAPE AND REEL INFORMATION

REEL DIMENSIONS

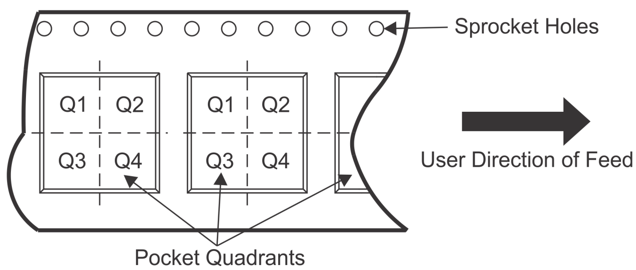


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

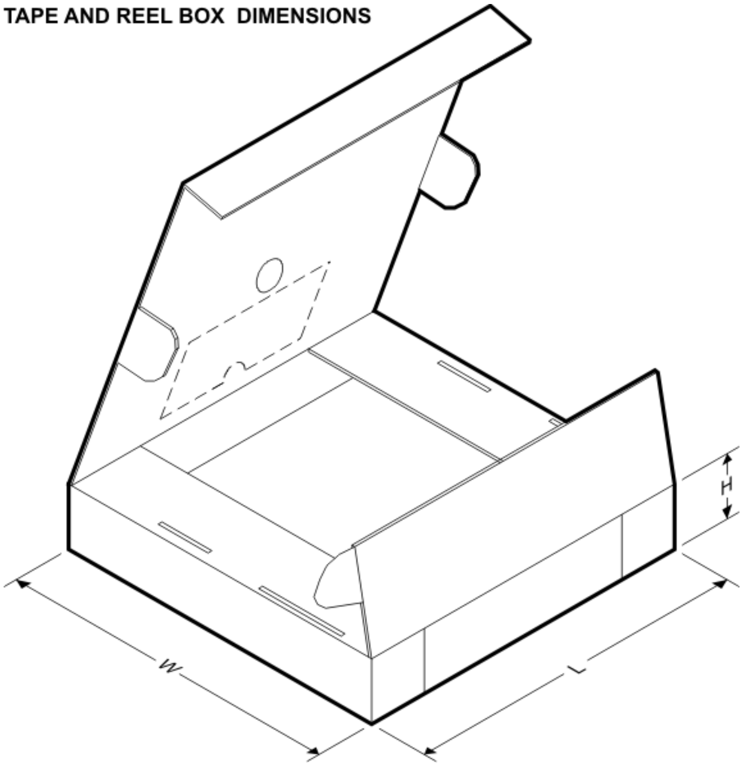
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5958RTQR	QFN	RTQ	56	2000	330.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2
TLC5958RTQT	QFN	RTQ	56	250	180.0	16.4	8.3	8.3	1.1	12.0	16.0	Q2

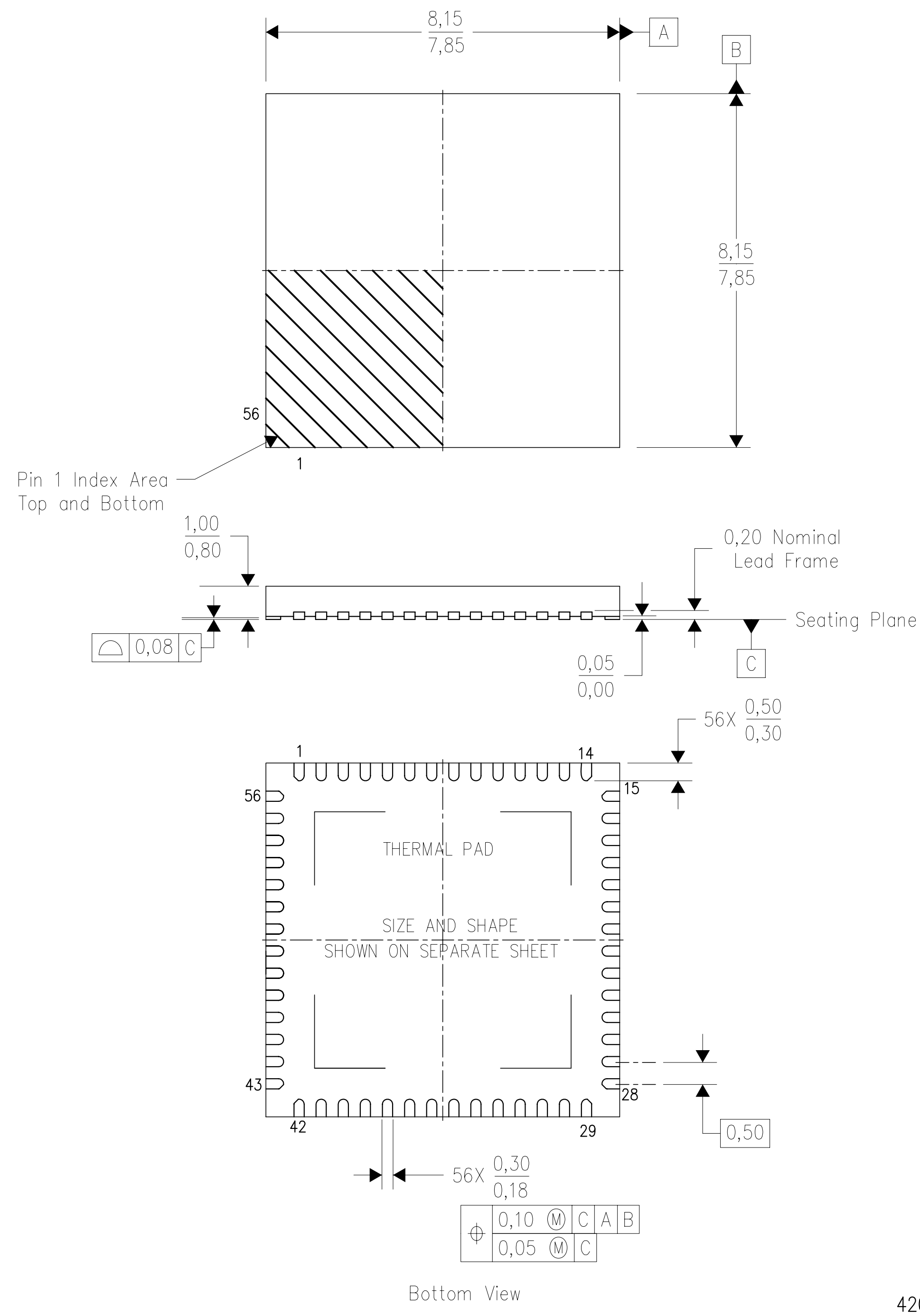
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5958RTQR	QFN	RTQ	56	2000	367.0	367.0	38.0
TLC5958RTQT	QFN	RTQ	56	250	210.0	185.0	35.0

RTQ (S-PVQFN-N56) PLASTIC QUAD FLATPACK NO-LEAD



4206089/D 08/11

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Package complies to JEDEC MO–220.

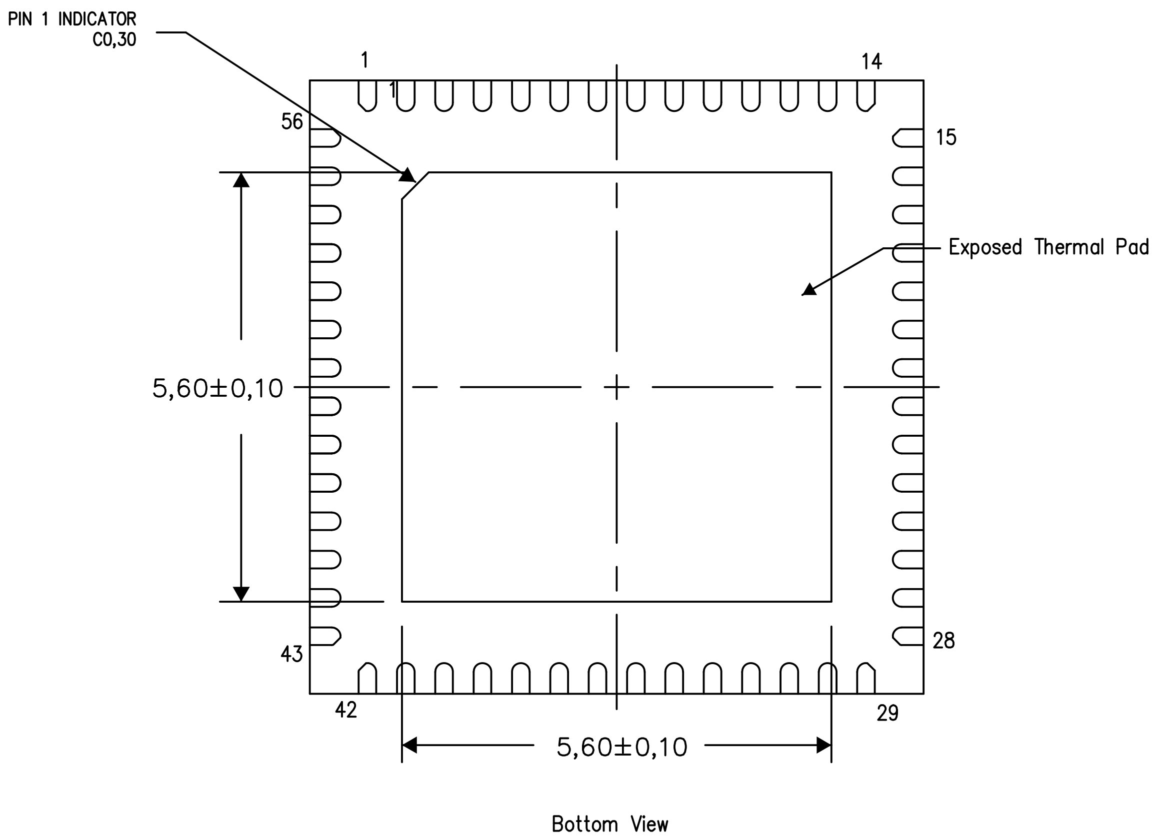
RTQ (S-PVQFN-N56) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206252-8/Q 03/15

NOTE: All linear dimensions are in millimeters

产品		应用	
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