WL18xxMOD WiLink™ 8 双频段工业模块 – Wi-Fi®， *Bluetooth*®，和 *Bluetooth* 低功耗 (BLE)

1 器件概述

1.1 特性

- 常规说明
  - 集成了射频 (RF)、功率放大器 (PA)、时钟、RF 开关、滤波器、无源器件和电源管理单元
  - 可利用 TI 模块配套资料和参考设计实现快速硬件设计
  - 工作温度：–40°C 至 85°C（工业级）
  - 小封装尺寸：13.3mm x 13.4mm x 2mm
  - 100 引脚 MOC 封装
  - 经 FCC，IC，ETSI/CE 和 TELEC 认证的芯片天线
- **Wi-Fi**
  - 支持 IEEE 标准 802.11a、802.11b、802.11g 和 802.11n 的 WLAN 基带处理器和 RF 收发器
  - 2.4GHz 20MHz 和 40MHz 单输入单输出 (SISO) 以及 2.4GHz 20MHz 2 x 2 多输入多输出 (MIMO)，针对高数据吞吐量：80Mbps (TCP)，100Mbps (UDP)
  - 2.4GHz 最大比合并 (MRC)，支持扩展范围且具备 5GHz 分集能力
  - 完全校准：无需生产校准
  - 4 位 SDIO 主机接口支持
  - Wi-Fi 直接并发运行（多通道、多用途）
- ***Bluetooth*** 和 **BLE**（仅适用于 **WL1837MOD**）
  - 支持 *Bluetooth* 4.1 和 CSA2
  - 主机控制器接口 (HCI) 传输，用于通过通用异步收发器 (UART) 进行的 *Bluetooth* 传输
  - 支持子带 (SBC) 编码 + 高级音频传输协议 (A2DP) 的专用音频处理器
  - 双模 *Bluetooth* 和 BLE
  - Bluetopia + LE 认证堆栈（由 TI 提供）
- 主要优势
  - 减少设计开销
  - 通过在两极（STA 和 AP）上同时配置 WiLink 8，可将差别化的使用案例直接连接至不同 RF 通道（Wi-Fi 网络）上的其它 Wi-Fi 器件
  - 用于高性能音频和视频流参考应用的一流 Wi-Fi，覆盖范围高达单根天线的 1.4 倍
  - 提供多种配置方法，可一步将室内设备连接至 Wi-Fi
  - 连接空闲时最低 Wi-Fi 功耗 (< 800µA)
  - WLAN 滤波器上只将系统唤醒的可配置唤醒
  - Wi-Fi-*Bluetooth* 单天线共存

1.2 应用范围

- 物联网
- 多媒体
- 家用电子产品
- 家用电器和大型家电
- 工业和家庭自动化
- 智能网关和仪表计量
- 视频会议
- 视频摄像机和安防器材

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1.3 说明

TI 经认证的 WiLink 8 模块采用功率优化设计，可提供高数据吞吐量和扩展范围，并且支持 Wi-Fi 和 *Bluetooth* 共存（只适用于 WL1837MOD）。 WL18x7MOD 是一套支持 Wi-Fi 的双频带 2.4GHz 和 5GHz 模块解决方案，配有两根支持工业温度级的天线。 该器件经 FCC、IC、ETSI/CE 和 TELEC 认证，适用于接入点 (AP)（支持 DFS）和客户端。 TI 为 Linux®、 Android™、WinCE 和 RTOS 等高级操作系统提供了驱动程序。

器件信息

订货编号	封装	封装尺寸
WL1807MOD	MOC (100)	13.3mm × 13.4mm × 2mm
WL1837MOD	MOC (100)	13.3mm × 13.4mm × 2mm

1.4 功能方框图

图 1-1 显示了 WL1837 变型的功能方框图。

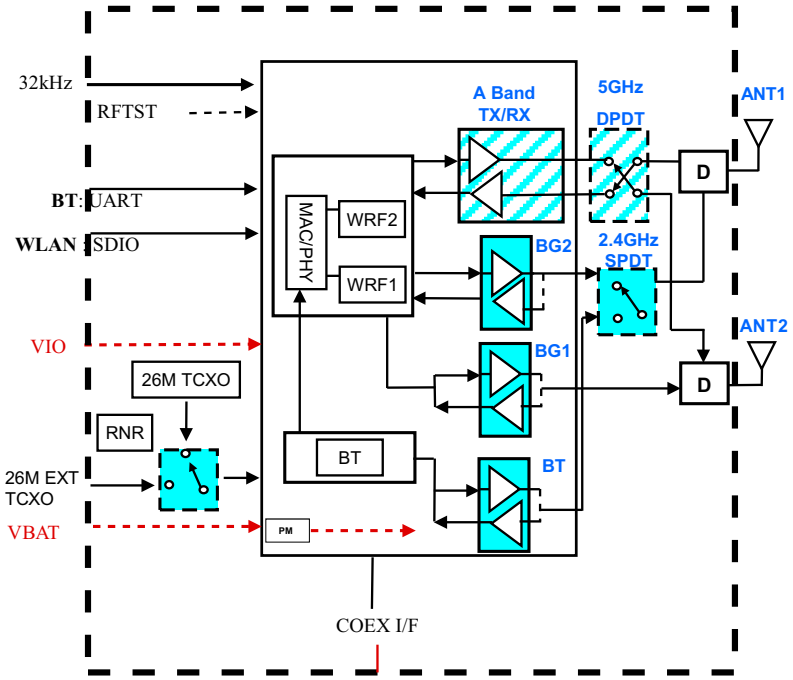

图 **1-1. WL1837** 功能方框图

内容

2 修订历史记录

Changes from Revision A (September 2014) to Revision B **Page**

- Changed 节 1.2，*应用* 1
- Added 节 9.2, *Packaging Information* 39

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3 Device Comparison

The TI WiLink 8 module offers four footprint-compatible dual-band 2.4- and 5-GHz industrial temperature grade variants providing stand-alone and *Bluetooth* combo connectivity. Table 3-1 compares the features of the module variants.

Table 3-1. TI WiLink 8 Module Variants

DEVICE	WLAN 2.4-GHZ SISO	WLAN 2.4-GHZ MISO	WLAN 2.4-GHZ MRC(1)	*BLUETOOTH*	WLAN 5-GHZ SISO
WL1837MOD	√	√	√	√	√
WL1807MOD	√	√	√		√

(1) MRC: maximum ratio combining.supported at 2.4-GHz only

4 Terminal Configuration and Functions

Figure 4-1 shows the pin assignments for the 100-pin MOC package.

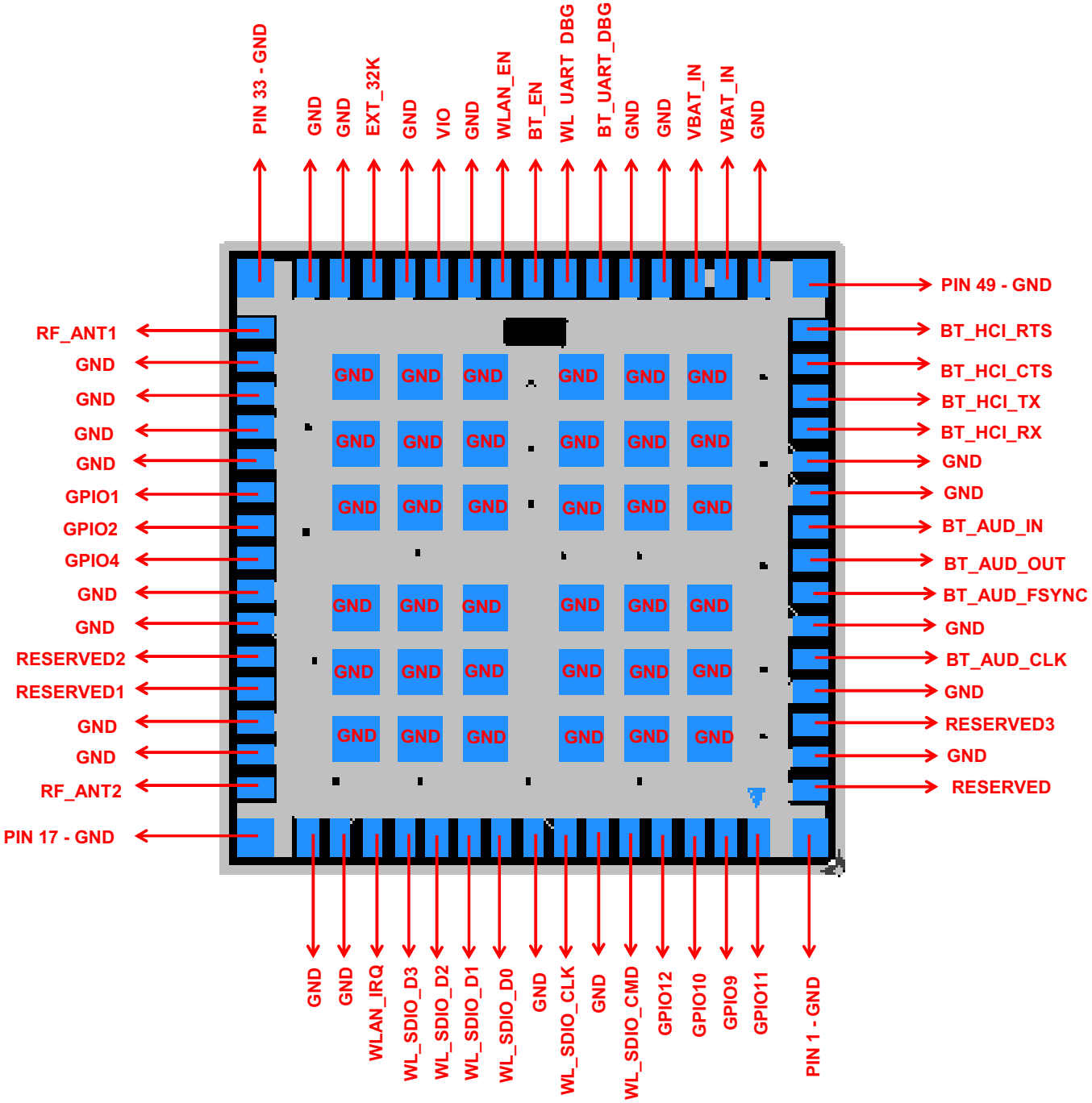
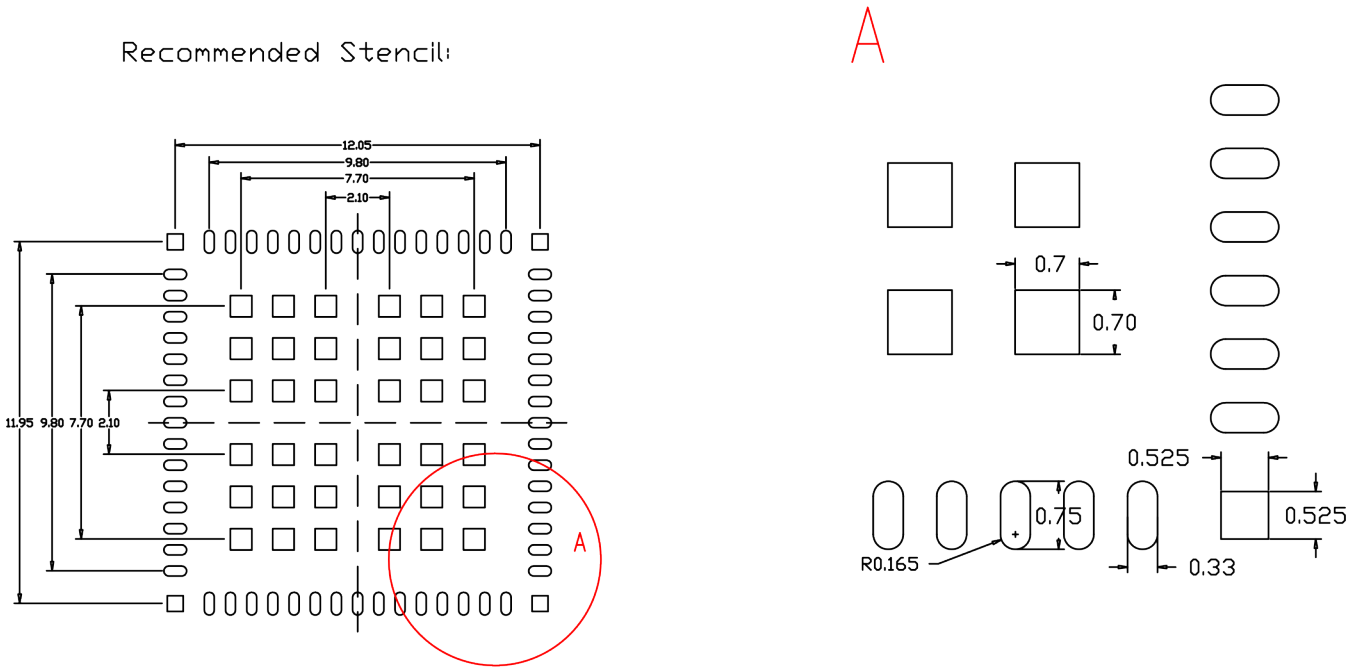


Figure 4-1. 100-Pin MOC Package (Bottom View)

Figure 4-2 shows the outline of the 100-pin MOC package.



NOTE: 1. Module size: 13.4 x 13.3 mm
2. Pad size: 0.75 x 0.40 mm
3. Pitch: 0.7 mm

Figure 4-2. Outline of 100-Pin MOC Package

Figure 4-3 shows the outline of the recommended PCB pattern for the 100-pin MOC package.

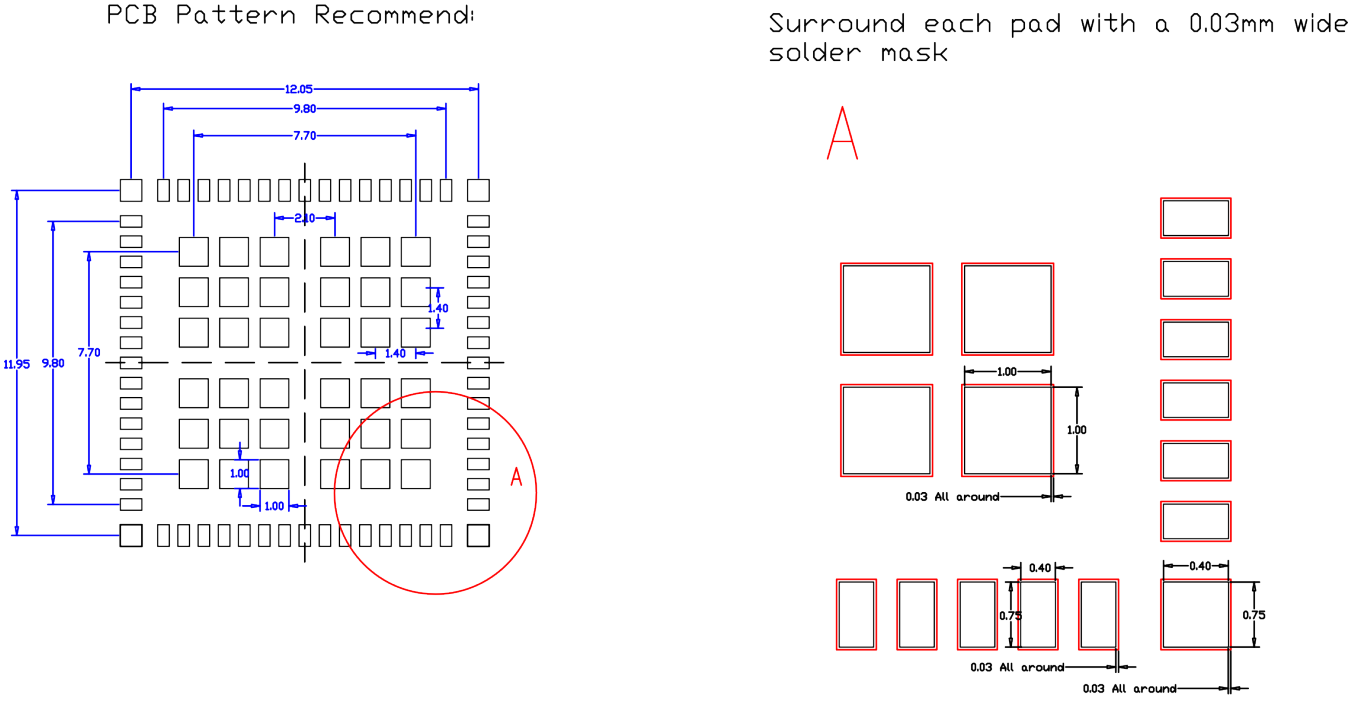


Figure 4-3. Outline of Recommended PCB Pattern for 100-Pin MOC Package

4.1 Pin Description

Table 4-1 describes the module pins.

Table 4-1. Pin Description

PIN NAME	PIN	TYPE/ DIR	SHUTDOWN STATE	AFTER POWER UP	VOLTAGE LEVEL	CONNECTIVITY		DESCRIPTION
						1807	1837	
Clocks and Reset Signals								
WL_SDIO_CLK_1V8	8	I	Hi-Z	Hi-Z	1.8 V	v	v	WLAN SDIO clock. Must be driven by the host.
EXT_32K	36	ANA			–	v	v	Input sleep clock: 32.768 kHz
WLAN_EN	40	I	PD	PD	1.8 V	v	v	Mode setting: high = enable
BT_EN	41	I	PD	PD	1.8 V	x	v	Mode setting: high = enable
Power-Management Signals								
VIO_IN	38	POW	PD	PD	1.8 V	v	v	Connect to 1.8-V external VIO
VBAT_IN	46	POW			VBAT	v	v	Power supply input, 2.9 to 4.8 V
VBAT_IN	47	POW			VBAT	v	v	Power supply input, 2.9 to 4.8 V
TI Reserved								
GPIO11	2	I/O	PD	PD	1.8 V	v	v	Reserved for future use. NC if not used.
GPIO9	3	I/O	PD	PD	1.8 V	v	v	Reserved for future use. NC if not used.
GPIO10	4	I/O	PU	PU	1.8 V	v	v	Reserved for future use. NC if not used.
GPIO12	5	I/O	PU	PU	1.8 V	v	v	Reserved for future use. NC if not used.
RESERVED1	21	I	PD	PD	1.8 V	x	x	Reserved for future use. NC if not used.
RESERVED2	22	I	PD	PD	1.8 V	x	x	Reserved for future use. NC if not used.
GPIO4	25	I/O	PD	PD	1.8 V	v	v	Reserved for future use. NC if not used.
RESERVED3	62	O	PD	PD	1.8 V	x	x	Reserved for future use. NC if not used. Option: External TCXO.
RESERVED	64	GND			–	v	v	Reserved for future use. NC if not used. Option: External TCXO.
WLAN Functional Block: Int Signals								
WL_SDIO_CMD_1V8	6	I/O	Hi-Z	Hi-Z	1.8 V	v	v	WLAN SDIO command in
WL_SDIO_D0_1V8	10	I/O	Hi-Z	Hi-Z	1.8 V	v	v	WLAN SDIO data bit 0
WL_SDIO_D1_1V8	11	I/O	Hi-Z	Hi-Z	1.8 V	v	v	WLAN SDIO data bit 1
WL_SDIO_D2_1V8	12	IO	Hi-Z	Hi-Z	1.8 V	v	v	WLAN SDIO data bit 2
WL_SDIO_D3_1V8	13	I/O	Hi-Z	PU	1.8 V	v	v	WLAN SDIO data bit 3. Changes state to PU at WL_EN or BT_EN assertion for card detects. Later disabled by software during initialization. (1)

Table 4-1. Pin Description (continued)

PIN NAME	PIN	TYPE/ DIR	SHUTDOWN STATE	AFTER POWER UP	VOLTAGE LEVEL	CONNECTIVITY		DESCRIPTION
						1807	1837	
WL_IRQ_1V8	14	O	PD	0	1.8 V	v	v	SDIO available, interrupt out. Active high. (For WL_RS232_TX/RX pullup is at power up.) Set to rising edge (active high) on power up. The Wi-Fi interrupt line can be configured by the driver according to the IRQ configuration (polarity/level/edge).
2G4_ANT2_W	18	ANA			–	v	v	2.4G ant2 TX, RX
GPIO2	26	I/O	PD	PD	1.8 V	v	v	WL_RS232_RX (when WLAN_IRQ = 1 at power up)
GPIO1	27	I/O	PD	PD	1.8 V	v	v	WL_RS232_TX (when WLAN_IRQ = 1 at power up)
2G4_ANT1_WB	32	ANA			–	v	v	2.4G ant1 TX, RX
WL_UART_DBG	42	O	PU	PU	1.8 V	v	v	Option: WLAN logger
***Bluetooth* Functional Block:Int Signals**								
BT_UART_DBG	43	O	PU	PU	1.8 V	x	v	Option: *Bluetooth* logger
BT_HCI_RTS_1V8	50	O	PU	PU	1.8 V	x	v	UART RTS to host. NC if not used.
BT_HCI_CTS_1V8	51	I	PU	PU	1.8 V	x	v	UART CTS from host. NC if not used.
BT_HCI_TX_1V8	52	O	PU	PU	1.8 V	x	v	UART TX to host. NC if not used.
BT_HCI_RX_1V8	53	I	PU	PU	1.8 V	x	v	UART RX from host. NC if not used.
BT_AUD_IN	56	I	PD	PD	1.8 V	x	v	*Bluetooth* PCM/I2S bus. Data in. NC if not used.
BT_AUD_OUT	57	O	PD	PD	1.8 V	x	v	*Bluetooth* PCM/I2S bus. Data out. NC if not used.
BT_AUD_FSYNC	58	I/O	PD	PD	1.8 V	x	v	*Bluetooth* PCM/I2S bus. Frame sync. NC if not used.
BT_AUD_CLK	60	I/O	PD	PD	1.8 V	x	v	*Bluetooth* PCM/I2S bus. NC if not used.
Ground Pins								
GND	1, 7, 9, 15, 16, 17, 18, 19, 20, 23, 24, 28, 29, 30, 31, 33, 34, 35, 37, 39, 44, 45, 48, 49, 54, 55, 59, 61, 63, G1-G36	GND			–	v	v	

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5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	VALUE	UNIT
VBAT	4.8(2)	V
VIO	–0.5 to 2.1	V
Input voltage to analog pins	–0.5 to 2.1	V
Input voltage limits (CLK_IN)	–0.5 to VDD_IO	V
Input voltage to all other pins	–0.5 to (VDD_IO + 0.5 V)	V
Operating ambient temperature range	–40 to 85(3)	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) 4.8 V cumulative to 2.33 years, including charging dips and peaks
(3) Operating free-air temperature range at which the device can operate reliably for 15K cumulative active TX power-on hours (assuming a maximum junction temperature of (T_j) of 125°C). Section 5.3, *Power-On Hours (POH)*, describes the correlation between T_j and PoH. In the WL18xx system, a control mechanism automatically ensures T_j < 125°C. Whenever T_j approaches the threshold, this mechanism controls the transmitter patterns.

5.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–40	+85	°C
ESD stress voltage(1)	Human body model (HBM)(2)	–1000	+1000	V
	Charged device model (CDM)(3)	–250	+250	

(1) ESD measures device sensitivity and immunity to damage caused by electrostatic discharges into the device.
(2) The level listed is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500-V HBM is possible, if necessary precautions are taken. Pins listed as 1000 V can actually have higher performance.
(3) The level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 250-V CDM is possible, if necessary precautions are taken. Pins listed as 250 V can actually have higher performance.

5.3 Power-On Hours (POH)

OPERATING JUNCTION TEMPERATURE (°C)	POH
125	15,000
120	20,000
115	27,000
110	37,000
105	50,000

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VBAT(1)	DC supply range for all modes		2.9		4.8	V
	1.8-V I/O ring power supply voltage		1.62		1.95	V
V_{IH}	I/O high-level input voltage		0.65 x VDD_IO		VDD_IO	V
V_{IL}	I/O low-level input voltage		0		0.35 × VDD_IO	V
VIH_EN	Enable inputs high-level input voltage		1.365		VDD_IO	V

(1) 4.8 V is applicable only for 2.3 years (30% of the time). Otherwise, maximum VBAT must not exceed 4.3 V.

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Recommended Operating Conditions *(continued)*

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VIL_EN	Enable inputs low-level input voltage		0		0.4	V
V_{OH}	High-level output voltage	@ 4 mA	VDD_IO –0.45		VDD_IO	V
V_{OL}	Low-level output voltage	@ 4 mA	0		0.45	V
T_r,T_f	Input transitions time T_r,T_f from 10% to 90% (digital I/O)(2)		1		10	ns
T_r	Output rise time from 10% to 90% (digital pins)(2)	C_L < 25 pF			5.3	ns
T_f	Output fall time from 10% to 90% (digital pins)(2)	C_L < 25 pF			4.9	ns
	Ambient operating temperature		–40		85	ºC
Maximum power dissipation	WLAN operation				2.8	W
	Bluetooth operation				0.2	

(2) Applies to all digital lines except SDIO, UART, I2C, PCM and slow clock lines

5.5 External Digital Slow Clock Requirements

The supported digital slow clock is 32.768 kHz digital (square wave). All core functions share a single input.

PARAMETER	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Input slow clock frequency				32768		Hz
Input slow clock accuracy (Initial + temp + aging)	WLAN, *Bluetooth*				±250	ppm
Input transition time T_r,T_f (10% to 90%)		T_r,T_f			200	ns
Frequency input duty cycle			15	50	85	%
Input voltage limits	Square wave, DC-coupled	Vih	0.65 x VDD_IO		VDD_IO	V_{peak}
		Vil	0		0.35 x VDD_IO	
Input impedance			1			MΩ
Input capacitance					5	pF

5.6 Thermal Characteristics

AIR FLOW		
NAME	DESCRIPTION	FCBGA (°C/W)(1)
θ_{JC}	Junction to case	12.7
θ_{JB}	Junction to board	13.6
θ_{JA}	Junction to free air(2)	20.5
φ_{JB}	Junction to board	8.7

(1) °C/W = degrees Celsius per watt
(2) According to the JEDEC EIA/JESD 51 document

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5.7 WLAN Performance

All RF and performance numbers are aligned to the module pin.

5.7.1 WLAN 2.4-GHz Receiver Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Operation frequency range	2400 to 2480	2400		2480	MHz
Sensitivity: 20-MHz bandwidth. At < 10% PER limit	1 Mbps DSSS		–96.3		dBm
	2 Mbps DSSS		–93.2		
	5.5 Mbps CCK		–90.6		
	11 Mbps CCK		–87.9		
	6 Mbps OFDM		–92.0		
	9 Mbps OFDM		–90.4		
	12 Mbps OFDM		–89.5		
	18 Mbps OFDM		–87.2		
	24 Mbps OFDM		–84.1		
	36 Mbps OFDM		–80.7		
	48 Mbps OFDM		–76.5		
	54 Mbps OFDM		–74.9		
	MCS0 MM 4K		–90.4		
	MCS1 MM 4K		–87.6		
	MCS2 MM 4K		–85.9		
	MCS3 MM 4K		–82.8		
	MCS4 MM 4K		–79.4		
	MCS5 MM 4K		–75.2		
	MCS6 MM 4K		–73.5		
	MCS7 MM 4K		–72.4		
	MCS0 MM 4K 40 MHz		–86.7		
	MCS7 MM 4K 40 MHz		–67.0		
	MCS0 MM 4K MRC		–92.7		
	MCS7 MM 4K MRC		–75.2		
	MCS13 MM 4K		–73.7		
	MCS14 MM 4K		–72.3		
	MCS15 MM 4K		–71.0		
Max Input Level At < 10% PER limit	OFDM (11g/n)	–19	–9		dBm
	DSSS	–4	–0		dBm
Adjacent channel rejection: Sensitivity level +3 dB for OFDM; Sensitivity level +6 dB for 11b	2 Mbps DSSS	42.7			dB
	11 Mbps CCK	37.9			dB
	54 Mbps OFDM	2.0			dB

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5.7.2 WLAN 2.4-GHz Transmitter Power

over operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
	RF_IO2_BG_WL pin 2.4-GHz SISO				
Output Power: Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM(1)	1 Mbps DSSS		17.3		dBm
	2 Mbps DSSS		17.3		
	5.5 Mbps CCK		17.3		
	11 Mbps CCK		17.3		
	6 Mbps OFDM		17.1		
	9 Mbps OFDM		17.1		
	12 Mbps OFDM		17.1		
	18 Mbps OFDM		17.1		
	24 Mbps OFDM		16.2		
	36 Mbps OFDM		15.3		
	48 Mbps OFDM		14.6		
	54 Mbps OFDM		13.8		
	MCS0 MM		16.1		
	MCS1 MM		16.1		
	MCS2 MM		16.1		
	MCS3 MM		16.1		
	MCS4 MM		15.3		
	MCS5 MM		14.6		
	MCS6 MM		13.8		
	MCS7 MM(2)		12.6		
	MCS0 MM 40 MHz		14.8		
	MCS7 MM 40 MHz		11.3		
	2G4_ANT2_W + 2G4_ANT1_WB				
Operation frequency range		2412		2484	MHz
Return loss			–10.0		dB
Reference input impedance			50.0		Ω

(1) Regulatory constraints limit TI module output power to the following:
- Channels 1, 11, 13 @ OFDM legacy and HT 20-MHz rates: 14 dBm
- Channels 1, 11, 13 @ HT 40-MHz lower rates: 12 dBm
- Channel 7 @ HT 40-MHz lower rates: 12 dBm
- Channel 5 @ HT 40-MHz upper rates: 12 dBm

(2) To ensure compliance with the EVM conditions specified in the PHY chapter of IEEE Std 802.11™ – 2012:
- MCS7 20 MHz channel 12 output power is 2 dB lower than the typical value.
- MCS7 20 MHz channel 8 output power is 1 dB lower than the typical value.

5.7.3 WLAN 5-GHz Receiver Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Operation frequency range		4910.0		5825.0	MHz
Sensitivity: 20-MHz bandwidth. At < 10% PER limit	6 Mbps OFDM 1K		–92.2		dBm
	9 Mbps OFDM 1K		–90.4		
	12 Mbps OFDM 1K		–89.6		
	18 Mbps OFDM 1K		–87.1		
	24 Mbps OFDM 1K		–84.0		
	36 Mbps OFDM 1K		–80.6		
	48 Mbps OFDM 1K		–76.3		
	54 Mbps OFDM 1K		–74.7		
	MCS0 MM 4K		–90.5		
	MCS1 MM 4K		–87.7		
	MCS2 MM 4K		–85.9		
	MCS3 MM 4K		–82.8		
	MCS4 MM 4K		–79.4		
	MCS5 MM 4K		–75.1		
	MCS6 MM 4K		–73.5		
	MCS7 MM 4K		–72.2		
	MCS0 MM 4K 40 MHz		–87.7		
	MCS7 MM 4K 40 MHz		–69.0		
Max input level	802.11a/n	–27.0			dBm
Adjacent channel rejection: Sensitivity level +3 dB for OFDM	OFDM54	2.0			dBm
LO leakage			–53.0		dBm
PER floor			1.0	2.0	%
RSSI	Sensitivity ÷ –50 dBm			±2	dB
	–50 dBm ÷ –20 dBm			±3	dB

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5.7.4 WLAN 5-GHz Transmitter Power

over operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Output Power: Maximum RMS output power measured at 1 dB from IEEE spectral mask or EVM	6 Mbps OFDM		17.5		
	9 Mbps OFDM		17.5		
	12 Mbps OFDM		17.5		
	18 Mbps OFDM		17.5		
	24 Mbps OFDM		16.4		
	36 Mbps OFDM		15.7		
	48 Mbps OFDM		14.9		
	54 Mbps OFDM		14.1		
	MCS0 MM		17.1		
	MCS1 MM 4K		17.1		
	MCS2 MM 4K		17.1		
	MCS3 MM 4K		17.1		
	MCS4 MM 4K		15.7		
	MCS5 MM 4K		14.9		
	MCS6 MM 4K		14.1		
	MCS7 MM 4K		13.1		
	MCS0 MM 40 MHz		16.6		
	MCS7 MM 40 MHz		12.3		
Output power accuracy		–1.5		+1.5	dB
Output power resolution			0.125		dB
Operation frequency range		2412		2484	MHz
Return loss			–10.0		dB
Reference input impedance			50.0		Ω

5.7.5 WLAN Currents

	SPECIFICATION ITEMS	TYP (AVG) – 25°C	UNITS
Receiver	Low-power mode (LPM) 2.4-GHz RX SISO20 single chain	49	mA
	2.4 GHz RX search SISO20	54	mA
	2.4-GHz RX search MIMO20	74	mA
	2.4-GHz RX search SISO40	59	mA
	2.4-GHz RX 20 M SISO 11 CCK	56	mA
	2.4-GHz RX 20 M SISO 6 OFDM	61	mA
	2.4-GHz RX 20 M SISO MCS7	65	mA
	2.4-GHz RX 20 M MRC 1 DSSS	74	mA
	2.4-GHz RX 20 M MRC 6 OFDM	81	mA
	2.4-GHz RX 20 M MRC 54 OFDM	85	mA
	2.4-GHz RX 40 MHz MCS7	77	mA
	5-GHz RX 20 MHz OFDM6	77	mA
	5-GHz RX 20 MHz MCS7	68	mA
	5-GHz RX 40 MHz MCS7	73	mA

	SPECIFICATION ITEMS	TYP (AVG) – 25°C	UNITS
Transmitter	2.4-GHz TX 20 M SISO 6 OFDM 15.4 dBm	285	mA
	2.4-GHz TX 20 M SISO 11 CCK 15.4 dBm	273	mA
	2.4-GHz TX 20 M SISO 54 OFDM 12.7 dBm	247	mA
	2.4-GHz TX 20 M SISO MCS7 11.2 dBm	238	mA
	2.4-GHz TX 20 M MIMO MCS15 11.2 dBm	420	mA
	2.4-GHz TX 40 M SISO MCS7 8.2 dBm	243	mA
	5-GHz TX 20 M SISO 6 OFDM 18.2 dBm	366	mA
	5-GHz TX 20 M SISO 54 OFDM 15.5 dBm	329	mA
	5-GHz TX 20 M SISO MCS7 14.0 dBm	324	mA
	5-GHz TX 40 M SISO MCS7 11.0 dBm	332	mA

5.8 *Bluetooth* Performance

All RF and performance numbers are aligned to the module pin.

5.8.1 Bluetooth BR, EDR Receiver Characteristics—In-Band Signals

over operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITION		MIN	TYP	MAX	UNIT
Bluetooth BR, EDR operation frequency range			2402		2480	MHz
Bluetooth BR, EDR channel spacing				1		MHz
Bluetooth BR, EDR input impedance				50		Ω
Bluetooth BR, EDR sensitivity(1) dirty TX on	BR, BER = 0.1%			–92.2		dBm
	EDR2, BER = 0.01%			–91.7		dBm
	EDR3, BER = 0.01%			–84.7		dBm
Bluetooth EDR BER floor at sensitivity + 10 dB Dirty TX off (for 1,600,000 bits)	EDR2		1e-6			
	EDR3		1e-6			
Bluetooth BR, EDR maximum usable input power	BR, BER = 0.1%		–5.0			dBm
	EDR2, BER = 0.1%		–15.0			dBm
	EDR3, BER = 0.1%		–15.0			dBm
Bluetooth BR intermodulation	Level of interferers for n = 3, 4, and 5		–36.0	–30.0		dBm
Bluetooth BR, EDR C/I performance Numbers show wanted signal-to-interfering-signal ratio. Smaller numbers indicate better C/I performances (Image frequency = –1 MHz)	BR, co-channel				10	dB
	EDR, co-channel	EDR2			12	dB
		EDR3			20	dB
	BR, adjacent ±1 MHz				–3.0	dB
	EDR, adjacent ±1 MHz, (image)	EDR2			–3.0	dB
		EDR3			2.0	dB
	BR, adjacent +2 MHz				–33.0	dB
	EDR, adjacent +2 MHz	EDR2			–33.0	dB
		EDR3			–28.0	dB
	BR, adjacent –2 MHz				–20.0	dB
	EDR, adjacent –2 MHz	EDR2			–20.0	dB
		EDR3			–13.0	dB
	BR, adjacent ≥I±3I MHz				–42.0	dB
	EDR, adjacent ≥I±3I MHz	EDR2			–42.0	dB
		EDR3			–36.0	dB

(1) Sensitivity degradation up to –3 dB may occur due to fast clock harmonics with dirty TX on.

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PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Bluetooth BR, EDR RF return loss			–10.0		dB

5.8.2 Bluetooth Transmitter, BR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
BR RF output power(1)	VBAT ≥ 3 V		12.7		dBm
	VBAT < 3 V		7.2		dBm
BR gain control range			30.0		dB
BR power control step			5.0		dB
BR adjacent channel power |M-N| = 2			–43.0		dBm
BR adjacent channel power |M-N| > 2			–48.0		dBm

(1) Values reflect maximum power. Reduced power is available using a vendor-specific (VS) command.

5.8.3 Bluetooth Transmitter, EDR

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
EDR output power(1)	VBAT ≥ 3 V		7.2		dBm
	VBAT < 3 V		5.2		
EDR relative power					dB
EDR gain control range			30		dB
EDR power control step			5		dB
EDR adjacent channel power |M-N| = 1			–36		dBc
EDR adjacent channel power |M-N| = 2			–30		dBm
EDR adjacent channel power |M-N| > 2			–42		dBm

(1) Values reflect default maximum power. Max power can be changed using a VS command.

5.8.4 Bluetooth Modulation, BR

over operating free-air temperature range (unless otherwise noted)

CHARACTERISTICS	CONDITION(1)		MIN	TYP	MAX	UNIT
BR –20 dB bandwidth				925	995	kHz
BR modulation characteristics	Δf1avg	Mod data = 4 1s, 4 0s: 111100001111...	145	160	170	kHz
	Δf2max ≥ limit for at least 99.9% of all Δf2max	Mod data = 1010101...	120	130		kHz
	Δf2avg, Δf1avg		85	88		%
BR carrier frequency drift	One slot packet		–25		25	kHz
	Three and five slot packet		–35		35	kHz
BR drift rate	lfk+5 – fkl , k = 0 …. max				15	kHz/50 µs
BR initial carrier frequency tolerance(2)	f0–fTX		±75		±75	kHz

(1) Performance values reflect maximum power.
(2) Numbers include XTAL frequency drift over temperature and aging.

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5.8.5 *Bluetooth* Modulation, EDR

over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)	CONDITION	MIN	TYP	MAX	UNIT
EDR carrier frequency stability		–5		5	kHz
EDR initial carrier frequency tolerance(2)		±75		±75	kHz
EDR RMS DEVM	EDR2		4	15	%
	EDR3		4	10	%
EDR 99% DEVM	EDR2			30	%
	EDR3			20	%
EDR peak DEVM	EDR2		9	25	%
	EDR3		9	18	%

(1) Performance values reflect maximum power.
(2) Numbers include XTAL frequency drift over temperature and aging.

5.9 *Bluetooth* LE Performance

All RF and performance numbers are aligned to the module pin.

5.9.1 *Bluetooth* LE Receiver Characteristics – In-Band Signals

over operating free-air temperature range (unless otherwise noted)

PARAMETER	CONDITION(1)	MIN	TYP	MAX	UNIT
Bluetooth LE operation frequency range		2402		2480	MHz
Bluetooth LE channel spacing			2		MHz
Bluetooth LE input impedance			50		Ω
Bluetooth LE sensitivity(2) Dirty TX on			–92.2		dBm
Bluetooth LE maximum usable input power		–5			dBm
Bluetooth LE intermodulation characteristics	Level of interferers. For n = 3, 4, 5	–36	–30		dBm
Bluetooth LE C/I performance. Note: Numbers show wanted signal-to-interfering-signal ratio. Smaller numbers indicate better C/I performance.	LE, co-channel			12	dB
	LE, adjacent ±1 MHz			0	
	LE, adjacent +2 MHz			–38	
	LE, adjacent –2 MHz			–15	
Image = –1 MHz	LE, adjacent ≥ |±3|MHz			–40	

(1) BER of 0.1% corresponds to PER of 30.8% for a minimum of 1500 transmitted packets, according to the *Bluetooth* LE test specification.
(2) Sensitivity degradation of up to –3 dB can occur due to fast clock harmonics.

5.9.2 *Bluetooth* LE Transmitter Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
Bluetooth LE RF output power(1)	VBAT ≥ 3 V		10.0		dBm
	VBAT < 3 V		7.2		dBm
Bluetooth LE adjacent channel power |M-N| = 2			–51.0		dBm
Bluetooth LE adjacent channel power |M-N| > 2			–54.0		dBm

(1) To reduce the maximum BLE power, use a VS command. The optional extra margin is offered to compensate for design losses, such as trace and filter losses, and to achieve the maximum allowed output power at system level.

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5.9.3 *Bluetooth* LE Modulation Characteristics

over operating free-air temperature range (unless otherwise noted)

CHARACTERISTICS	CONDITION(1)		MIN	TYP	MAX	UNIT
Bluetooth LE modulation characteristics	Δf1avg	Mod data = 4 1s, 4 0s: 111100001111...	240	250	260	kHz
	Δf2max ≥ limit for at least 99.9% of all Δf2max	Mod data = 1010101...	195	215		kHz
	Δf2avg, Δf1avg		85	90		%
Bluetooth LE carrier frequency drift	lf0 – fnl , n = 2,3 …. K		–25		25	kHz
Bluetooth LE drift rate	lf1 – f0l and lfn – fn-5l ,n = 6,7…. K				15	kHz/50 µs
LE initial carrier frequency tolerance(2)	fn – fTX		±75		±75	kHz

(1) Performance values reflect maximum power.
(2) Numbers include XTAL frequency drift over temperature and aging.

5.10 *Bluetooth*-BLE Dynamic Currents

Current is measured at output power as follows:

- BR at 12.7 dBm
- EDR at 7.2 dBm

USE CASE(1) (2)	TYP	UNIT
BR voice HV3 + sniff	11.6	mA
EDR voice 2-EV3 no retransmission + sniff	5.9	mA
Sniff 1 attempt 1.28 s	178.0	µA
EDR A2DP EDR2 (master). SBC high quality – 345 Kbs	10.4	mA
EDR A2DP EDR2 (master). MP3 high quality – 192 Kbs	7.5	mA
Full throughput ACL RX: RX-2DH5(3)(4)	18.0	mA
Full throughput BR ACL TX: TX-DH5(4)	50.0	mA
Full throughput EDR ACL TX: TX-2DH5(4)	33.0	mA
Page scan or inquiry scan (scan interval is 1.28 s or 11.25 ms, respectively)	253.0	µA
Page scan and inquiry scan (scan interval is 1.28 s and 2.56 s, respectively)	332.0	µA

(1) The role of *Bluetooth* in all scenarios except A2DP is slave.
(2) CL1P5 PA is connected to VBAT, 3.7 V.
(3) ACL RX has the same current in all modulations.
(4) Full throughput assumes data transfer in one direction.

5.11 Bluetooth LE Currents

All current measured at output power of 7.2 dBm

USE CASE(1)	TYP	UNIT
Advertising, not connectable(2)	131	µA
Advertising, discoverable(2)	143	µA
Scanning(3)	266	µA
Connected, master role, 1.28-s connect interval(4)	124	µA
Connected, slave role, 1.28-s connect interval (4)	132	µA

(1) CL1p% PA is connected to VBAT, 3.7 V.
(2) Advertising in all three channels, 1.28-s advertising interval, 15 bytes advertise data
(3) Listening to a single frequency per window, 1.28-s scan interval, 11.25-ms scan window
(4) Zero slave connection latency, empty TX and RX LL packets

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5.12 Timing and Switching Characteristics

5.12.1 Power Management

5.12.1.1 Block Diagram – Internal DC2DCs

The device incorporates three internal DC2DCs (switched-mode power supplies) to provide efficient internal supplies, derived from V_{BAT}.

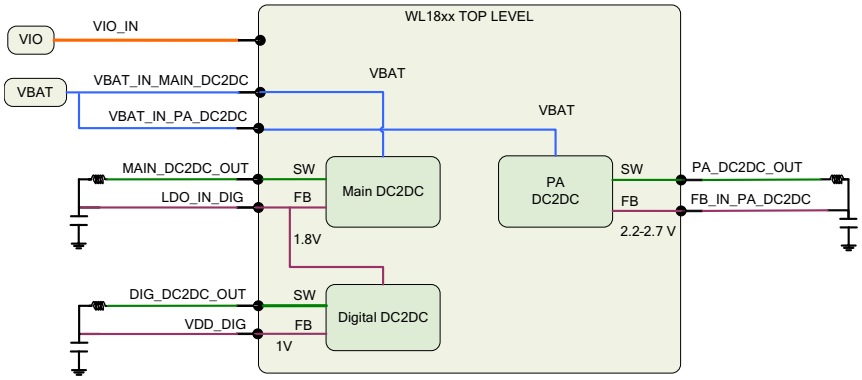

Figure 5-1. Internal DC2DCs

5.12.2 Power-Up and Shut-Down States

The correct power-up and shut-down sequences must be followed to avoid damage to the device.

While V_{BAT} or V_{IO} or both are deasserted, no signals should be driven to the device. The only exception is the slow clock that is a fail-safe I/O.

While V_{BAT}, V_{IO}, and slow clock are fed to the device, but WL_EN is deasserted (low), the device is in SHUTDOWN state. In SHUTDOWN state all functional blocks, internal DC2DCs, clocks, and LDOs are disabled.

To perform the correct power-up sequence, assert (high) WL_EN. The internal DC2DCs, LDOs, and clock start to ramp and stabilize. Stable slow clock, V_{IO}, and V_{BAT} are prerequisites to the assertion of one of the enable signals.

To perform the correct shut-down sequence, deassert (low) WL_EN while all the supplies to the device (V_{BAT}, V_{IO}, and slow clock) are still stable and available. The supplies to the chip (V_{BAT} and V_{IO}) can be deasserted only after both enable signals are deasserted (low).

Figure 5-2 shows the general power scheme for the module, including the powerdown sequence.

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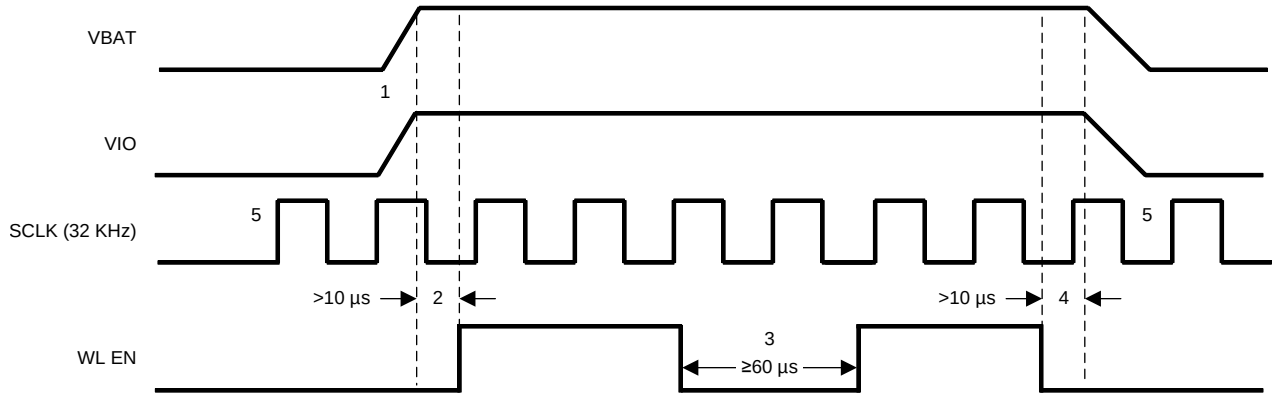

NOTE: 1. Either VBAT or VIO can come up first.
2. VBAT and VIO supplies and slow clock (SCLK), must be stable prior to EN being asserted and at all times when the EN is active.
3. At least 60 µs is required between two successive device enables. The device is assumed to be in shutdown state during that period, meaning all enables to the device are LOW for that minimum duration.
4. EN must be deasserted at least 10 µs before VBAT or VIO supply can be lowered. (Order of supply turn off after EN shutdown is immaterial)
5. SCLK - Fail safe I/O

Figure 5-2. Power-Up System

5.12.3 Chip Top-level Power-Up Sequence

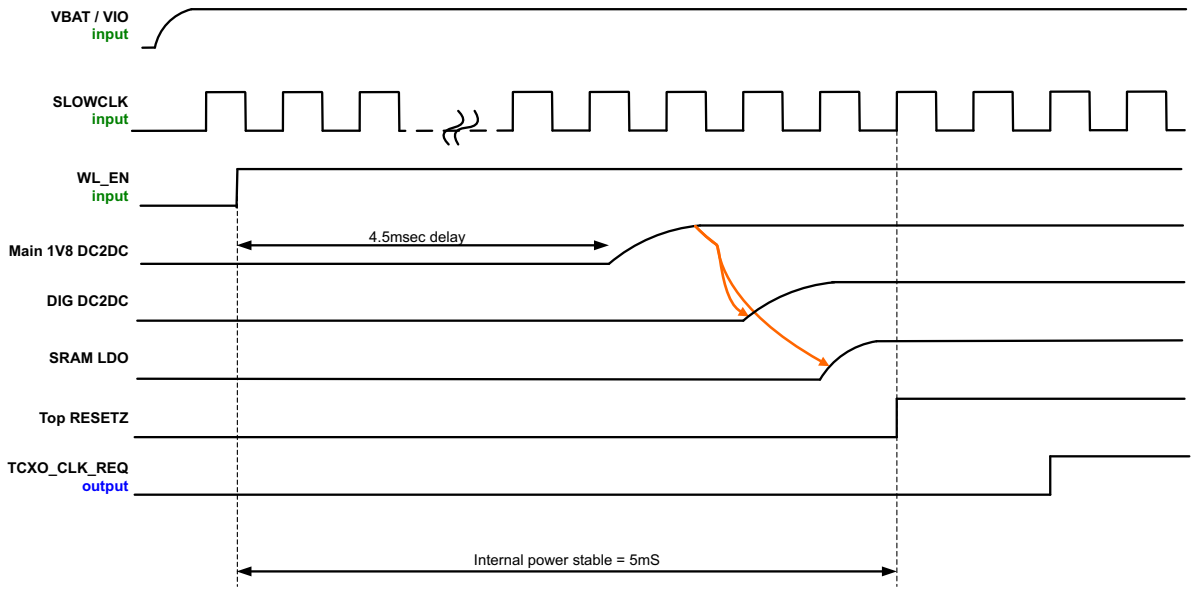

Figure 5-3. Chip Top-Level Power-Up Sequence

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5.12.4 WLAN Power-Up Sequence

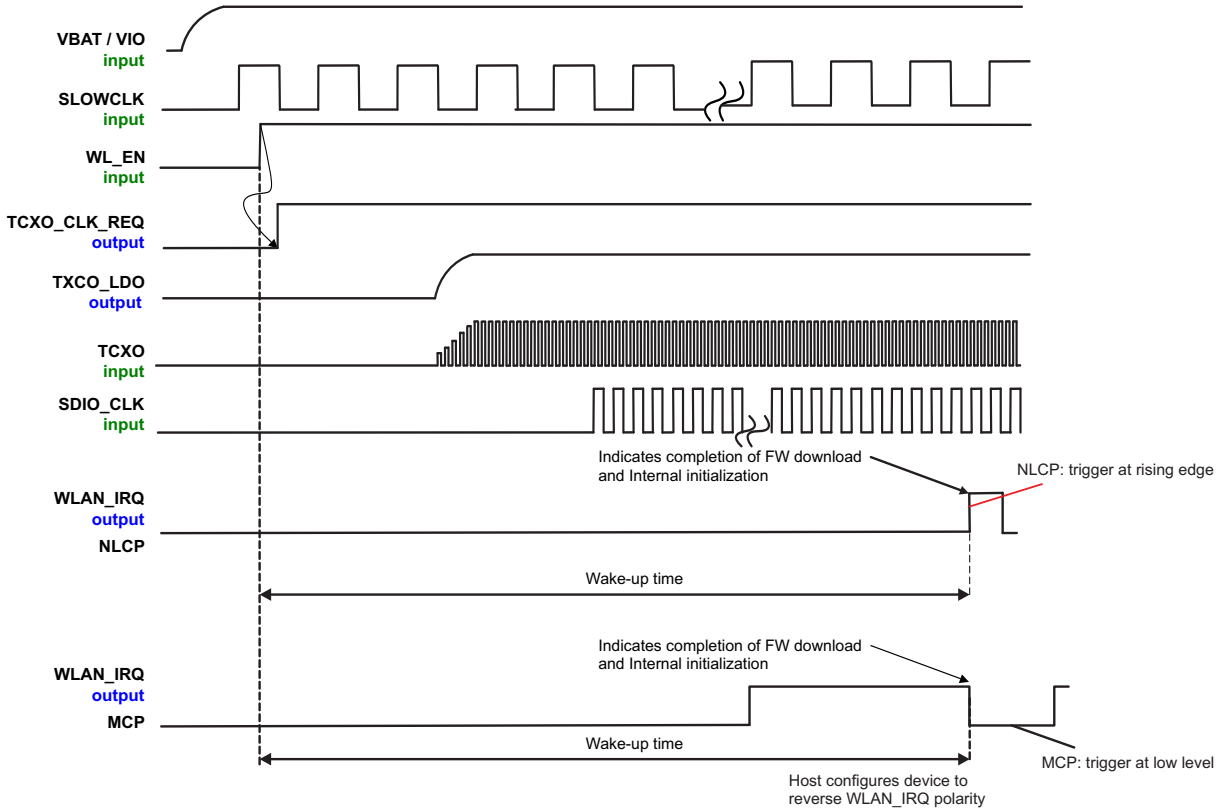

Figure 5-4. WLAN Power-Up Sequence

5.12.5 Bluetooth-BLE Power-Up Sequence

Figure 5-5 shows the *Bluetooth*-BLE power-up sequence.

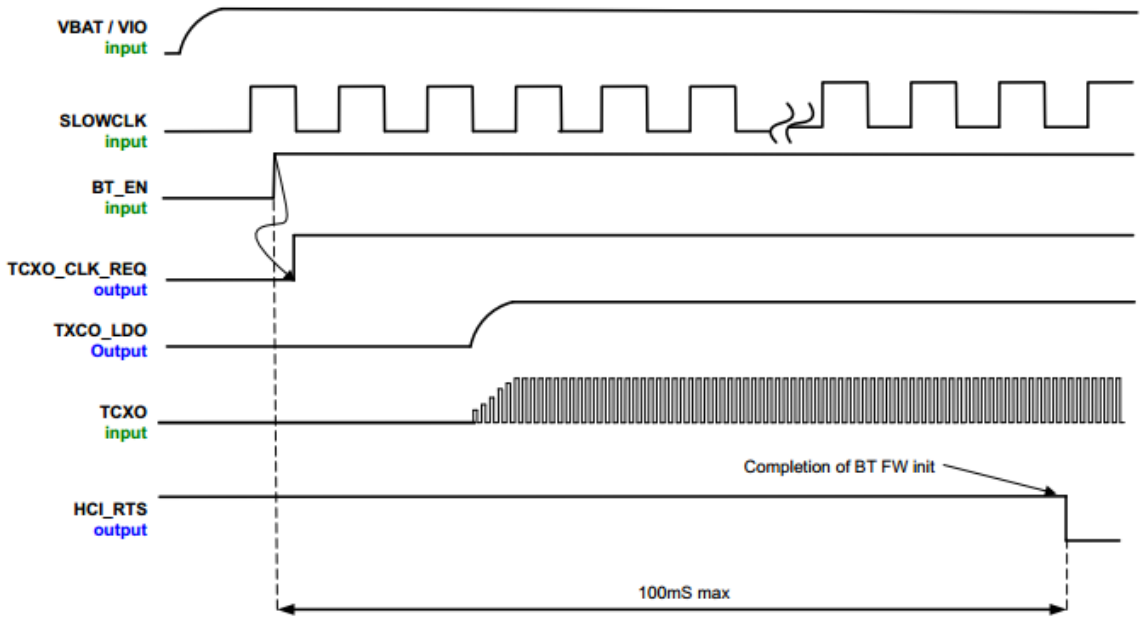

Figure 5-5. Bluetooth/BLE Power-Up Sequence

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5.12.6 WLAN SDIO Transport Layer

The SDIO is the host interface for WLAN. The interface between the host and the WL18xx module uses an SDIO interface and supports a maximum clock rate of 50 MHz.

The device SDIO also supports the following features of the SDIO V3 specification:

- 4-bit data bus
- Synchronous and asynchronous in-band interrupt
- Default and high-speed (HS, 50 MHz) timing
- Sleep and wake commands

5.12.6.1 SDIO Timing Specifications

Figure 5-6 and Figure 5-7 show the SDIO switching characteristics over recommended operating conditions and with the default rate for input and output.

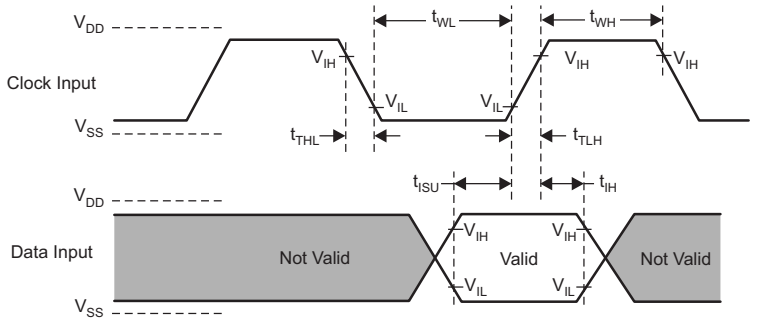

Figure 5-6. SDIO Default Input Timing

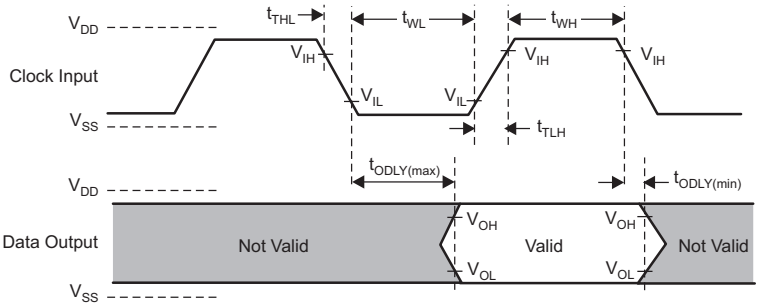

Figure 5-7. SDIO Default Output Timing

Table 5-1 lists the SDIO default timing characteristics.

Table 5-1. SDIO Default Timing Characteristics (1)

PARAMETER (2)		MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK	0.0	26.0	MHz
DC	Low, high duty cycle	40.0	60.0	%
t_{TLH}	Rise time, CLK		10.0	ns
t_{THL}	Fall time, CLK		10.0	ns
t_{ISU}	Setup time, input valid before CLK ↑	3.0		ns
t_{IH}	Hold time, input valid after CLK ↑	2.0		ns
t_{ODLY}	Delay time, CLK ↓ to output valid	7.0	10.0	ns
C_l	Capacitive load on outputs		15.0	pF

(1) To change the data out clock edge from the falling edge (default) to the rising edge, set the configuration bit.
(2) Parameter values reflect maximum clock frequency.

5.12.6.2 SDIO Switching Characteristics – High Rate

Figure 5-8 and Figure 5-9 show the parameters for maximum clock frequency.

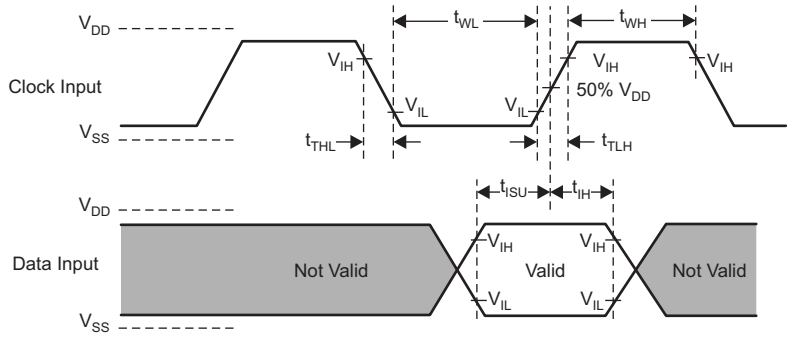

Figure 5-8. SDIO HS Input Timing

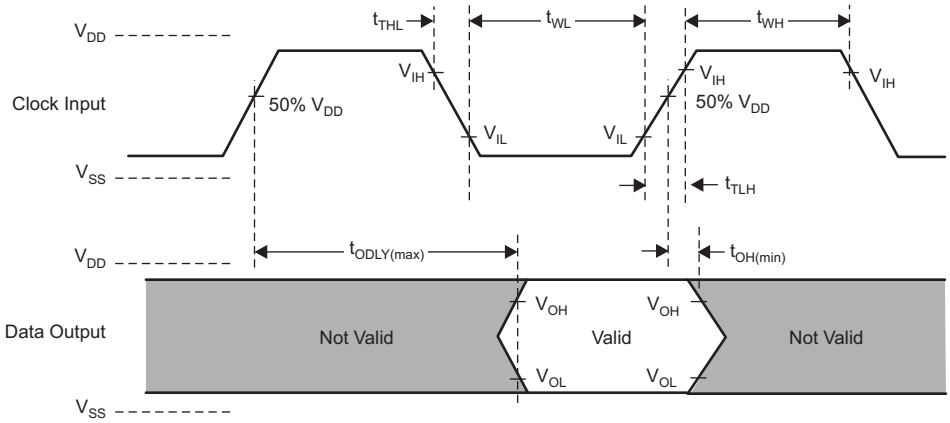

Figure 5-9. SDIO HS Output Timing

Table 5-2 lists the SDIO high-rate timing characteristics.

Table 5-2. SDIO HS Timing Characteristics

PARAMETER		MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK	0.0	52.0	MHz
DC	Low, high duty cycle	40.0	60.0	%
t_{TLH}	Rise time, CLK		3.0	ns
t_{THL}	Fall time, CLK		3.0	ns
t_{ISU}	Setup time, input valid before CLK ↑	3.0		ns
t_{IH}	Hold time, input valid after CLK ↑	2.0		ns
t_{ODLY}	Delay time, CLK ↑ to output valid	7.0	10.0	ns
C_l	Capacitive load on outputs		10.0	pF

5.12.7 HCI UART Shared Transport Layers for All Functional Blocks (Except WLAN)

The device incorporates a UART module dedicated to the *Bluetooth* shared-transport, host controller interface (HCI) transport layer. The HCI interface transports commands, events, and ACL between the *Bluetooth* device and its host using HCI data packets acting as a shared transport for all functional blocks except WLAN.

WLAN	SHARED HCI FOR ALL FUNCTIONAL BLOCKS EXCEPT WLAN	*BLUETOOTH* VOICE-AUDIO
WLAN HS SDIO	Over UART	*Bluetooth* PCM

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The HCI UART supports most baud rates (including all PC rates) for all fast-clock frequencies up to a maximum of 4 Mbps. After power up, the baud rate is set for 115.2 kbps, regardless of the fast-clock frequency. The baud rate can then be changed using a VS command. The device responds with a Command Complete Event (still at 115.2 kbps), after which the baud rate change occurs.

HCI hardware includes the following features:

- Receiver detection of break, idle, framing, FIFO overflow, and parity error conditions
- Receiver-transmitter underflow detection
- CTS, RTS hardware flow control
- 4 wire (H4)

Table 5-3 lists the UART default settings.

Table 5-3. UART Default Setting

PARAMETER	VALUE
Bit rate	115.2 kbps
Data length	8 bits
Stop bit	1
Parity	None

5.12.7.1 UART 4-Wire Interface – H4

The interface includes four signals:

- TXD
- RXD
- CTS
- RTS

Flow control between the host and the device is byte-wise by hardware.

When the UART RX buffer of the device passes the flow-control threshold, the buffer sets the UART_RTS signal high to stop transmission from the host. When the UART_CTS signal is set high, the device stops transmitting on the interface. If HCI_CTS is set high in the middle of transmitting a byte, the device finishes transmitting the byte and stops the transmission.

Figure 5-10 shows the UART timing.

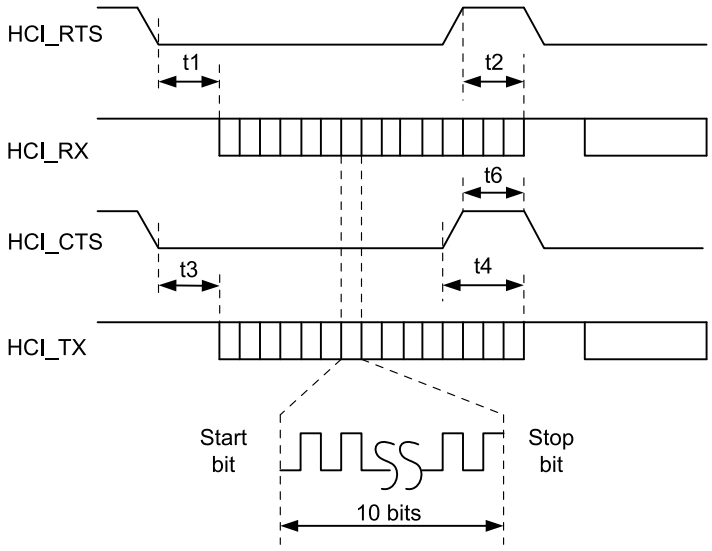

Figure 5-10. UART Timing Diagram

Table 5-4 lists the UART timing characteristics.

Table 5-4. UART Timing Characteristics

PARAMETER	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Baud rate			37.5		4364	Kbps
Baud rate accuracy per byte	Receive-transmit		–2.5		+1.5	%
Baud rate accuracy per bit	Receive-transmit		–12.5		+12.5	%
CTS low to TX_DATA on		t3	0.0	2.0		µs
CTS high to TX_DATA off	Hardware flow control	t4			1.0	Byte
CTS high pulse width		t6	1.0			Bit
RTS low to RX_DATA on		t1	0.0	2.0		µs
RTS high to RX_DATA off	Interrupt set to 1/4 FIFO	t2			16.0	Bytes

Figure 5-11 shows the UART data frame.

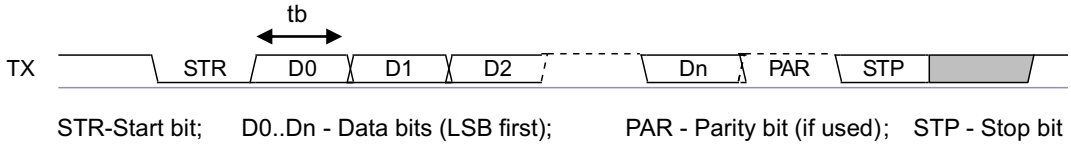

Figure 5-11. UART Data Frame

5.12.8 Bluetooth Codec-PCM (Audio) Timing Specifications

Figure 5-12 shows the *Bluetooth* codec-PCM (audio) timing diagram.

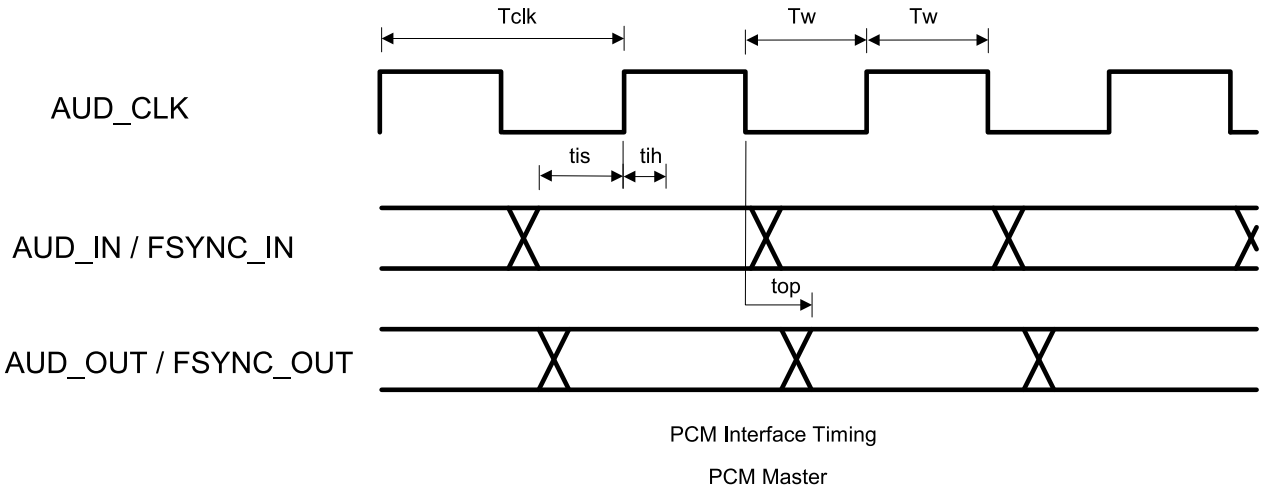

Figure 5-12. *Bluetooth* Codec-PCM (Audio) Master Timing Diagram

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Table 5-5 lists the *Bluetooth* codec-PCM master timing characteristics.

Table 5-5. *Bluetooth* Codec-PCM Master Timing Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNIT
Cycle time	T_{clk}	162.76 (6.144 MHz)	15625 (64 kHz)	ns
High or low pulse width	T_s	35% of T_{clk} min		
AUD_IN setup time	t_{is}	10.6		
AUD_IN hold time	t_{ih}	0		
AUD_OUT propagation time	t_{op}	0	15	
FSYNC_OUT propagation time	t_{op}	0	15	
Capacitive loading on outputs	C_l		40	pF

Table 5-6 lists the *Bluetooth* codec-PCM slave timing characteristics.

Table 5-6. *Bluetooth* Codec-PCM Slave Timing Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNIT
Cycle time	T_{clk}	81.38 (12.266 MHz)		ns
High or low pulse width	T_w	35% of T_{clk} min		
AUD_IN setup time	t_{is}	5		
AUD_IN hold time	t_{ih}	0		
AUD_FSYNC setup time	t_{is}	5		
AUD_FSYNC hold time	t_{ih}	0		
AUD_OUT propagation time	t_{op}	0	19	
Capacitive loading on outputs	C_l		40	pF

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6 Detailed Description

The WiLink 8 module is a self-contained connectivity solution based on WiLink 8 connectivity. As the eighth-generation connectivity combo chip from TI, the WiLink 8 module is based on proven technology.

Table 6-1 through Table 6-3 list performance parameters along with shutdown and sleep currents.

Table 6-1. WLAN Performance Parameters

WLAN(1)	SPECIFICATION (TYP)	CONDITIONS
Maximum TX power	17.3 dBm	1 Mbps DSSS
Minimum sensitivity	–96.3 dBm	1 Mbps DSSS
Sleep current	160 µA	Leakage, firmware retained
Connected IDLE	750 µA	No traffic IDLE connect
RX search	54 mA	Search (SISO20)
RX current (SISO20)	65 mA	MCS7, 2.4 GHz
TX current (SISO20)(2)	238 mA	MCS7, 2.4 GHz, +11.2 dBm
Maximum peak current consumption during calibration(3)	850 mA	

(1) System design power scheme must comply with both peak and average TX bursts.
(2) WLAN maximum VBAT current draw of 725 mA with MIMO continues burst configuration.
(3) Peak current VBAT can hit 850 mA during device calibration.
- At wakeup, the WiLink 8 module performs the entire calibration sequence at the center of the 2.4-GHz band.
- Once a link is established, calibration is performed periodically (every 5 minutes) on the specific channel tuned.
- The maximum VBAT value is based on peak calibration consumption with a 30% margin.

Table 6-2. *Bluetooth* Performance Parameters

BLUETOOTH	SPECIFICATION (TYP)	CONDITIONS
Maximum TX power	12.7 dBm	GFSK
Minimum sensitivity	–92.2 dBm	GFSK
Sniff	178 µA	1 attempt, 1.28 s (+4 dBm)
Page or inquiry	253 µA	1.28-s interrupt, 11.25-ms scan window (+4 dBm)
A2DP	7.5 mA	MP3 high quality 192 kbps (+4 dBm)

Table 6-3. Shutdown and Sleep Currents

PARAMETER	POWER SUPPLY CURRENT	TYP	UNIT
Shutdown mode All functions shut down	VBAT	10	µA
	VIO	2	µA
WLAN sleep mode	VBAT	160	µA
Bluetooth sleep mode	VBAT	110	µA

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Figure 6-1 shows a high-level view of the WL1837MOD variant.

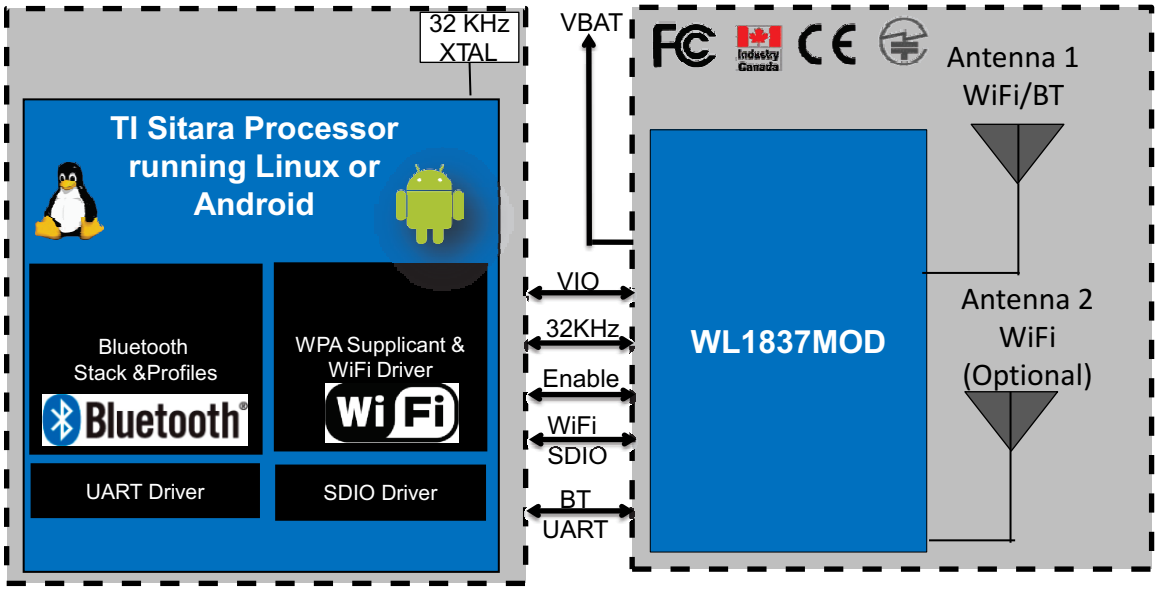

Figure 6-1. WL1837MOD High-Level System Diagram

6.1 WLAN

The device supports the following WLAN features:

- Integrated 2.4-GHz power amplifiers (PAs) for a complete WLAN solution
- Baseband processor: IEEE Std 802.11a, 802.11b/g, and IEEE Std 802.11n data rates with 20- or 40-MHz SISO and 20-MHz MIMO
- Fully calibrated system (production calibration not required)
- Medium access controller (MAC)
  - Embedded ARM® central processing unit (CPU)
  - Hardware-based encryption-decryption using 64-, 128-, and 256-bit WEP, TKIP, or AES keys
  - Requirements for Wi-Fi-protected access (WPA and WPA2.0) and IEEE Std 802.11i (includes hardware-accelerated Advanced Encryption Standard [AES])
- New advanced coexistence scheme with *Bluetooth* and BLE
- 2.4- and 5-GHz radio
  - Internal LNA and PA
  - IEEE Std 802.11a, 802.11b, 802.11g, and 802.11n
- 4-bit SDIO host interface, including high speed (HS) and V3 modes

6.2 *Bluetooth*

The device supports the following *Bluetooth* features:

- *Bluetooth* 4.1 as well as CSA2
- Concurrent operation and built-in coexisting and prioritization handling of *Bluetooth*, BLE, audio processing, and WLAN
- Dedicated audio processor supporting on-chip SBC encoding + A2DP
  - Assisted A2DP (A3DP): SBC encoding implemented internally
  - Assisted WB-speech (AWBS): modified SBC codec implemented internally

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6.3 BLE

The device supports the following BLE features:

- *Bluetooth* 4.0 BLE dual-mode standard
- All roles and role combinations, mandatory as well as optional
- Up to 10 BLE connections
- Independent LE buffering allowing many multiple connections with no affect on BR-EDR performance

6.4 WiLink 8 Module Markings

Figure 6-2 shows the markings for the TI WiLink 8 module.

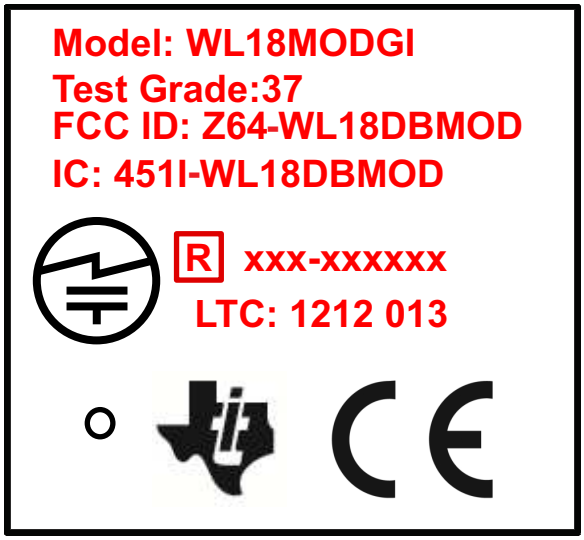

Figure 6-2. WiLink 8 Module Markings

Table 6-4 describes the WiLink 8 module markings.

Table 6-4. Description of WiLink 8 Module Markings

MARKING	DESCRIPTION
WL18 MODGI	Model
37	Test grade (for more information, see Section 6.5, *Test Grades*)
Z64-WL18DBMOD	FCC ID: single modular FCC grant ID
451I-WL18DBMOD	IC: single modular IC grant ID
TBD	R: single modular TELEC grant ID
YYWWSSF	LTC (lot trace code): • YY = year (for example, 12 = 2012) • WW = week • SS = serial number (01 to 99) matching manufacturer lot number • F = Reserved for internal use
TBD	R: dual modular TELEC grant ID
	TELEC compliance mark
CE	CE compliance mark

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6.5 Test Grades

To minimize delivery time, TI may ship the device ordered or an equivalent device currently available that contains at least the functions of the part ordered. From all aspects, this device will behave exactly the same as the part ordered. For example, if a customer orders device WL1807MOD, the part shipped can be marked with a test grade of 37, 07 (see Table 6-5).

Table 6-5. Test Grade Markings

MARK 1	WLAN	*BLUETOOTH*
0&	Tested	–
3&	Tested	Tested
MARK 2	**WLAN 2.4 and 5 GHz**	**MIMO 2.4 GHz**
&7	Tested	Tested

7 Applications and Implementation

7.1 Application Information

7.1.1 Typical Application – WL1837MOD Reference Design

Figure 7-1 shows the TI WL1837MOD reference design.

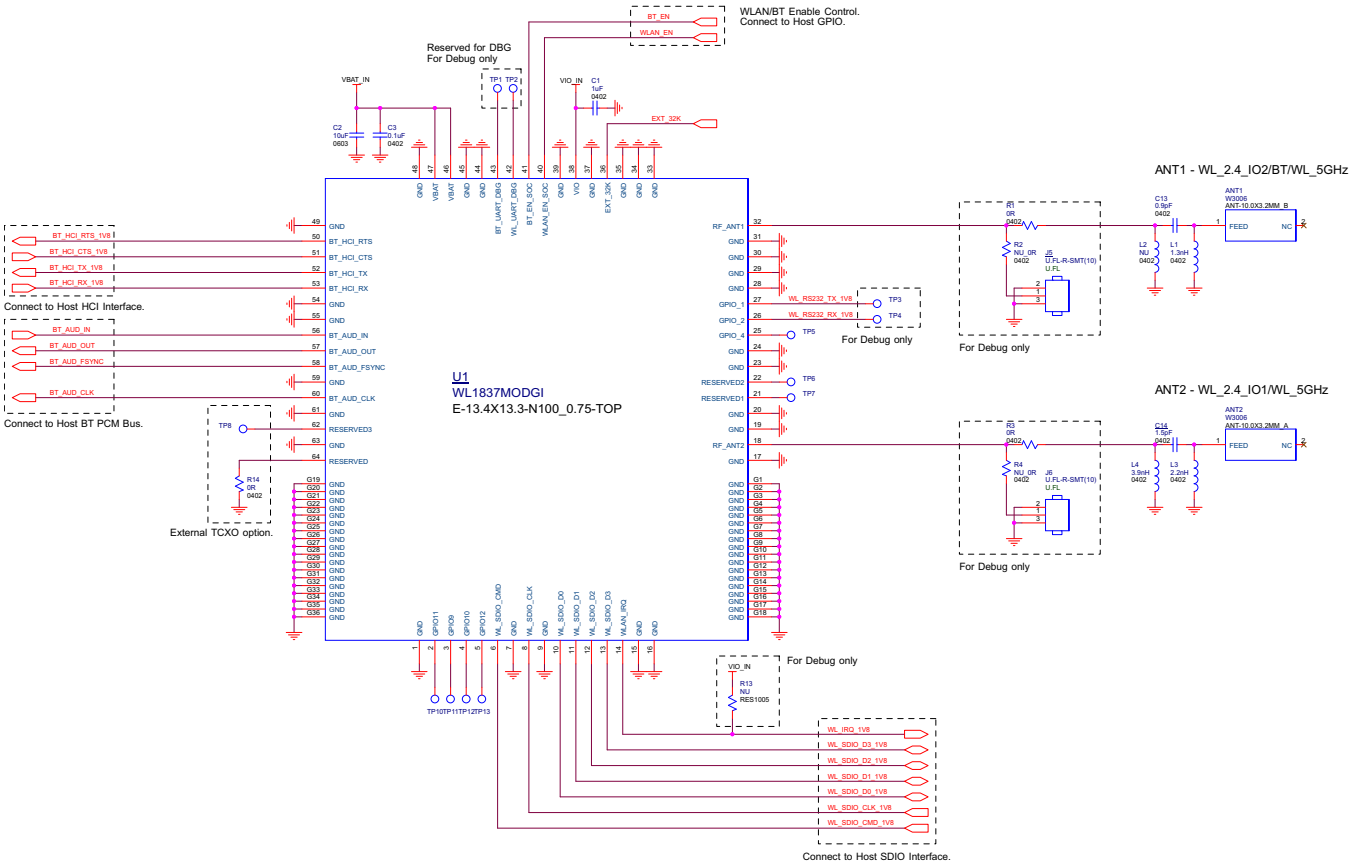

Figure 7-1. TI Module Reference Schematics

Table 7-1 lists the bill materials (BOM).

Table 7-1. Bill of Materials

DESCRIPTION	PART NUMBER	PACKAGE	REFERENCE	QTY	MFR
TI WL1837 Wi-Fi/Bluetooth Module	WL1837MODGI	13.4 × 13.3 × 2.0 mm	U1	1	TI
ANT/Chip/2.4 and 5 GHz (1)	W3006	10.0 × 3.2 × 1.5 mm	ANT1, ANT2	2	Pulse
Mini RF Header Receptacle	U.FL-R-SMT-1(10)	3.0 × 2.6 × 1.25 mm	J5, J6	2	Hirose
IND 0402/1 nH/±0.3 nH/70 mΩ/300 mA	LQG15HS1N0S02D	0402	L1, L3	2	Murata
Capacitor 0402/10 pF/50 V/NPO/±5%	0402N100J500LT	0402	C7, C8, C13, C14	4	Walsin
Capacitor 0402/0.1 µF/10 V/X7R/±10%	0402B104K100CT	0402	C3, C4	2	Walsin
Capacitor 0402/1 µF/6.3 V/X5R/±10%/HF	GRM155R60J105KE19D	0402	C1	1	Murata
Capacitor 0603/10 µF/6.3 V/X5R/±20%	C1608X5R0J106M	0603	C2	1	TDK
Resistor 0402/10K/±5%	WR04X103 JTL	0402	R20	1	Walsin
Resistor 0603/0R/±5%	WR06X000 PTL	0603	R31, R32	2	Walsin

(1) For more information see productfinder.pulseeng.com/product/W3006.

PRODUCT PREVIEW

7.1.2 Design Recommendations

This section describes the layout recommendations for the (X)WL1837 module, RF trace, and antenna.

Table 7-2 summarizes the layout recommendations.

Table 7-2. Layout Recommendations Summary

ITEM	DESCRIPTION
	Thermal
1	The proximity of ground vias must be close to the pad.
2	Signal traces must not be run underneath the module on the layer where the module is mounted.
3	Have a complete ground pour in layer 2 for thermal dissipation.
4	Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
5	Increase the ground pour in the first layer and have all of the traces from the first layer on the inner layers, if possible.
6	Signal traces can be run on a third layer under the solid ground layer, which is below the module mounting layer.
	RF Trace and Antenna Routing
7	The RF trace antenna feed must be as short as possible beyond the ground reference. At this point, the trace starts to radiate.
8	The RF trace bends must be gradual with an approximate maximum bend of 45 degrees with trace mitered. RF traces must not have sharp corners.
9	RF traces must have via stitching on the ground plane beside the RF trace on both sides.
10	RF traces must have constant impedance (microstrip transmission line).
11	For best results, the RF trace ground layer must be the ground layer immediately below the RF trace. The ground layer must be solid.
12	There must be no traces or ground under the antenna section.
13	RF traces must be as short as possible. The antenna, RF traces, and modules must be on the edge of the PCB product. The proximity of the antenna to the enclosure and the enclosure material must also be considered.
	Supply and IF
14	The power trace for VBAT must be at least 40-mil wide.
15	The 1.8-V trace must be at least 18-mil wide.
16	Make VBAT traces as wide as possible to ensure reduced inductance and trace resistance.
17	If possible, shield VBAT traces with ground above, below, and beside the traces.
18	SDIO signals traces (CLK, CMD, D0, D1, D2, and D3) must be routed in parallel to each other and as short as possible (less than 12 cm). In addition, every trace length must be the same as the others. There should be enough space between traces – greater than 1.5 times the trace width or ground – to ensure signal quality, especially for the SDIO_CLK trace. Remember to keep these traces away from the other digital or analog signal traces. TI recommends adding ground shielding around these buses.
19	SDIO and digital clock signals are a source of noise. Keep the traces of these signals as short as possible. If possible, maintain a clearance around them.

7.1.3 RF Trace and Antenna Layout Recommendations

Figure 7-2 shows the location of the antenna on the WL1837MODCOM8 board as well as the RF trace routing from the (X)WL1837 module (TI reference design). The TDK chip multilayer antennas are mounted on the board with a specific layout and matching circuit for the radiation test conducted in FCC, CE, and IC certifications.

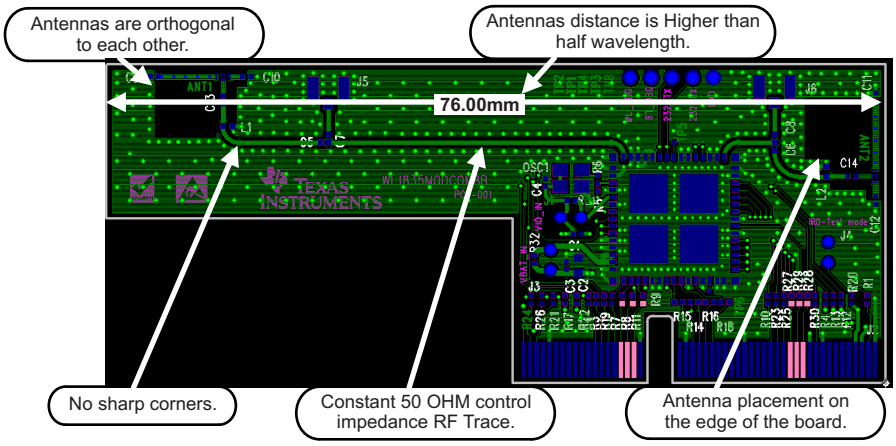

Figure 7-2. Location of Antenna and RF Trace Routing on the TMDXWL1837MODCOM8T Board

Follow these RF trace routing recommendations:

- RF traces must have 50-Ω impedance.
- RF traces must not have sharp corners.
- RF traces must have via stitching on the ground plane beside the RF trace on both sides.
- RF traces must be as short as possible. The antenna, RF traces, and module must be on the edge of the PCB product in consideration of the product enclosure material and proximity.

7.1.4 Module Layout Recommendations

Figure 7-3 shows layer 1 and layer 2 of the TI module layout:

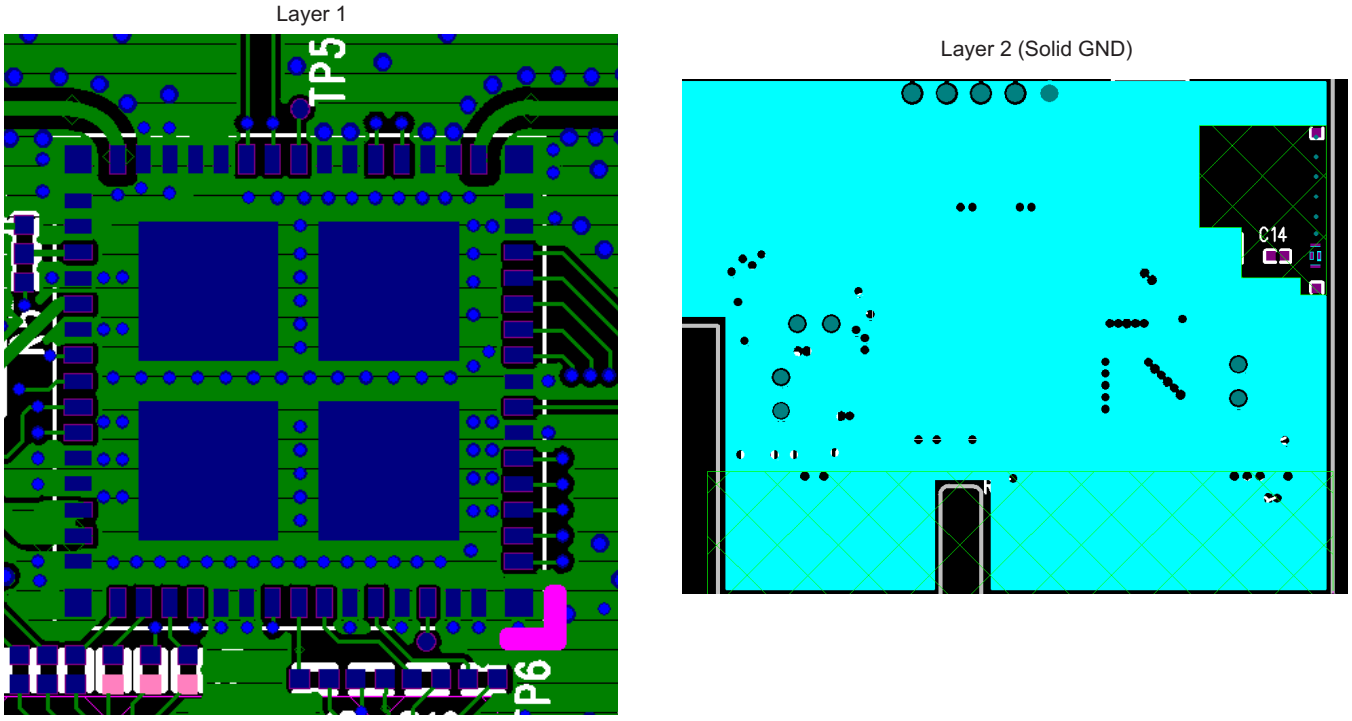

Figure 7-3. TI Module Layout

Follow these module layout recommendations:

- Ensure a solid ground plane and ground vias under the module for stable system and thermal dissipation.

PRODUCT PREVIEW

- Do not run signal traces underneath the module on a layer where the module is mounted.
- Signal traces can be run on a third layer under the solid ground layer and beneath the module mounting.
- Run the host interfaces with ground on the adjacent layer to improve the return path.
- TI recommends routing the signals as short as possible to the host.

7.1.5 Thermal Board Recommendations

The TI module uses µvias for layers 1 through 6 with full copper filling, providing heat flow all the way to the module ground pads.

TI recommends using one big ground pad under the module with vias all the way to connect the pad to all ground layers (see Figure 7-4).

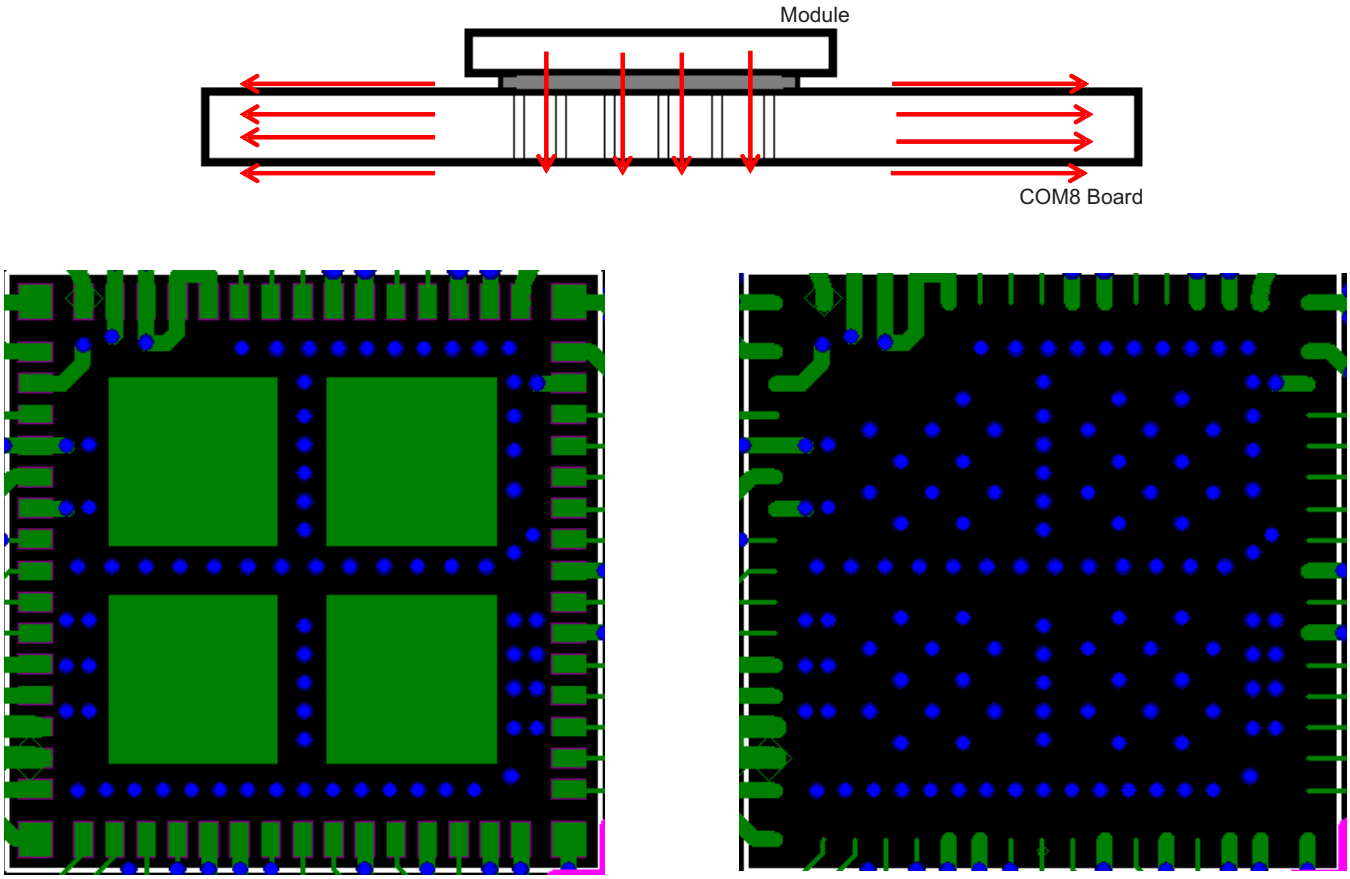

Figure 7-4. Block of Ground Pads on Bottom Side of Package

Figure 7-5 shows via array patterns, which are applied wherever possible to connect all of the layers to the TI module central or main ground pads.

Figure 7-5. Via Array Patterns

7.1.6 Baking and SMT Recommendations

7.1.6.1 Baking Recommendations

Follow these baking guidelines for the WiLink 8 module:

- Follow MSL level 3 to perform the baking process.
- After the bag is open, devices subjected to reflow solder or other high temperature processes must be mounted within 168 hours of factory conditions (< 30°C/60% RH) or stored at <10% RH.
- if the Humidity Indicator Card reads >10%, devices require baking before being mounted.
- If baking is required, bake devices for 8 hours at 125 °C.

7.1.6.2 SMT Recommendations

Figure 7-6 shows the recommended reflow profile for the WiLink 8 module.

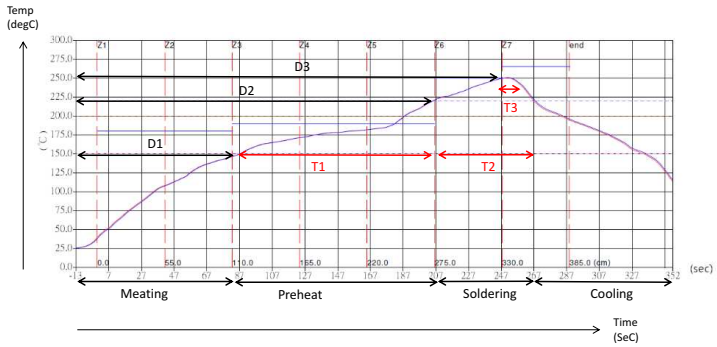

Figure 7-6. Reflow Profile for the WiLink 8 Module

Table 7-3 lists the temperature values for the profile shown in Figure 7-6.

Table 7-3. Temperature Values for Reflow Profile

ITEM	TEMPERATURE (°C)	TIME (s)
Preheat	D1 to approximately D2: 140 to 200	T1: 80 to approximately 120
Soldering	D2: 220	T2: 60 ±10
Peak temperature	D3: 250 max	T3: 10

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8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

For a complete listing of development-support tools, visit the Texas Instruments WL18xx Wiki. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

8.1.2 Device Support Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices.

X Experimental, preproduction, sample or prototype device. Device may not meet all product qualification conditions and may not fully comply with TI specifications. Experimental/Prototype devices are shipped against the following disclaimer: "This product is still in development and is intended for internal evaluation purposes." Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

null Device is qualified and released to production. TI's standard warranty applies to production devices.

8.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 **8-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
WL1807MOD	Click here	Click here	Click here	Click here	Click here
WL1837MOD	Click here	Click here	Click here	Click here	Click here

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

PRODUCT PREVIEW

8.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

9 Mechanical Packaging and Orderable Information

9.1 TI Module Mechanical Outline

图 9-1 shows the mechanical outline for the device.

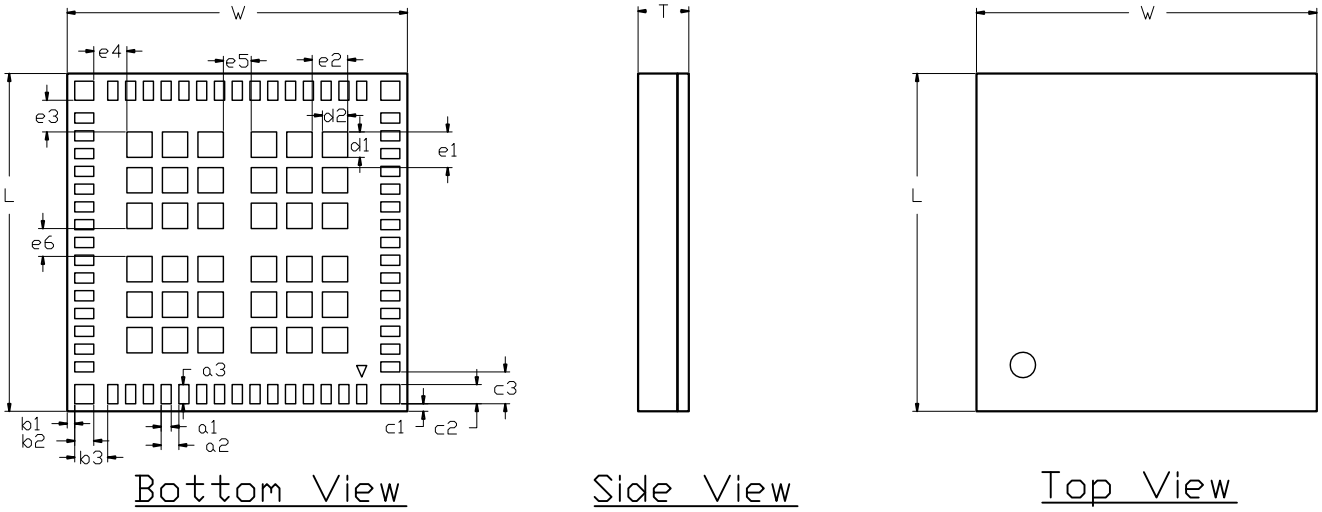

图 **9-1. TI Module Mechanical Outline**

表 9-1 lists the dimensions for the mechanical outline of the device.

表 **9-1. Dimensions for TI Module Mechanical Outline**

MARKING	MIN (mm)	NOM (mm)	MAX (mm)	MARKING	MIN (mm)	NOM (mm)	MAX (mm)
L (body size)	13.20	13.30	13.40	c2	0.65	0.75	0.85
W (body size)	13.30	13.40	13.50	c3	1.15	1.25	1.35
T (thickness)	1.90		2.00	d1	0.90	1.00	1.10
a1	0.30	0.40	0.50	d2	0.90	1.00	1.10
a2	0.60	0.70	0.80	e1	1.30	1.40	1.50
a3	0.65	0.75	0.85	e2	1.30	1.40	1.50
b1	0.20	0.30	0.40	e3	1.15	1.25	1.35
b2	0.65	0.75	0.85	e4	1.20	1.30	1.40
b3	1.20	1.30	1.40	e5	1.00	1.10	1.20
c1	0.20	0.30	0.40	e6	1.00	1.10	1.20

PRODUCT PREVIEW

9.2 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
WL1807MODGIMOCR	ACTIVE	QFM	MOC	100	1200	Green (RoHS & no Sb/Br)	NiPdAu	Level-3-260C-168 HR	-40 to 85	WL18MODGI 07 Z64-WL18DBMOD 451I-WL18DBMOD 201-140447	Samples
WL1807MODGIMOCT	ACTIVE	QFM	MOC	100	250	Green (RoHS & no Sb/Br)	NiPdAu	Level-3-260C-168 HR	-40 to 85	WL18MODGI 07 Z64-WL18DBMOD 451I-WL18DBMOD 201-140447	Samples
WL1837MODGIMOCR	ACTIVE	QFM	MOC	100	1200	Green (RoHS & no Sb/Br)	NiPdAu	Level-3-260C-168 HR	-40 to 85	WL18MODGI 37 Z64-WL18DBMOD 451I-WL18DBMOD 201-140447	Samples
WL1837MODGIMOCT	ACTIVE	QFM	MOC	100	250	Green (RoHS & no Sb/Br)	NiPdAu	Level-3-260C-168 HR	-40 to 85	WL18MODGI 37 Z64-WL18DBMOD 451I-WL18DBMOD 201-140447	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

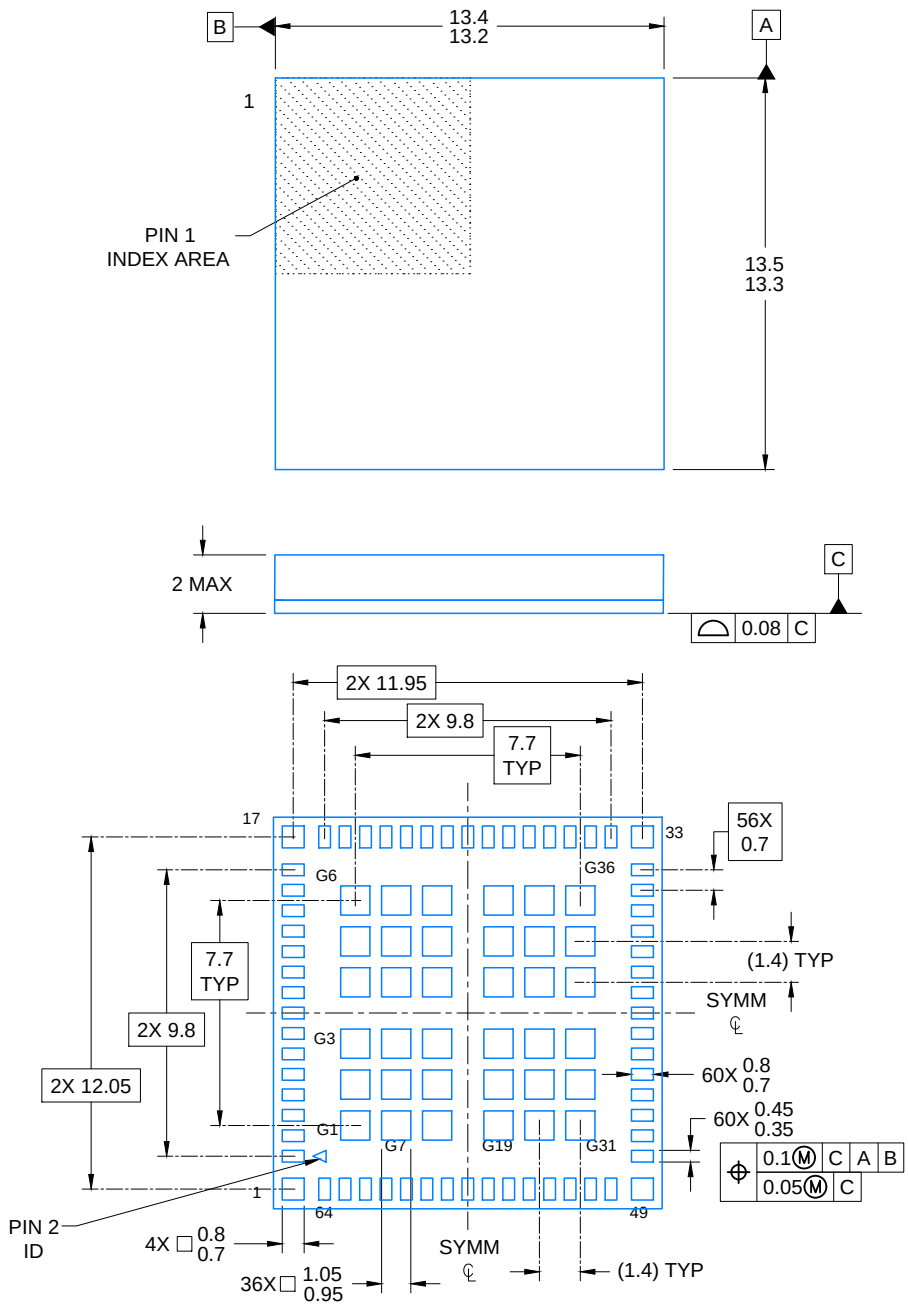
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

MOC0100A

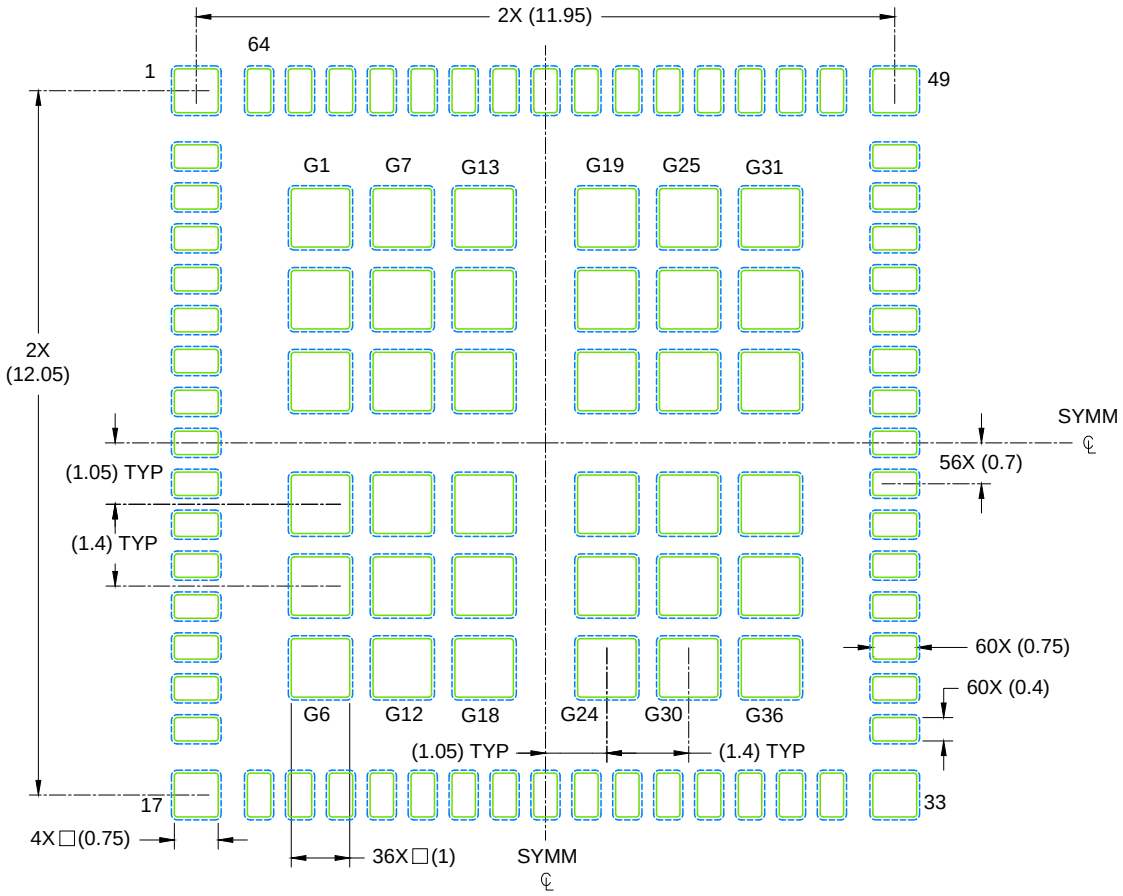
QFM - 2.0 mm max height

QUAD FLAT MODULE



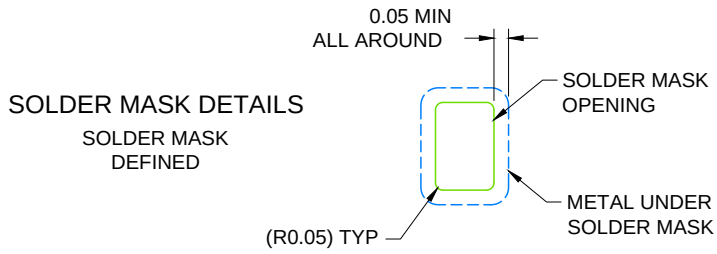
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 8X



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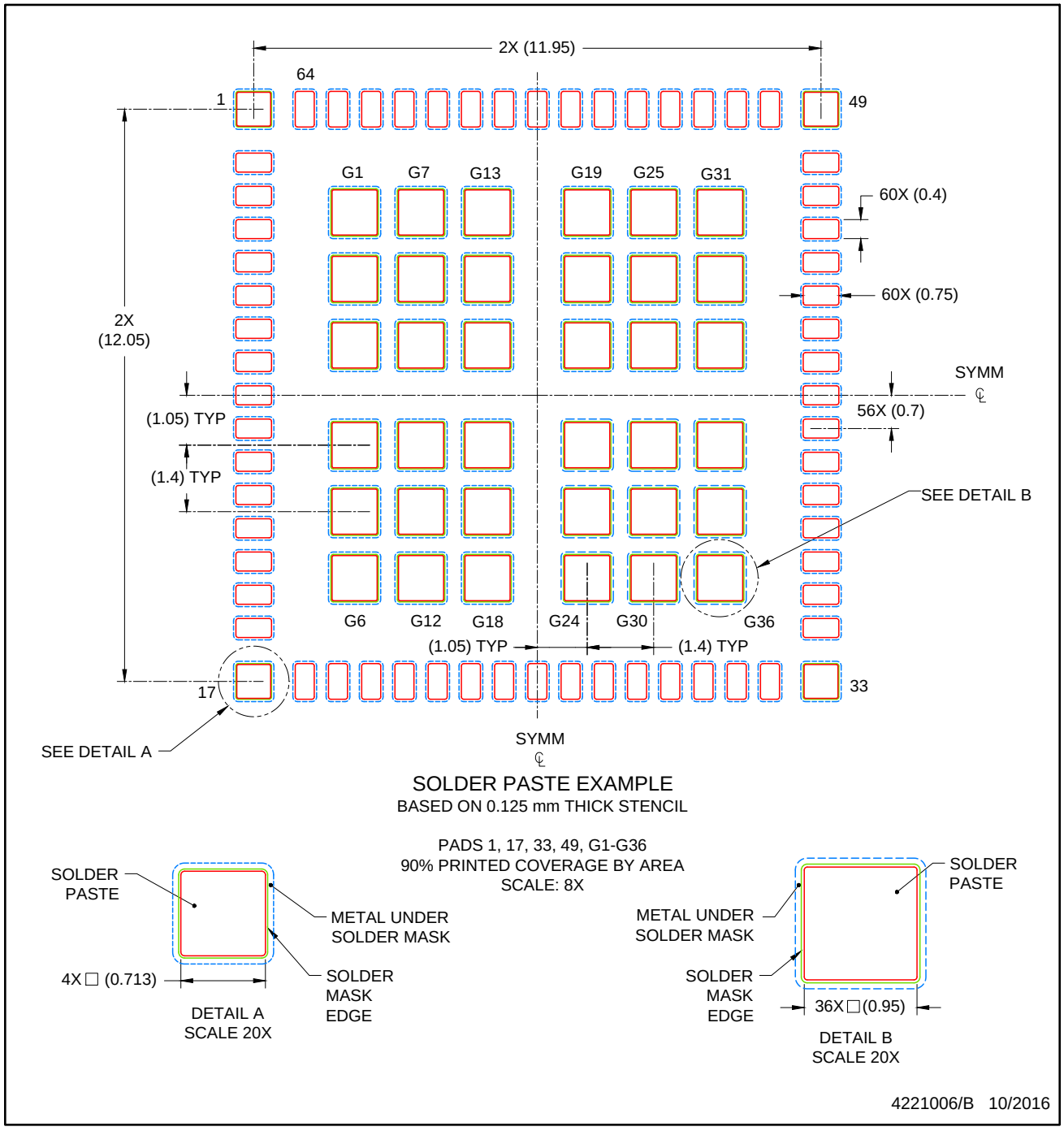
NOTES: (continued)

4. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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