

CSD85302L 20 V Dual N-Channel NexFET™ Power MOSFET

1 Features

- Common Drain Configuration
- Low On-Resistance
- Small Footprint of 1.35 mm × 1.35 mm
- Pb Free and Halogen Free
- RoHS Compliant
- ESD HBM Protection >2.5 kV

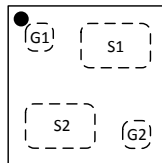
2 Applications

- USB Type-C/PD
- Battery Management
- Battery Protection

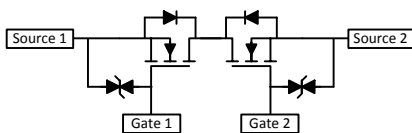
3 Description

This 20 V, 18.7 mΩ, 1.35 mm × 1.35 mm LGA Dual NexFET™ power MOSFET is designed to minimize resistance in the smallest footprint. Its small footprint and common drain configuration make the device ideal for battery-powered applications in small handheld devices.

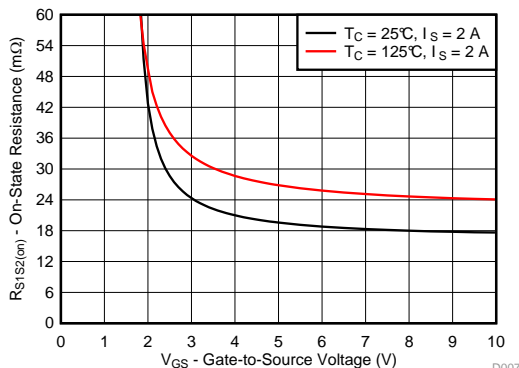
Top View



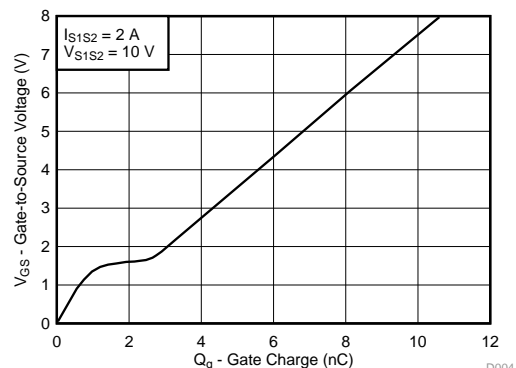
Configuration



$R_{DS(on)}$ vs V_{GS}



Gate Charge



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
V_{S1S2}	Source-to-Source Voltage	20	V
Q_g	Gate Charge Total (4.5 V)	6	nC
Q_{gd}	Gate Charge Gate-to-Drain	1.4	nC
$R_{S1S2(on)}$	Source-to-Source On-Resistance	$V_{GS} = 2.5\text{ V}$	29 mΩ
		$V_{GS} = 4.5\text{ V}$	20 mΩ
		$V_{GS} = 6.5\text{ V}$	18.7 mΩ
$V_{GS(th)}$	Threshold Voltage	0.9	V

Ordering Information⁽¹⁾

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD85302L	3000	7-Inch Reel	1.35 × 1.35 mm Land Grid Array (LGA) Package	Tape and Reel
CSD85302LT	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{S1S2}	Source-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	±10	V
I_S	Continuous Source Current ⁽¹⁾	7	A
I_{SM}	Pulsed Source Current ⁽²⁾	37	A
P_D	Power Dissipation ⁽¹⁾	1.7	W
$V_{(ESD)}$	Human Body Model (HBM)	2.5	kV
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150	°C

- (1) Typical $R_{\theta JA} = 75^\circ\text{C/W}$ when mounted on a 1 inch², 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.
 (2) Max $R_{\theta JA} = 90^\circ\text{C/W}$, pulse duration ≤100 μs, duty cycle ≤1%



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4 Revision History

DATE	REVISION	NOTES
November 2015	*	Initial release.

5 Specifications

5.1 Electrical Characteristics

 $(T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
V_{S1S2}	Source-to-source voltage	$V_{GS} = 0\text{ V}, I_S = 250\ \mu\text{A}$	20			V
I_{S1S2}	Source-to-source leakage current	$V_{GS} = 0\text{ V}, V_{S1S2} = 16\text{ V}$			1	μA
I_{GSS}	Gate-to-source leakage current	$V_{S1S2} = 0\text{ V}, V_{GS} = 6\text{ V}$			0.5	μA
		$V_{S1S2} = 0\text{ V}, V_{GS} = 10\text{ V}$			4	μA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{S1S2} = V_{GS}, I_S = 250\ \mu\text{A}$	0.68	0.9	1.3	V
$R_{S1S2(on)}$	Source-to-source on-resistance	$V_{GS} = 2.5\text{ V}, I_S = 2\text{ A}$	20	29	36	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_S = 2\text{ A}$	14	20	24	$\text{m}\Omega$
		$V_{GS} = 6.5\text{ V}, I_S = 2\text{ A}$	13	18.7	22.5	$\text{m}\Omega$
g_{fs}	Transconductance	$V_{S1S2} = 2\text{ V}, I_S = 2\text{ A}$		19		S
DYNAMIC CHARACTERISTICS⁽¹⁾						
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{S1S2} = 10\text{ V}, f = 1\text{ MHz}$		718	933	pF
C_{oss}	Output capacitance			92	120	pF
C_{rss}	Reverse transfer capacitance			61	79	pF
Q_g	Gate charge total (4.5 V)	$V_{S1S2} = 10\text{ V}, I_S = 2\text{ A}$		6.0	7.8	nC
Q_{gd}	Gate charge gate-to-drain			1.4		nC
Q_{gs}	Gate charge gate-to-source			1.2		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.6		nC
Q_{oss}	Output charge	$V_{S1S2} = 10\text{ V}, V_{GS} = 0\text{ V}$		2.3		nC
$t_{d(on)}$	Turn-on delay time	$V_{S1S2} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_{S1S2} = 2\text{ A}, R_G = 0\ \Omega$		37		ns
t_r	Rise time			54		ns
$t_{d(off)}$	Turn-off delay time			173		ns
t_f	Fall time			99		ns

(1) Charge and timing values specified are per single FET.

5.2 Thermal Information

 $(T_A = 25^\circ\text{C}$ unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾		75		$^\circ\text{C/W}$
	Junction-to-ambient thermal resistance ⁽²⁾		175		$^\circ\text{C/W}$

(1) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

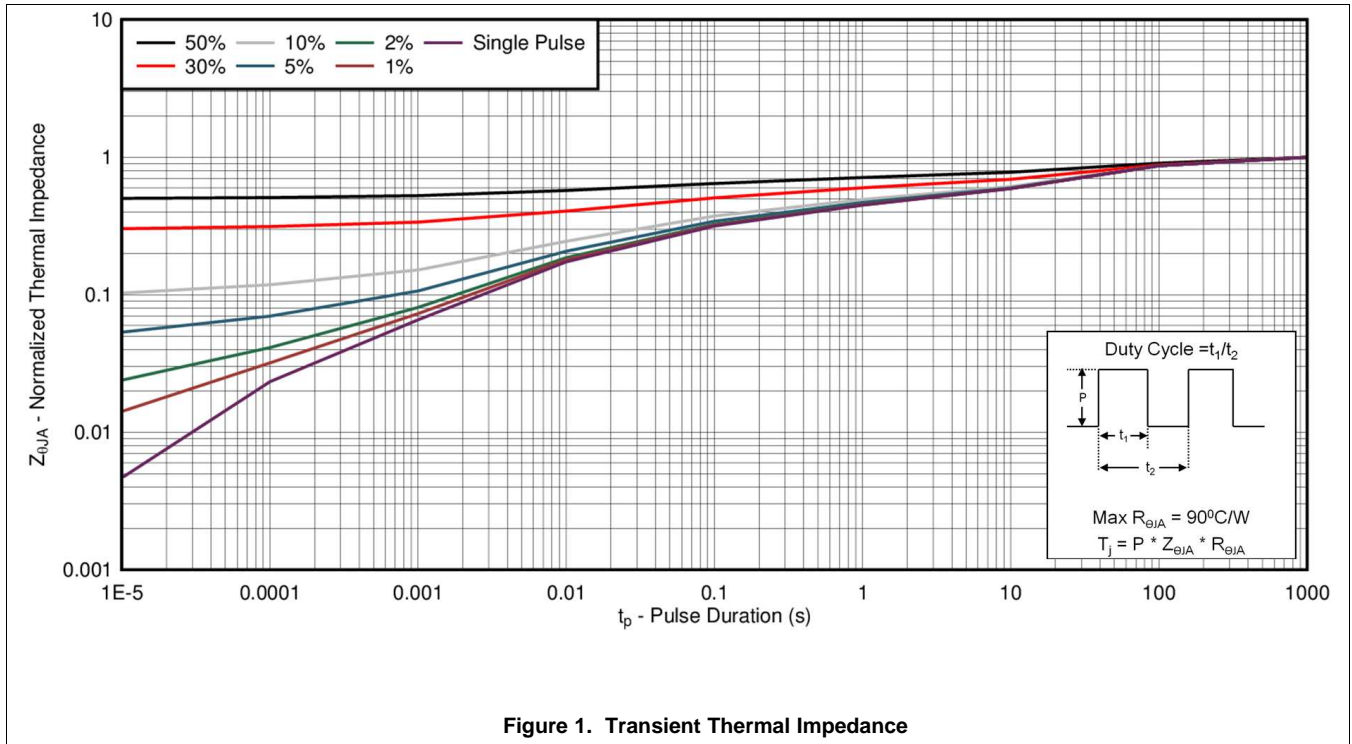


Figure 1. Transient Thermal Impedance

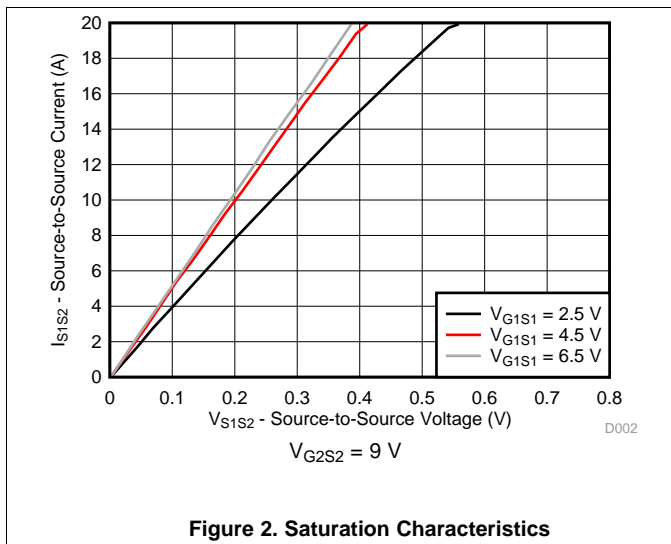


Figure 2. Saturation Characteristics

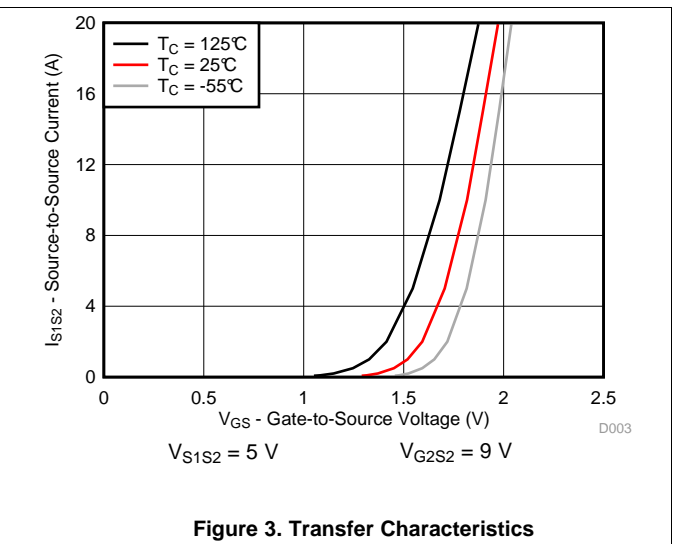


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

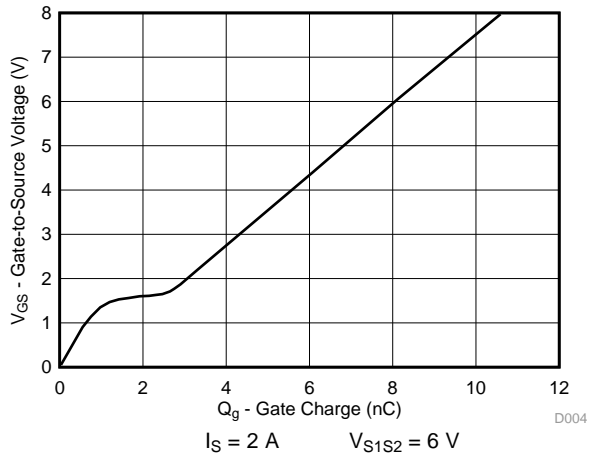


Figure 4. Gate Charge

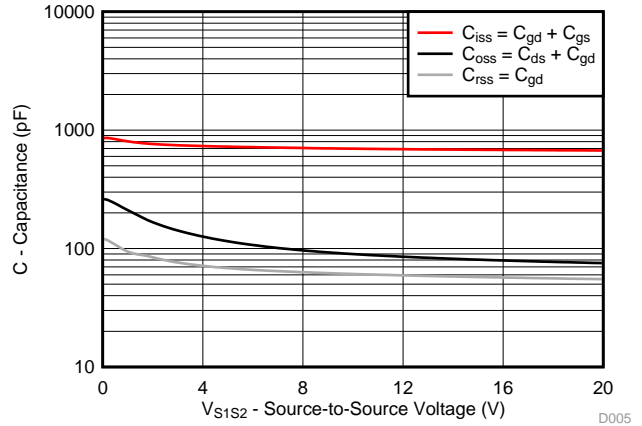


Figure 5. Capacitance

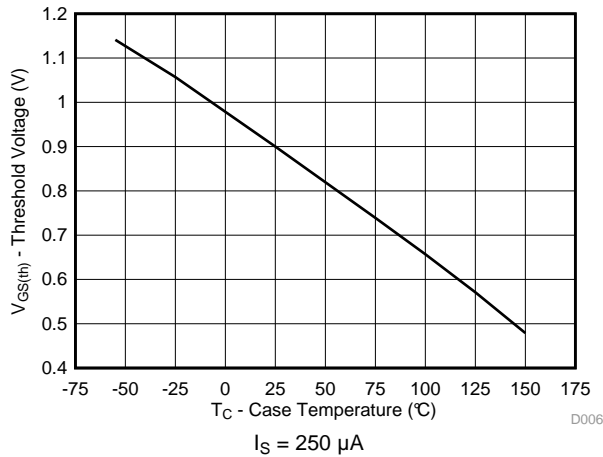


Figure 6. Threshold Voltage vs Temperature

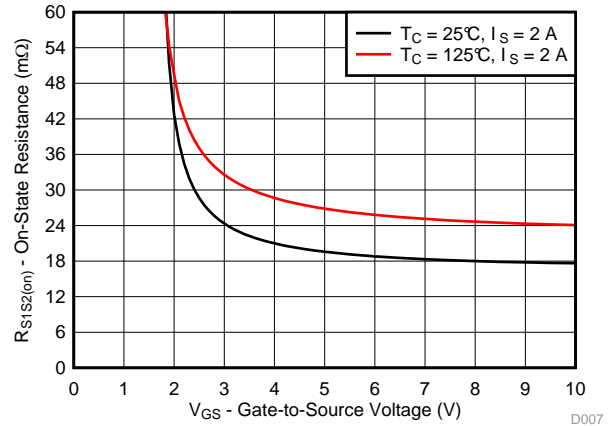


Figure 7. On-State Source-to-Source Resistance vs Gate-to-Source Voltage

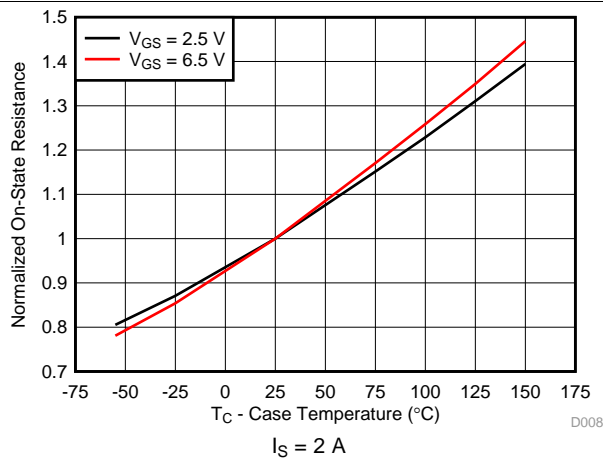


Figure 8. Normalized On-State Resistance vs Temperature

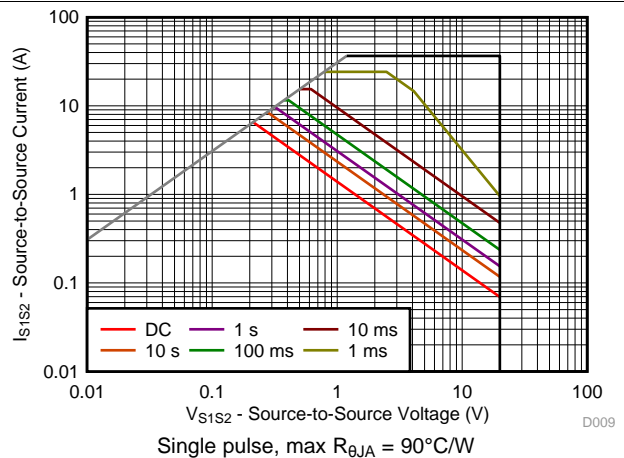


Figure 9. Maximum Safe Operating Area

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

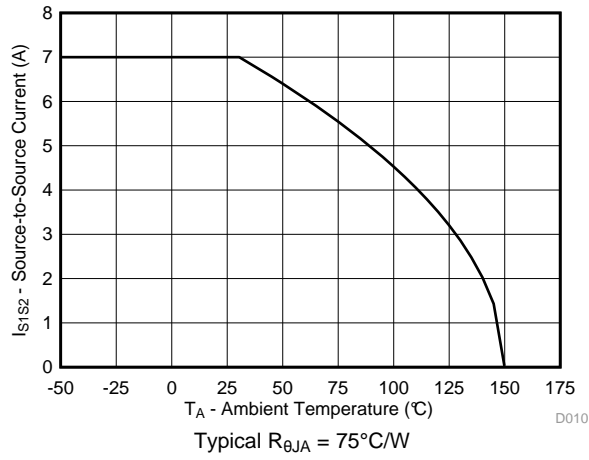


Figure 10. Maximum Source Current vs Temperature

6 Device and Documentation Support

6.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
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6.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.4 Glossary

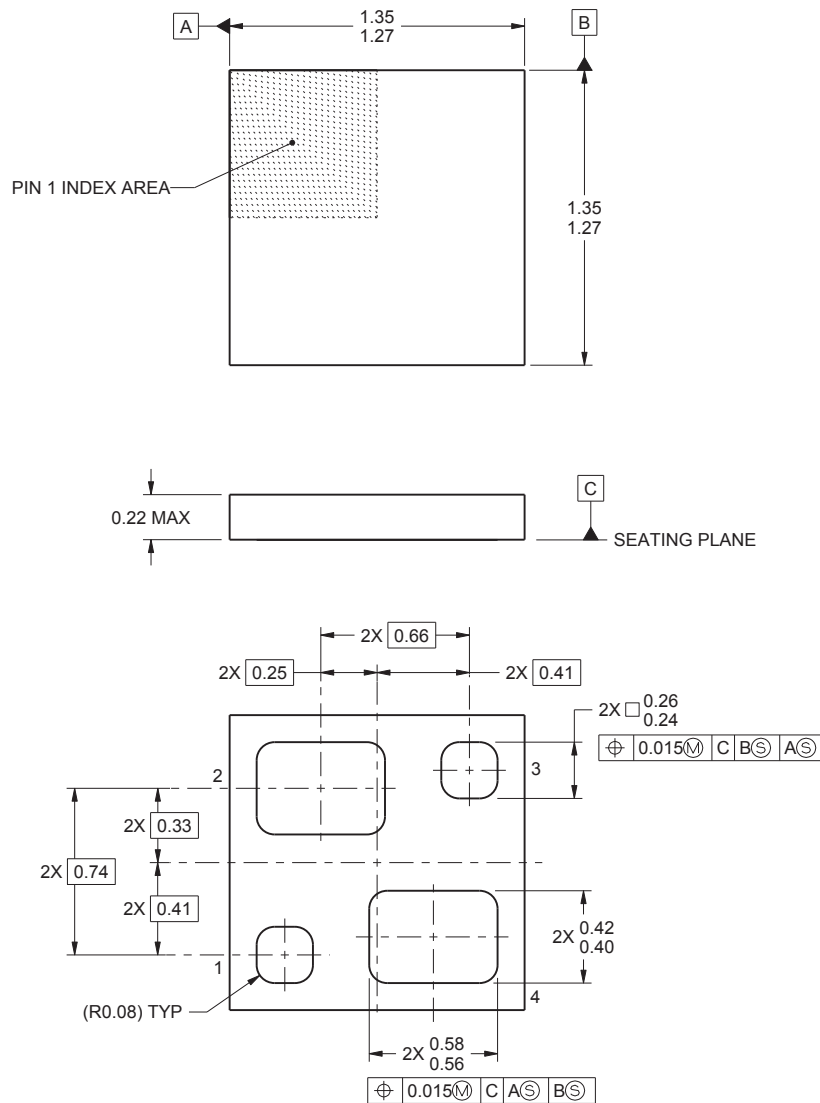
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Package Dimensions

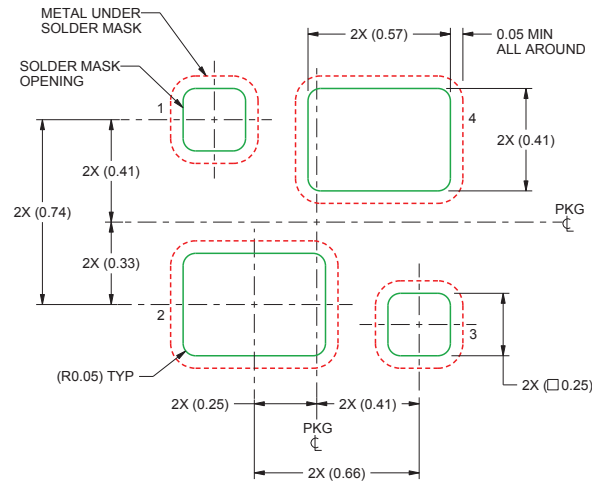


Pin Configuration

PIN NUMBER	NAME
1	G1
2	S2
3	G2
4	S1

1. All linear dimensions are in millimeters.

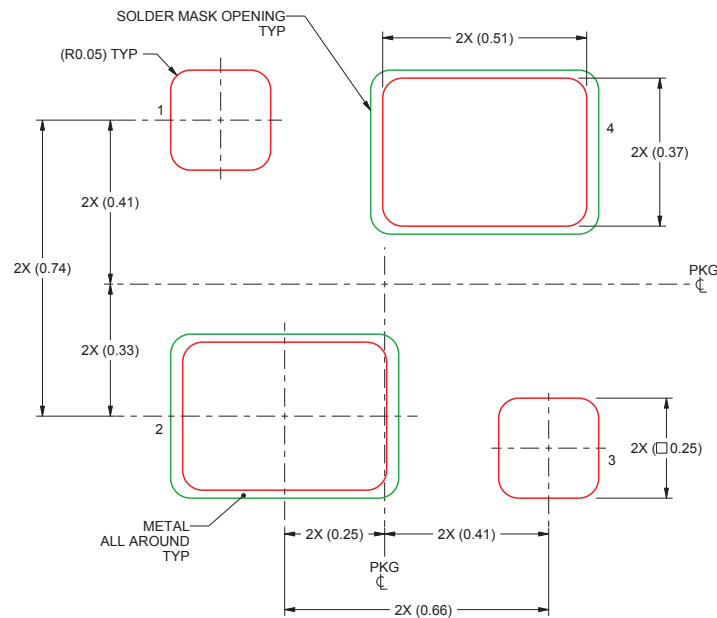
7.2 Recommended PCB Pattern



Land Pattern Example

Solder Mask Defined
Scale: 50X

7.3 Recommended Stencil Pattern

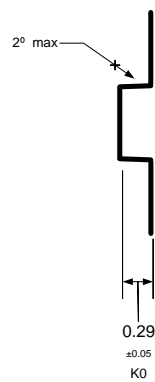
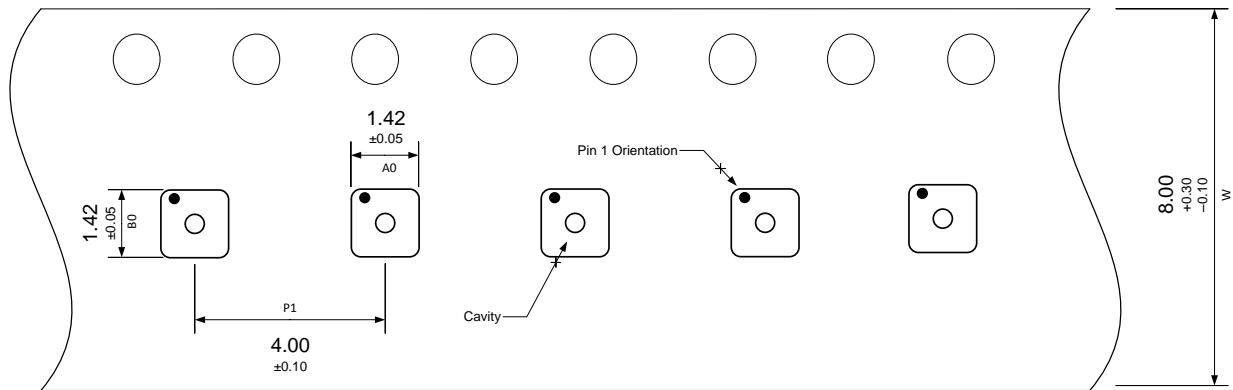


Solder Paste Example

Based on 0.1 mm thick stencil
Pads 2 and 4: 81% printed on solder coverage by area
Scale: 80X

1. All linear dimensions are in millimeters.
2. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7.4 Q3A Tape and Reel Information



All Measurements in
Millimeters (mm)

- Notes:
1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
 2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
 3. Material: black static-dissipative polystyrene
 4. MSL1 260°C (IR and convection) PbF-reflow compatible

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD85302L	ACTIVE	PICOSTAR	YME	4	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	85302	Samples
CSD85302LT	ACTIVE	PICOSTAR	YME	4	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	85302	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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