

## CSD25481F4 20 V P-Channel FemtoFET™ MOSFET

### 1 Features

- Ultra-Low On Resistance
- Ultra-Low  $Q_g$  and  $Q_{gd}$
- High Operating Drain Current
- Ultra-Small Footprint (0402 Case Size)
  - 1 mm × 0.6 mm
- Ultra-Low Profile
  - 0.35 mm Max Height
- Integrated ESD Protection Diode
  - Rated >4 kV HBM
  - Rated >2 kV CDM
- Lead and Halogen Free
- RoHS Compliant

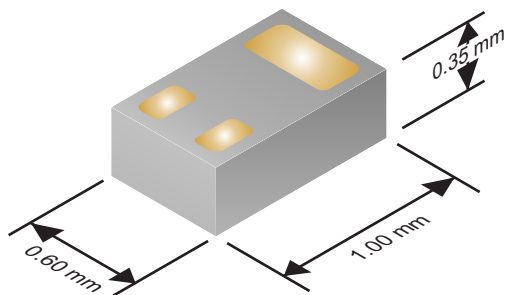
### 2 Applications

- Optimized for Load Switch Applications
- Optimized for General Purpose Switching Applications
- Battery Applications
- Handheld and Mobile Applications

### 3 Description

This 90 mΩ, 20 V P-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

Typical Part Dimensions



### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	-20		V
$Q_g$	Gate Charge Total (-4.5 V)	913		pC
$Q_{gd}$	Gate Charge Gate-to-Drain	153		pC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = -1.8\text{ V}$	395	mΩ
		$V_{GS} = -2.5\text{ V}$	145	mΩ
		$V_{GS} = -4.5\text{ V}$	90	mΩ
$V_{GS(th)}$	Threshold Voltage	-0.95		V

### Ordering Information<sup>(1)</sup>

Device	Qty	Media	Package	Ship
CSD25481F4	3000	7-Inch Reel	Femto(0402) 1.0 mm × 0.6 mm	Tape and Reel
CSD25481F4T	250	7-Inch Reel	Land Grid Array (LGA)	

(1) For all available packages, see the orderable addendum at the end of the data sheet.

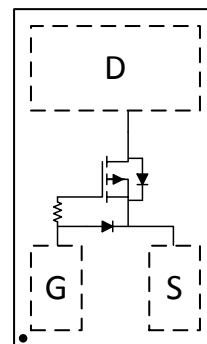
### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	-20	V
$V_{GS}$	Gate-to-Source Voltage	-12	V
$I_D$	Continuous Drain Current <sup>(1)</sup>	-2.5	A
$I_{DM}$	Pulsed Drain Current <sup>(2)</sup>	-10	A
$I_G$	Continuous Gate Clamp Current	-35	mA
	Pulsed Gate Clamp Current <sup>(2)</sup>	-350	
$P_D$	Power Dissipation <sup>(1)</sup>	500	mW
$V_{(ESD)}$	Human Body Model (HBM)	4	kV
	Charged Device Model (CDM)	2	kV
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	-55 to 150	°C

(1) Typical  $R_{\theta JA} = 85^\circ\text{C/W}$  on 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu pad on a 0.06 inch (1.52 mm) thick FR4 PCB.

(2) Pulse duration  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$

Top View



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision C (February 2014) to Revision D Page

- Corrected timing  $V_{DS}$  to read –10 V ..... 3

### Changes from Revision B (February 2013) to Revision C Page

- Corrected capacitance units to read pF in [Figure 5](#) ..... 5

### Changes from Revision A (December 2013) to Revision B Page

- Updated lead and halogen free in features ..... 1
- Added  $I_G$  parameter ..... 1
- Lowered  $I_{DSS}$  limit ..... 3
- Lowered  $I_{GSS}$  limit ..... 3

### Changes from Original (September 2013) to Revision A Page

- Took out jumbo reel info and added small reel info ..... 1
- Removed UIS graph ..... 5
- Corrected device name ..... 10

## 5 Specifications

### 5.1 Electrical Characteristics

(T<sub>A</sub> = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
B <sub>V</sub> DSS	Drain-to-Source Voltage	V <sub>GS</sub> = 0 V, I <sub>DS</sub> = -250 μA	-20			V
I <sub>DSS</sub>	Drain-to-Source Leakage Current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -16 V			-100	nA
I <sub>GSS</sub>	Gate-to-Source Leakage Current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = -12 V			-50	nA
V <sub>GS(th)</sub>	Gate-to-Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>DS</sub> = -250 μA	-0.7	-0.95	-1.2	V
R <sub>DS(on)</sub>	Drain-to-Source On-Resistance	V <sub>GS</sub> = -1.8 V, I <sub>DS</sub> = -0.1 A		395	800	mΩ
		V <sub>GS</sub> = -2.5 V, I <sub>DS</sub> = -0.5 A		145	174	mΩ
		V <sub>GS</sub> = -4.5 V, I <sub>DS</sub> = -0.5 A		90	105	mΩ
		V <sub>GS</sub> = -8 V, I <sub>DS</sub> = -0.5 A		75	88	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = -10 V, I <sub>DS</sub> = -0.5 A		3.3		S
<b>DYNAMIC CHARACTERISTICS</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = -10 V, f = 1 MHz		189		pF
C <sub>oss</sub>	Output Capacitance			78		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			5.5		pF
R <sub>G</sub>	Series Gate Resistance			20		Ω
Q <sub>g</sub>	Gate Charge Total (4.5 V)	V <sub>DS</sub> = -10 V, I <sub>DS</sub> = -0.5 A		913		pC
Q <sub>gd</sub>	Gate Charge Gate-to-Drain			153		pC
Q <sub>gs</sub>	Gate Charge Gate-to-Source			240		pC
Q <sub>g(th)</sub>	Gate Charge at V <sub>th</sub>			116		pC
Q <sub>oss</sub>	Output Charge		V <sub>DS</sub> = -10 V, V <sub>GS</sub> = 0 V		1030	
t <sub>d(on)</sub>	Turn On Delay Time	V <sub>DS</sub> = -10 V, V <sub>GS</sub> = -4.5 V, I <sub>DS</sub> = -0.5 A, R <sub>G</sub> = 2 Ω		4.1		ns
t <sub>r</sub>	Rise Time			3.6		ns
t <sub>d(off)</sub>	Turn Off Delay Time			16.9		ns
t <sub>f</sub>	Fall Time			6.7		ns
<b>DIODE CHARACTERISTICS</b>						
V <sub>SD</sub>	Diode Forward Voltage	I <sub>SD</sub> = -0.5 A, V <sub>GS</sub> = 0 V		-0.75		V
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DS</sub> = -10 V, I <sub>F</sub> = -0.5 A, di/dt = 100 A/μs		1010		pC
t <sub>rr</sub>	Reverse Recovery Time			7.5		ns

### 5.2 Thermal Information

(T<sub>A</sub> = 25°C unless otherwise stated)

THERMAL METRIC		TYPICAL VALUES	UNIT
R <sub>θJA</sub>	Junction-to-Ambient Thermal Resistance <sup>(1)</sup>	85	°C/W
	Junction-to-Ambient Thermal Resistance <sup>(2)</sup>	245	

(1) Device mounted on FR4 material with 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

### 5.3 Typical MOSFET Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

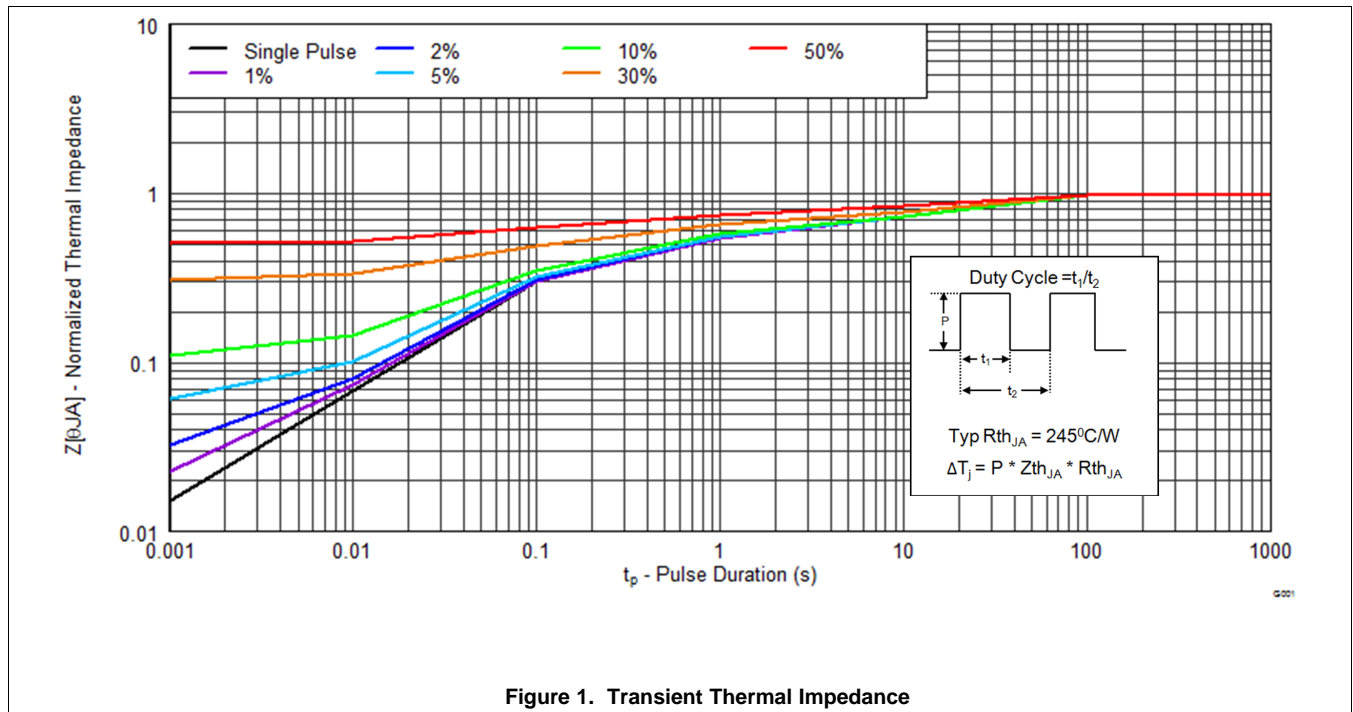


Figure 1. Transient Thermal Impedance

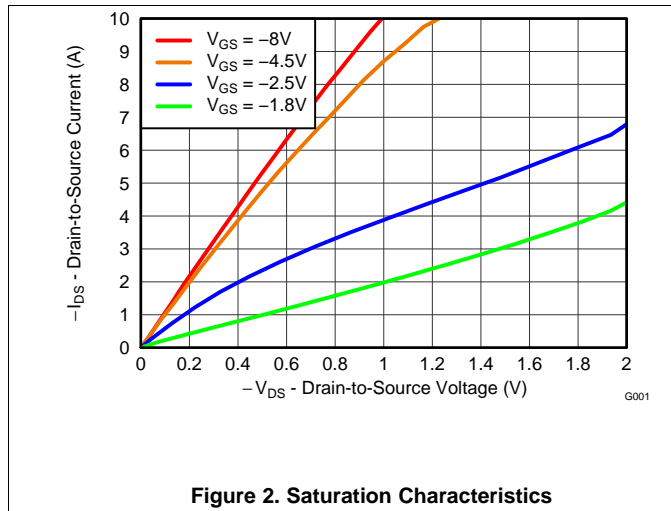


Figure 2. Saturation Characteristics

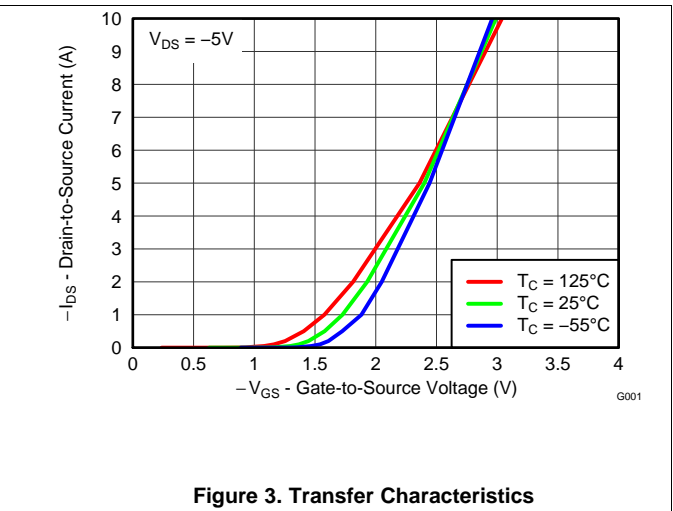
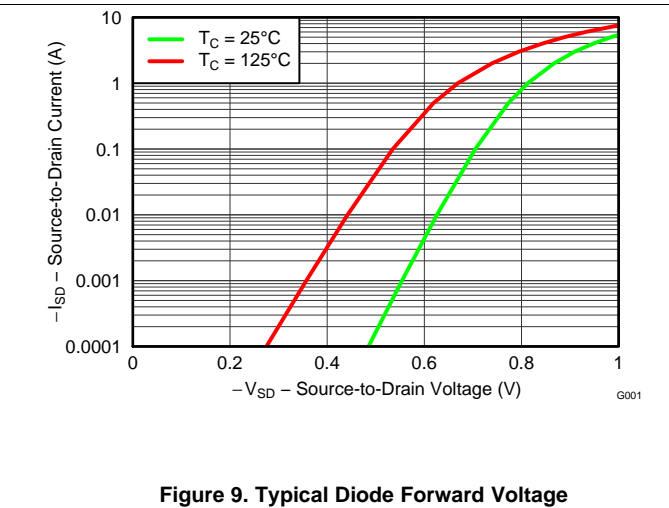
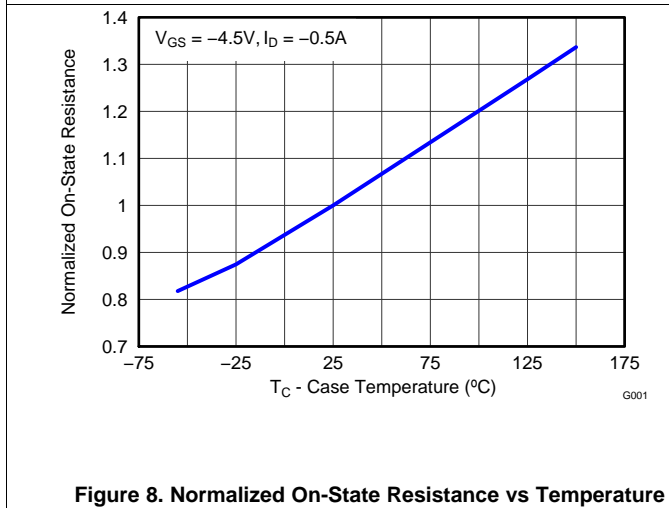
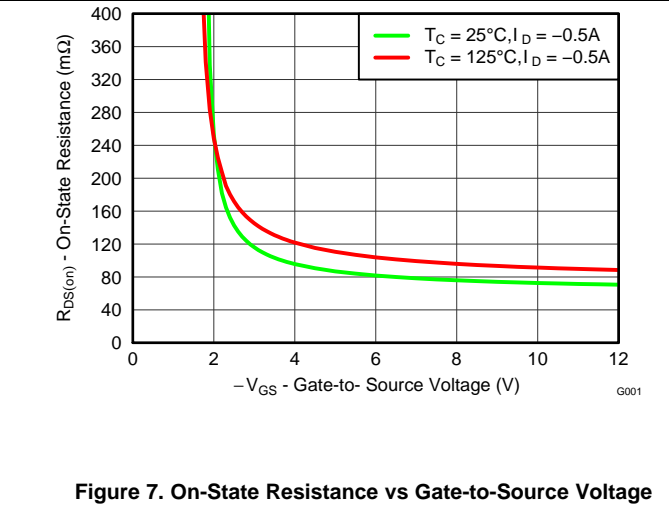
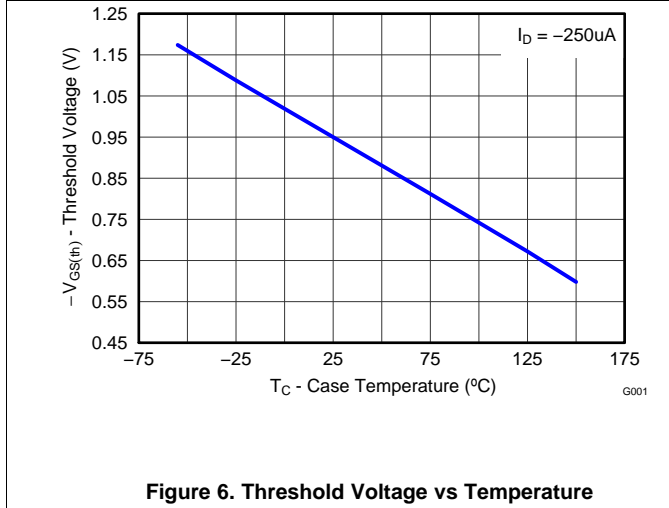
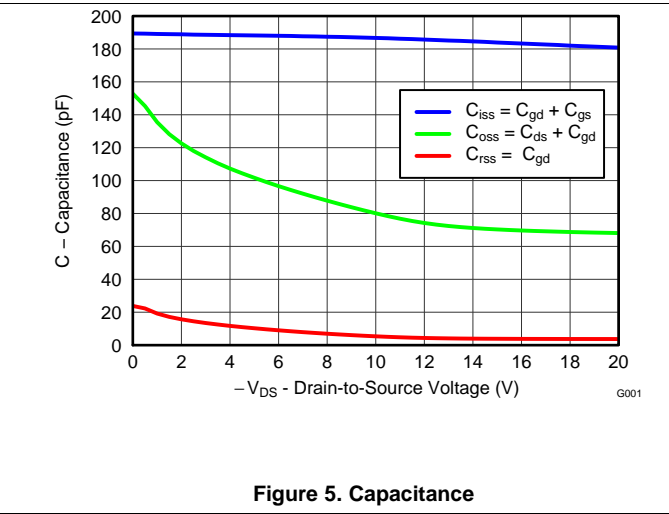
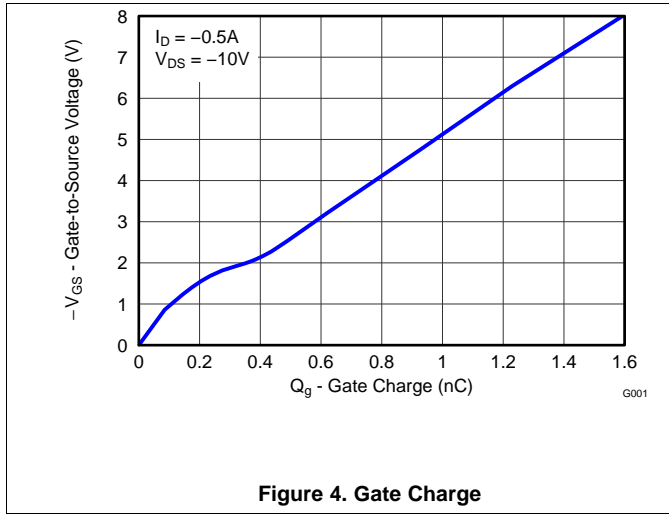


Figure 3. Transfer Characteristics

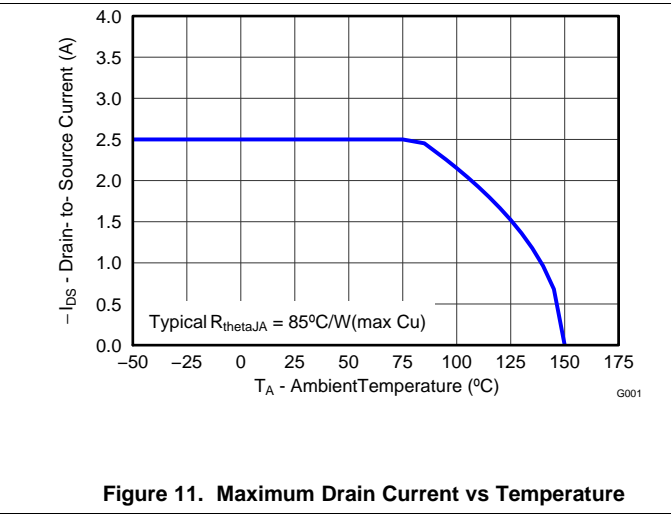
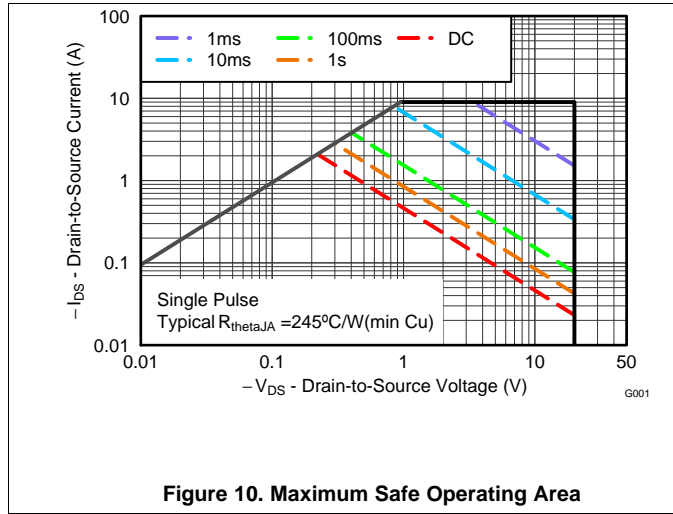
Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)



**Typical MOSFET Characteristics (continued)**

( $T_A = 25^\circ\text{C}$  unless otherwise stated)



## 6 Device and Documentation Support

### 6.1 Trademarks

FemtoFET is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.3 Glossary

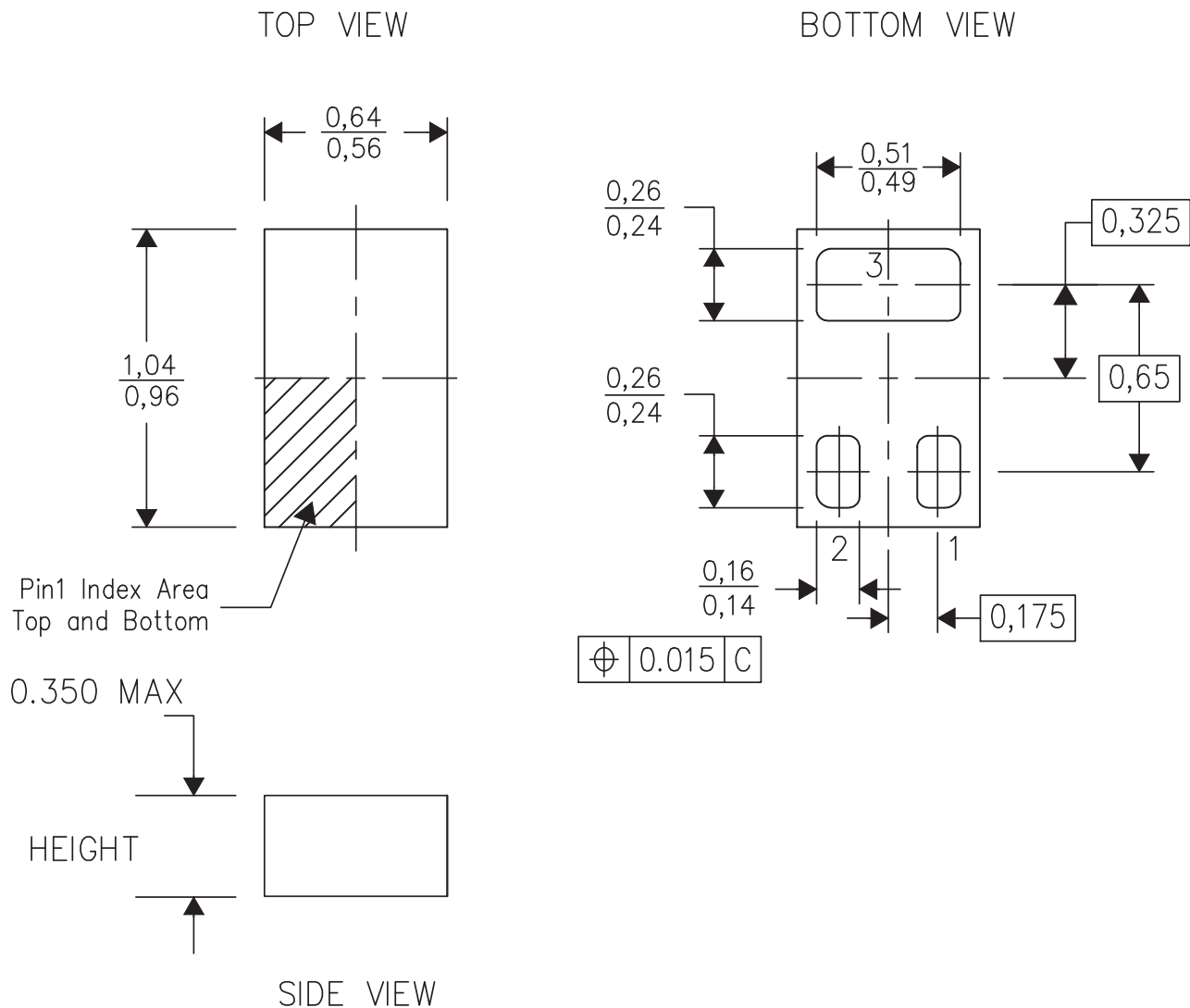
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical Data

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

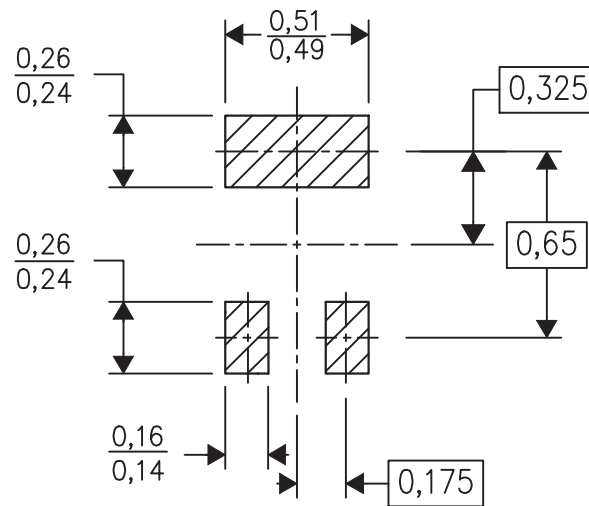
### 7.1 Mechanical Dimensions



- (1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- (2) This drawing is subject to change without notice.
- (3) This package is a PB-free solder land design.

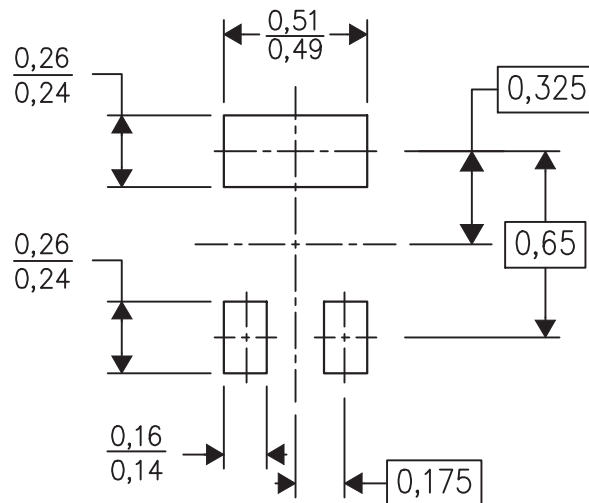


## 7.2 Recommended Minimum PCB Layout



(1) All dimensions are in millimeters.

## 7.3 Recommended Stencil Pattern



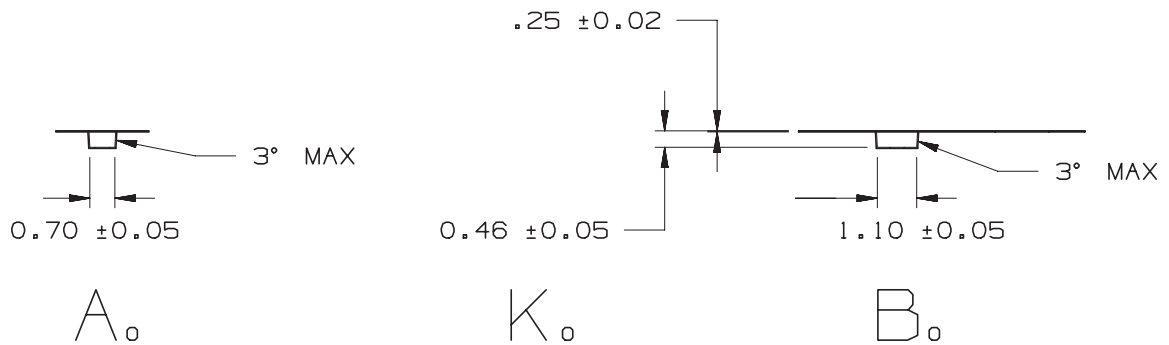
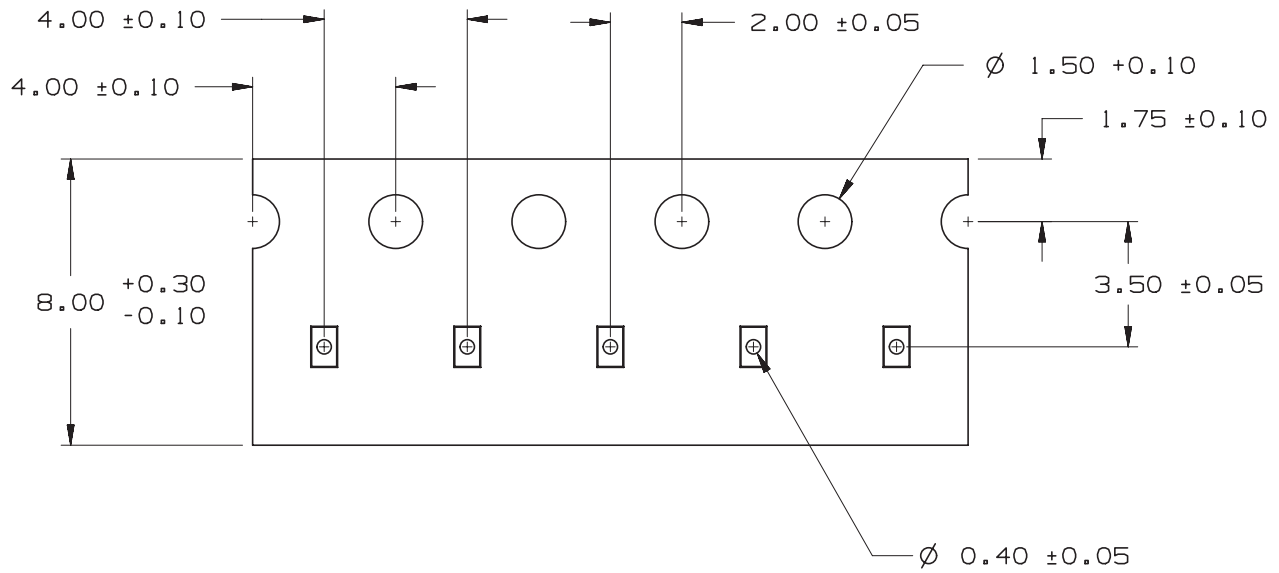
(1) All dimensions are in millimeters.

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**7.4 CSD25481F4 Embossed Carrier Tape Dimensions**



- (1) Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25481F4	ACTIVE	PICOSTAR	YJC	3	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	CS	<a href="#">Samples</a>
CSD25481F4T	ACTIVE	PICOSTAR	YJC	3	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	CS	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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