# ADS7142 Nanopower, Dual-Channel, Programmable Sensor Monitor

## 1 Features

- Standalone, Nanopower Sensor Monitor for cost-sensitive designs
- Small Package Size: 1.5 x 2 mm
- Efficient Host Sleep and Wake-up
  - Autonomous Monitoring at 900 nW
  - Windowed Comparator for Event-triggered Host Wake-up
  - Data Buffering during Host Sleep
- Independent Sensor Configuration and Calibration
  - Dual-Channel, Pseudo-Differential, or Ground-Sense Input Configuration
  - Programmable Thresholds for Calibration
  - Internal Calibration improves Offset and Drift
- False Trigger Prevention
  - Programmable Thresholds per Channel
  - Programmable Hysteresis for Noise Immunity
  - Event Counter for Transient Rejection
- Deep Data Analysis
  - Data Buffer for Fault Diagnostics
  - High Precision Mode for 16-bit Accuracy
  - One-Shot Mode for Fast Data Capture
- $I^2C$™ Interface
  - Compatible from 1.65 V to 3.6 V
  - 8 Configurable Addresses
  - Up to 3.4 MHz (High Speed)
- Wide Operating Range
  - Analog Supply: 1.65 V to 3.6 V
  - Temperature Range: –40°C to 125°C

## 2 Applications

- Sensor Nodes for Internet of Things (IoT)
- Gas, Heat, PIR Motion and Smoke Detectors
- Preventive Maintenance for Elevators, Escalators, HVAC, Industrial Equipment, etc.
- Wearable Electronics
- Zero Cross Detection for Fault Indicators
- Supervisory Functions
- Comparator with Programmable Reference
- Sensors for Deep Learning Artificial Intelligence

## 3 Description

The ADS7142 autonomously monitors signals while maximizing system power, reliability, and performance. It implements event-triggered interrupts per channel using a digital windowed comparator with programmable high and low thresholds, hysteresis, and event counter. The device includes a dual-channel analog multiplexer in front of a successive approximation register analog-to-digital converter (SAR ADC) followed by an internal data buffer for converting and capturing data from sensors.

The ADS7142 is available in 10-pin QFN package and consumes only 900 nW of power. The small form-factor and low power consumption make this device suitable for space-constrained and/or battery-powered applications.

**Device Information**(1)

| PART NAME | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| ADS7142 | X2QFN (10) | 1.50 mm × 2.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

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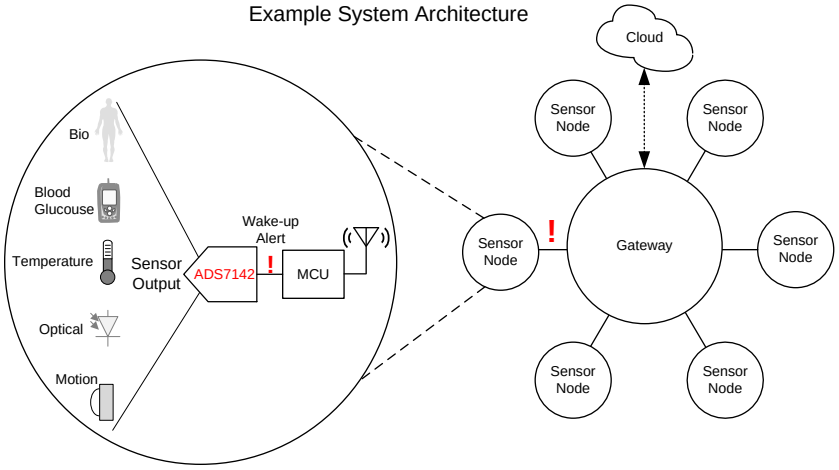
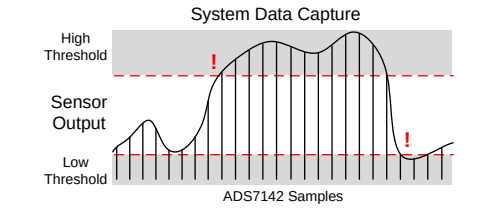
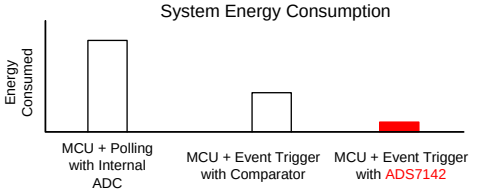
Example System Architecture



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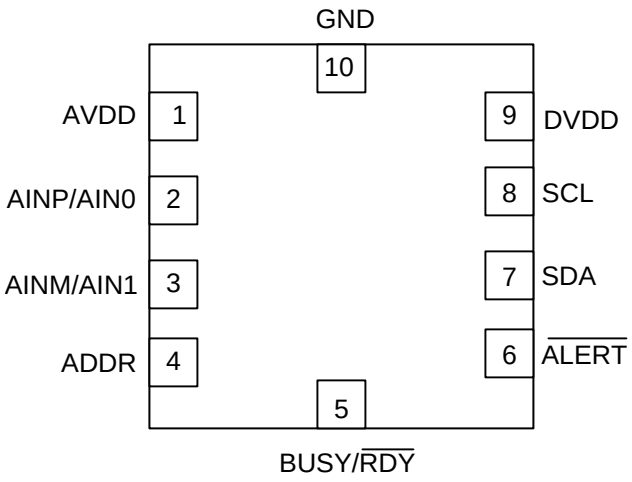
## 4 Revision History

| DATE | REVISION | NOTES |
|---|---|---|
| September 2017 | * | Initial release. |

# 5 Pin Configuration and Functions

**RUG PACKAGE**
**10-Pin X2QFN**
**TOP VIEW**




**Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AVDD | 1 | Supply | Analog supply input, also used as the reference voltage for analog to digital conversion. |
| AINP/AIN0 | 2 | Analog input | Single-Channel operation: Positive analog signal input<br>Two-Channel operation: Analog signal input, Channel 0 |
| AINM/AIN1 | 3 | Analog input | Single-Channel operation: Negative analog signal input<br>Two-Channel operation: Analog signal input, Channel 1 |
| ADDR | 4 | Analog Input | Input for selecting $I^2C$ address of the device<br>Refer Table 2 for details |
| BUSY/$\overline{\text{RDY}}$ | 5 | Digital output | The device pulls this pin high when it is scanning through channels in a sequence and brings this pin low when sequence is completed or aborted. |
| $\overline{\text{ALERT}}$ | 6 | Digital output | Active low, open drain output. Status of this pin is controlled by Digital window comparator block. Connect a pull-up resistor from DVDD to this pin |
| SDA | 7 | Digital input/output | Serial data in/out for $I^2C$ interface. Connect a pull-up resistor from DVDD to this pin |
| SCL | 8 | Digital input | Serial clock for $I^2C$ interface. Connect a pull-up resistor from DVDD to this pin |
| DVDD | 9 | Supply | Digital I/O supply voltage |
| GND | 10 | Supply | Ground for power supply, all analog and digital signals are referred to this pin |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings[1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | ADDR to GND | -0.3 | AVDD + 0.3 | V |
| | AVDD to GND | –0.3 | 3.9 | V |
| | DVDD to GND | –0.3 | 3.9 | V |
| | AINP/AIN0 to GND | –0.3 | AVDD + 0.3 | V |
| | AINM/AIN1 to GND | –0.3 | AVDD + 0.3 | V |
| Digital input voltage to GND | | –0.3 | DVDD + 0.3 | V |
| Storage temperature, $T_{stg}$ | | –60 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| AVDD | Analog supply voltage range | 1.65 | 3.6 | V |
| DVDD | Digital supply voltage range | 1.65 | 3.6 | V |
| $T_A$ | Operating free-air temperature | –40 | 125 | °C |

## 6.3 Thermal Information

| THERMAL METRIC[1] | | ADS7142 | UNIT |
|---|---|---|---|
| | | RUG (X2QFN) | |
| | | 10 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 120.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 42.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 51.1 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 51.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the*Semiconductor and IC Package Thermal Metrics* application report.

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## 6.4 Electrical Characteristics - All Modes

At $T_A$ = –40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG INPUT - Two-Channel Single-Ended Configuration** | | | | | | |
| | Full-scale input voltage span(1) | AINP/AIN0 to GND or AINM/AIN1 to GND | 0 | | AVDD | V |
| | Absolute Input voltage range | AINP/AIN0 to GND or AINM/AIN1 to GND | –0.1 | | AVDD + 0.1 | V |
| **ANALOG INPUT - Single-Channel Single-Ended Configuration (with Remote Ground Sense)** | | | | | | |
| | Full-scale input voltage span(1) | AINP/AIN0 to AINM/AIN1 | 0 | | AVDD | V |
| | Absolute Input voltage range | AINP/AIN0 to GND | –0.1 | | AVDD + 0.1 | V |
| | | AINM/AIN1 to GND | –0.1 | | 0.1 | |
| **ANALOG INPUT - Single-Channel Pseudo-Differential Configuration** | | | | | | |
| | Full-scale input voltage span(1) | AINP/AIN0 to AINM/AIN1 | –AVDD/2 | | AVDD/2 | V |
| | Absolute Input voltage range | AINP/AIN0 to GND | –0.1 | | AVDD + 0.1 | V |
| | | AINM/AIN1 to GND | (AVDD/2 - 0.1) | | (AVDD/2 + 0.1) | |
| **Internal Oscillator** | | | | | | |
| $t_{HSO}$ | Time period for High Speed Oscillator | | | 47.6 | | ns |
| $t_{LPO}$ | Time period for Low Power Oscillator | | | 95.2 | | us |
| **DIGITAL INPUT/OUTPUT (SCL, SDA)** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.7 x DVDD | | DVDD | V |
| $V_{IL}$ | Low-level input voltage | | 0 | | 0.3 x DVDD | V |
| $V_{OL}$ | Low-level output voltage | At $I_{sink}$ = 3 mA, 1.65 < DVDD < 2 V | 0 | | 0.2 x DVDD | V |
| | | At $I_{sink}$ = 3 mA, DVDD > 2 V | 0 | | 0.4 | |
| **POWER-SUPPLY REQUIREMENTS** | | | | | | |
| AVDD | Analog supply voltage | | 1.65 | 3 | 3.6 | V |
| DVDD | Digital I/O supply voltage | | 1.65 | 3 | 3.6 | V |

(1) Ideal input span; does not include gain or offset error.

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## 6.5 Electrical Characteristics - I²C Command Mode

At $T_A$ = –40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, unless otherwise noted.

| PARAMETER0 | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Sampling Dynamics** | | | | | | |
| $f_{SCL}$ | $I^2C$ clock frequency | | 0 | | 3.4 | MHz |
| $f_S$ | Sampling Rate (1) | SCL = 3.4 MHz | | | 140 | Ksps |
| **DC Specifications** | | | | | | |
| | Resolution | | | 12 | | Bits |
| NMC | No missing codes | | 12 | | | Bits |
| INL | Integral nonlinearity | | | ±0.5 | | LSB (2) |
| DNL | Differential nonlinearity | | | ±0.3 | | LSB |
| $E_O$ | Offset error | Post OFFSET_CAL | | ±0.75 | | LSB |
| $dV_{OS}/dT$ | Offset error drift with temperature | With OFFSET_CAL | | ±5 | | ppm/°C |
| $E_G$ | Gain error | | | ±0.03 | | %FS |
| | Gain error drift with temperature | | | 5 | | ppm/°C |
| **AC Specifications** | | | | | | |
| SNR | Signal-to-noise ratio (3) | $f_{IN}$ = 2 kHz, AVDD = 3 V, $f_{sample}$ = 140 kSPS | | 70 | | dB |
| THD | Total harmonic distortion (3) (4) | $f_{IN}$ = 2 kHz, AVDD = 3 V, $f_{sample}$ = 140 kSPS | | –83.5 | | dB |
| SINAD | Signal-to-noise and distortion (3) | $f_{IN}$ = 2 kHz, AVDD = 3 V, $f_{sample}$ = 140 kSPS | | 69.5 | | dB |
| SFDR | Spurious-free dynamic range (3) | $f_{IN}$ = 2 kHz, AVDD = 3 V, $f_{sample}$ = 140 kSPS | | 88 | | dB |
| $BW_{(fp)}$ | Full-power bandwidth | At –3 dB, AVDD = 3 V | | 25 | | MHz |
| **Power Consumption** | | | | | | |
| $I_{AVDD}$ | Analog supply current | SCL = 3.4 MHz | | 235 | | µA |
| | | SCL = 1.7 MHz | | 120 | | |
| | | SCL = 1 MHz | | 70 | | |
| | | SCL = 400 kHz | | 28 | | |
| | | SCL = 100 kHz, AVDD = 1.8 V | | 3.5 | | |
| | Static Analog Supply Current | No activity on SCL and SDA | | 0.015 | | |
| $I_{DVDD}$ | Digital Supply Current | SCL = 3.4 MHz | | 25 | | µA |
| | | SCL = 100 kHz, AVDD = 1.8 V | | 0.5 | | |
| | Static Digital Supply Current | No activity on SCL and SDA | | 0.01 | | |

(1) Refer to Electrical Characteristics - $I^2C$ Command Mode for details.
(2) LSB means least significant bit.
(3) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified..
(4) Calculated on the first nine harmonics of the input frequency.

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## 6.6 Electrical Characteristics - Autonomous Monitoring Modes

At $T_A$ = –40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Sampling Dynamics** | | | | | | |
| $t_{conv}$ | Conversion Time | High Speed Oscillator | | 14 x $t_{HSO}$ | | |
| | | Low Power Oscillator | | 14 x $t_{LPO}$ | | |
| $t_{acq}$ | Acquisition Time | High Speed Oscillator | 7 x $t_{HSO}$ | | | |
| | | Low Power Oscillator | 4 x $t_{LPO}$ | | | |
| $t_{cycle}$ | Cycle Time | High Speed Oscillator | | nCLK x $t_{HSO}$ | | |
| | | Low Power Oscillator | | nCLK x $t_{LPO}$ | | |
| **DC Specifications** | | | | | | |
| | Resolution | | | 12 | | Bits |
| $E_O$ | Offset error | Post OFFSET_CAL | | ±0.75 | | LSB |
| $E_G$ | Gain error | | | ±0.03 | | %FS |
| **Power Consumption** | | | | | | |
| $I_{AVDD}$ | Analog supply current | With Low Power Oscillator, nCLK = 250, AVDD = 1.8 V | | 0.3 | | µA |
| | | With Low Power Oscillator, nCLK = 18, AVDD = 1.8 V | | 0.5 | | |
| | | With Low Power Oscillator, nCLK = 18 | | 0.8 | | |
| | | With High Frequency Oscillator, nCLK = 250 | | 585 | | |
| | | With High Frequency Oscillator, nCLK = 100 | | 640 | | |
| | | With High Frequency Oscillator, nCLK = 21 | | 975 | | |
| | Static Analog supply current | No activity on SCL and SDA, BUSY/$\overline{RDY}$ Pin Low | | 0.015 | | |
| $I_{DVDD}$ | Digital supply current | No activity on SCL and SDA | | 0.05 | | µA |

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## 6.7 Electrical Characteristics - High Precision Mode

At $T_A$ = –40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Sampling Dynamics** | | | | | | |
| $t_{conv}$ | Conversion Time | High Speed Oscillator | | 14 x $t_{HSO}$ | | |
| | | Low Power Oscillator | | 14 x $t_{LPO}$ | | |
| $t_{acq}$ | Acquisition Time | High Speed Oscillator | 7 x $t_{HSO}$ | | | |
| | | Low Power Oscillator | 4 x $t_{LPO}$ | | | |
| $t_{cycle}$ | Cycle Time | High Speed Oscillator | | nCLK x $t_{HSO}$ | | |
| | | Low Power Oscillator | | nCLK x $t_{LPO}$ | | |
| **DC Specifications** | | | | | | |
| | Resolution | | | 16 | | Bits |
| ENOB | Effective number of bits | For DC Input | | 14.4 | | |
| $E_O$ | Offset error | Post OFFSET_CAL | | ±18 | | LSB(1) |
| $E_G$ | Gain error | | | ±0.03 | | %FS |
| **Power Consumption** | | | | | | |
| $I_{AVDD}$ | Analog supply current | With Low Power Oscillator, nCLK = 18 | | 4.5 | | µA |
| | | With Low Power Oscillator, nCLK = 18, AVDD = 1.8 V | | 1.5 | | |
| | | With High Speed Oscillator, nCLK = 21 | | 115 | | |
| | | No activity on SCL and SDA, BUSY/$\overline{RDY}$ Pin Low | | 0.015 | | |
| $I_{DVDD}$ | Digital supply current | With Low Power Oscillator | | 0.3 | | µA |
| | | With High Speed Oscillator | | 10 | | |

(1) Refer to LSB equation in Accumulator Section.

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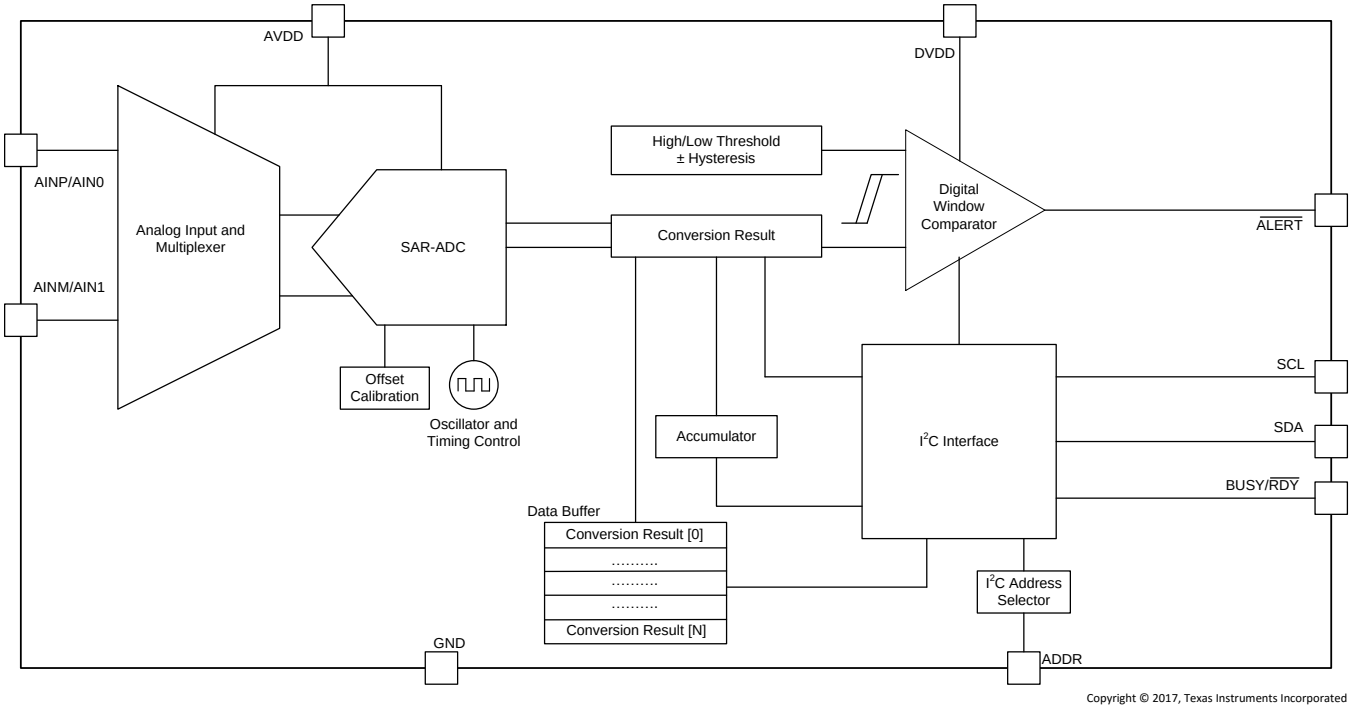
# 7 Detailed Description

## 7.1 Overview

The ADS7142 is an ultra low-power, ultra-small sensor monitor with an integrated analog-to-digital converter (ADC), input multiplexer, digital comparator, data buffer, accumulator and internal oscillator. The input multiplexer can be either configured as two single-ended channels,one single-ended channel with remote ground sensing or one pseudo-differential channel. The device includes a digital comparator with a dedicated output pin, which can be used to alert the host when a programmed high or low threshold is crossed. The device uses internal oscillators(High Speed oscillator or Low Power oscillator) for conversion. The start of conversion is controlled by the host in $I^2C$ Command mode and by the device in Autonomous Mode.

The device also features a data buffer and an accumulator. The data buffer can store the conversion results of the ADC in Autonomous Mode and the accumulator can accumulate up to 16 conversion results of ADC in High Precision Mode.

## 7.2 Functional Block Diagram

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## 7.3 Feature Description

### 7.3.1 Analog Input and Multiplexer

Figure 1 shows a small-signal equivalent circuit for the analog input pins. The device includes a two-channel analog multiplexer with each input pin having ESD protection diodes to AVDD and GND. The sampling switches are represented by ideal switches $SW_1$ and $SW_2$ in series with resistors $R_{s1}$ and $R_{s2}$ (typically 150 Ω). The sampling capacitors, $C_{s1}$ and $C_{s2}$, are typically 15 pF. The multiplexer configuration is set by the *CHANNEL_INPUT_CFG* register.

During acquisition, switches $SW_1$ and $SW_2$ are closed to allow the input signal to charge the internal sampling capacitors.

During conversion, switches $SW_1$ and $SW_2$ are opened to disconnect the input signal from the sampling capacitors.

Figure 2, Figure 3 and Figure 4 provide a simplified circuit for analog input without the ESD Diodes.

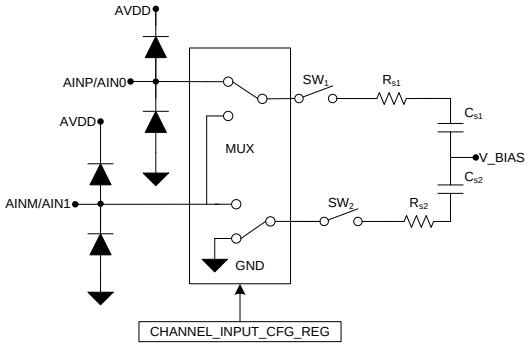


**Figure 1. Equivalent Circuit for Analog Input**

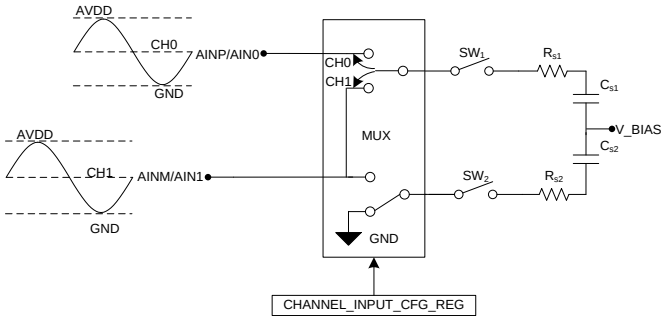


**Figure 2. Two-Channel, Single-Ended Configuration**

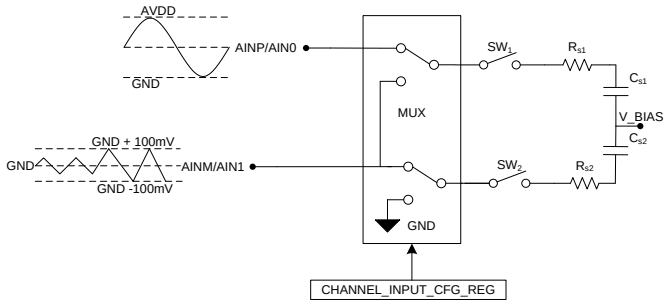


**Figure 3. Single-Channel, Single-Ended Configuration with Remote Ground Sensing**

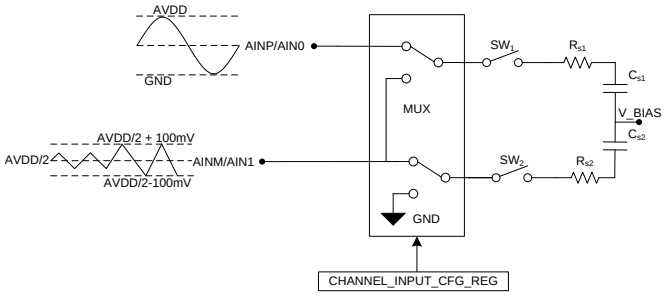


**Figure 4. Single-Channel, Pseudo-Differential Configuration**

The analog multiplexer supports following input configurations (set by writing into *CHANNEL_INPUT_CFG* register).

#### *7.3.1.1 Two-Channel Single-Ended Configuration*

Refer to Figure 2. Set CH0_CH1_IP_CFG bits = 00b or 11b to select this configuration. This is also the default configuration of the device after power up. In this configuration, $C_{S2}$ always samples the GND pin and $C_{S1}$ samples input signal provided on Channel 0 (AINP/AIN0) or Channel 1 (AINM/AIN1) based on the channel selection. Each analog input channel can accept input signals in the range 0 V to AVDD V.

## Feature Description (continued)

#### 7.3.1.2 Single-Channel, Single-Ended Configuration

Refer to Figure 3. Set CH0_CH1_IP_CFG bits = 01b to select this configuration. In this configuration, $C_{S1}$ samples input signal provided on the AINP/AIN0 pin whereas $C_{S2}$ samples input signal provided on the AINM/AIN1 pin. AINP/AIN0 pin can accept input signals in the range 0 V to AVDD V and AINM/AIN1 pin can accept input signals in the range –100 mV to +100 mV. This input configuration is useful in systems where the sensor and/or the signal conditioning block is placed far from the device and there could be a small difference between the ground potentials. In this channel configuration, selecting channel 1 in AUTO sequence leads to an error condition and the device sets an error flag in *SEQUENCE_STATUS* register.

#### 7.3.1.3 Single-Channel, Pseudo-Differential Configuration

Refer to Figure 4. Set CH0_CH1_IP_CFG bits = 10b to select this configuration. In this configuration, $C_{S1}$ samples input signal provided on the AINP/AIN0 pin whereas $C_{S2}$ samples input signal provided on the AINM/AIN1 pin. AINP/AIN0 pin can accept input signals in the range 0 V to AVDD V and AINM/AIN1 pin can accept input signals in the range (AVDD/2) - 100 mV to (AVDD/2) + 100 mV. This input configuration is useful to interface with sensors that provide pseudo-differential analog output .In this channel configuration, selecting channel 1 in AUTO sequence leads to an error condition and the device sets an error flag in *SEQUENCE_STATUS* register.

#### 7.3.1.4 Channel Sequencing

The device has two channel sequencing modes: Default and AUTO. On power-up, the device wakes up in default sequence with Two-Channel, Single-Ended Configuration and scans channel 0 only. The sequence and operation mode of the device can be selected by setting bits in *OPMODE_SEL* register. The device can not operate in default sequence in Autonomous modes and High Precision mode.

In AUTO sequence mode, the device can be configured to scan through either Channel 0 or Channel 1 by setting bits in *AUTO_SEQ_CHEN* register. The device can operate in all modes with AUTO sequence. Selecting Channel 1 in Single-Channel, Single-Ended Configuration and in Single-Channel, Pseudo-Differential Configuration leads to an error in *SEQUENCE_STATUS* register.

### 7.3.2 Reference

The device uses the analog supply voltage (AVDD) as a reference for the analog-to-digital conversion process. TI recommends placing a 220-nF, low-ESR ceramic decoupling capacitor between the AVDD pin and the GND pin. Refer to *Power-Supply Recommendations* section.

### 7.3.3 ADC Transfer Function

The ADC output is always in straight binary format. The ADC resolution can be computed by Equation 1:

$$1\ LSB = V_{REF} / 2^N \quad (1)$$

where:

- $V_{REF}$ = AVDD
- N = 12 for Autonomous Monitoring Modes and $I^2C$ Command Mode

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## Feature Description (continued)

Figure 5 and Figure 6 show the ideal transfer characteristics for Single-Ended Input and Pseudo-Differential Input, respectively. Table 1 show the digital output codes for the transfer functions.

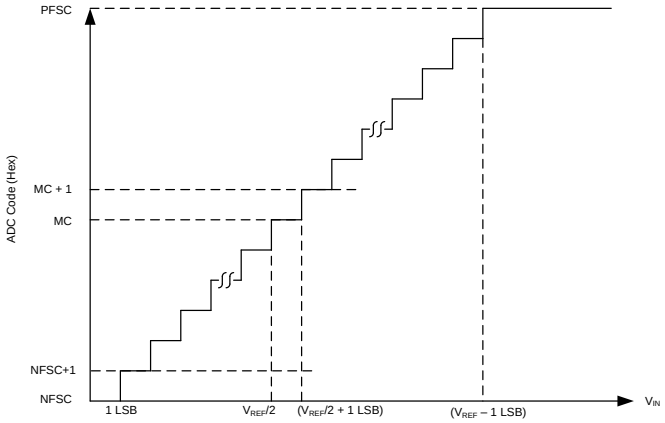


**Figure 5. Ideal Transfer Characteristics for Single-Ended Input**

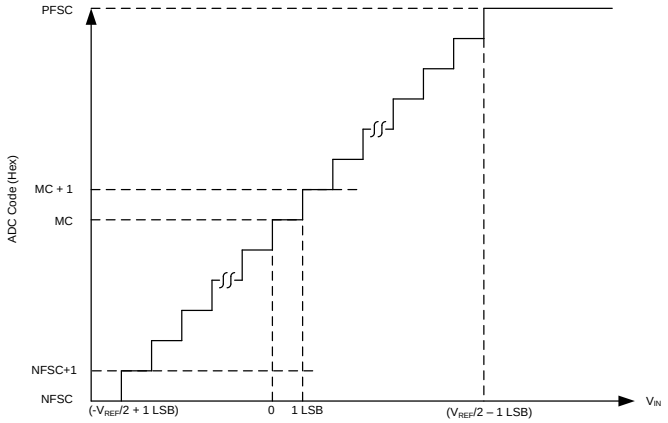


**Figure 6. Ideal Transfer Characteristics for Pseudo-Differential Input**

**Table 1. Transfer Characteristics**

| INPUT VOLTAGE for SINGLE ENDED INPUT | INPUT VOLTAGE for PSEUDO DIFFERENTIAL INPUT | CODE | DESCRIPTION | IDEAL OUTPUT CODE |
|---|---|---|---|---|
| | | | | Autonomous Monitoring Mode Or $I^2C$ Command Mode |
| ≤1 LSB | ≤($-V_{REF}$/2 + 1) LSB | NFSC | Negative full-scale code | 000 |
| 1 LSB to 2 LSBs | ($-V_{REF}$/2 + 1) to ($-V_{REF}$/2 + 2) LSB | NFSC + 1 | — | 001 |
| ($V_{REF}$ / 2) to ($V_{REF}$ / 2) + 1 LSB | 0 to 1 LSB | MC | Mid code | 800 |
| ($V_{REF}$ / 2) + 1 LSB to ($V_{REF}$ / 2) + 2 LSBs | 1 to 2 LSB | MC + 1 | — | 801 |
| ≥ $V_{REF}$ – 1 LSB | ≥ $V_{REF}$/2 – 1 LSB | PFSC | Positive full-scale code | FFF |

### 7.3.4 Oscillator and Timing Control

The device uses one of the two internal oscillators (Low Power Oscillator or High Speed Oscillator) for converting the analog input voltage into a digital output code.

In *Autonomous Mode* and *High Precision Mode*, the balance between sampling speed and power consumption can be obtained:

1. Select the Low Power Oscillator (*OSC_SEL* = 1b) to monitor slow moving signals at extremely low power consumption. Select the High Speed Oscillator (*OSC_SEL* = 0b) to scan the sensor signals with faster sampling speed.
2. Set sampling speed by programming the *nCLK* register:

$$f_S = \frac{f_{OSC}}{nCLK} \quad (2)$$

- $f_s$ = Sampling Speed
- $f_{OSC}$ = Oscillator Frequency = $1/t_{OSC}$, refer the *Specifications*
- nCLK is number of clocks in one conversion cycle (*nCLK* register)

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### 7.3.5 I²C Address Selector

The I²C address for the device is determined by connecting external resistors on ADDR pin. The device address will be selected on power-up based on the resistor values. The device retains this address until the next power up or untill next device reset or until the device receives a command to program its own address (*General Call with Write Software programmable part of slave address* ). Figure 7 provides the connection diagram for the ADDR pin and Table 2 provides the resistor values for selecting different addresses of the device.

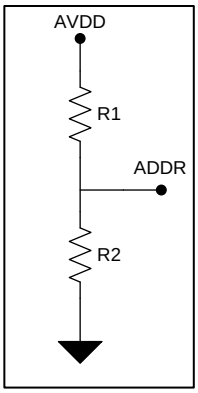




**Figure 7. External Resistor Connection Diagram for ADDR Pin**

**Table 2. I²C Address Selection**

| Resistors | | Address |
|---|---|---|
| R1 (1) | R2 (1) | |
| 0 Ω | DNP (2) | 0011111b (1Fh) |
| 11 kΩ | DNP (2) | 0011110b (1Eh) |
| 33 kΩ | DNP (2) | 0011101b (1Dh) |
| 100 kΩ | DNP (2) | 0011100b (1Ch) |
| DNP (2) | 0Ω or DNP (2) | 0011000b (18h) |
| DNP (2) | 11 kΩ | 0011001b (19h) |
| DNP (2) | 33 kΩ | 0011010b (1Ah) |
| DNP (2) | 100 kΩ | 0011011b (1Bh) |

(1) Tolerance for R1,R2 < ±5%
(2) DNP = Do not populate

### 7.3.6 Data Buffer

When operating in Autonomous Monitoring Mode, the device can utilize the internal data buffer for diagnostic and/or data storage. The internal data buffer is 16-bit wide and 16-word deep and follows the FIFO (first-in, first-out) approach.

The write operation to the data buffer starts and stops as per the settings in the *DATA_BUFFER_OPMODE* register. *DATA_BUFFER_STATUS* register provides the number of entries filled in the data buffer and this register can be read during an active sequence to get the current status of the data buffer. The time between two consecutive conversions is set by the *nCLK* register and Equation 3 provides the relationship for time between two consecutive conversions of the same channel and nCLK parameter.

$$t_{cc} = k \times nCLK \times t_{OSC}$$

where

- $t_{cc}$ is time between two consecutive conversions of same channel.
- k is number of channels enabled in the device sequence.
- nCLK is number of clocks used by device for one conversion cycle.
- $t_{OSC}$ is time period of oscillator used by the device. Refer to the *Specifications*. (3)

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The 16-bit contents of each entry in the data buffer are set by programming the *DATA_OUT_CFG* register. The DATA_OUT_CFG registers enables the Channel ID and DATA_VALID flag in data buffer. Channel ID represents the channel number for the data entry in the data buffer. DATA_VALID is set to zero in either of the following conditions:

- If the entry in the data buffer is not filled after the last start of sequence.
- If the $I^2C$ master tries to read more than 16 entries from the data buffer, device provides zeros with DATA_VALID set to zero.

At the end of the write operation, the data buffer always has results of 16 (or lesser) consecutive conversions. The data buffer is filled in the order that the data is converted by the ADC. The channels converted by the ADC are controlled by the *AUTO_SEQ_CHEN* register.

#### 7.3.6.1 Reading data from the Data Buffer

The device brings the BUSY/$\overline{\text{RDY}}$ pin low after completion of the sequence or after the *SEQ_ABORT* bit is set. As illustrated in Figure 8, the device provides the contents of the data buffer (in FIFO fashion) on receiving $I^2C$ read frame, which consists of the device address and the read bit set to 1.

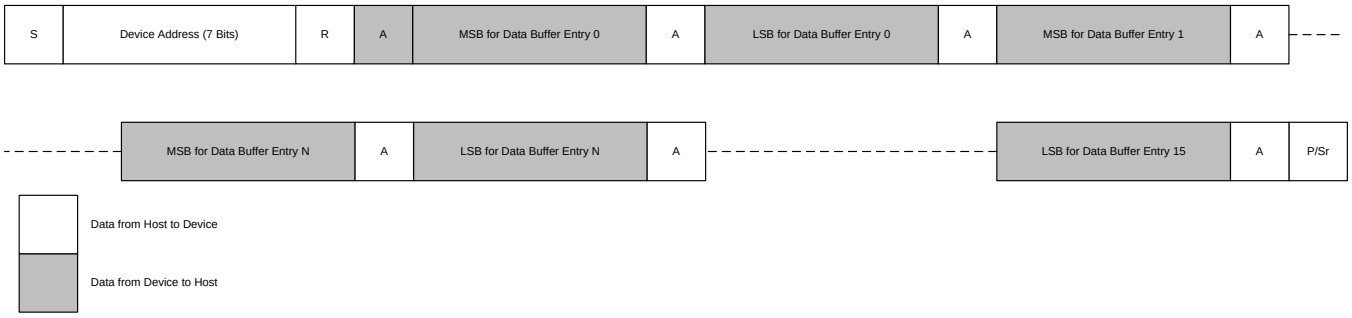


**Figure 8. Reading Data Buffer**

The device returns zeroes with DATA VALID flag set to zero for all $I^2C$ read frames received after all the valid data words from the data buffer are read or when a $I^2C$ read frame is issued during an active sequence (indicated by high on the BUSY/$\overline{\text{RDY}}$ pin).The data buffer is reset by setting the *SEQ_START* bit and after resetting the device.

### 7.3.7 Accumulator

When operating in High Precision Mode, the device offers a 16-bit internal accumulator per channel. Accumulator for a channel is enabled only if that channel is selected in the channel scanning sequence. The time between two consecutive conversions for accumulation is controlled by the *nCLK* register and Equation 3 provides the relationship for time between two consecutive conversions of same channel and nCLK parameter.

The accumulated data can be read from the *ACCUMULATOR_DATA* registers in the device. *ACCUMULATOR_STATUS* register provides the number of accumulations done in the accumulator till last conversion. This register can be read during an active sequence to get the current status of the accumulator. The accumulator is reset on setting the *SEQ_START* bit and on resetting the device. Equation 4 provides the relationship between High precision data and ADC conversion results.

$$\text{High Precision Data for CHx} = \sum_{k=1}^{16} \text{Conversion Result[k] for CHx} \tag{4}$$

Equation 5 provides the value of LSB in high precision mode for the accumulated result.

$$1\ LSB = \frac{AVDD}{2^{16}} \tag{5}$$

### 7.3.8 Digital Window Comparator

The internal Digital Window Comparator is available in all modes. In Autonomous modes with Thresholds monitoring and Diagnostics, the digital window comparator controls the filling of the data and the output of the alert pin buffer and in other modes, it only controls the output of the alert pin. Figure 9 provides the block diagram for digital window comparator.

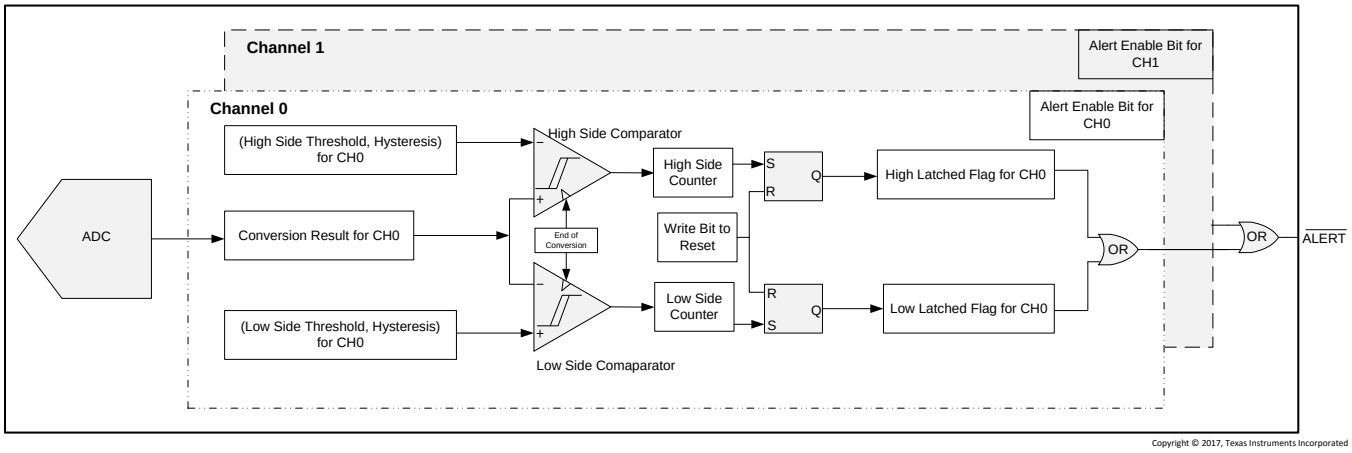


**Figure 9. Digital Comparator Block Diagram**

The Low Side Threshold, High Side Threshold, and Hysteresis parameters are independently programmable for each input channel. Figure 10 shows the comparison thresholds and hysteresis for the two comparators. A Pre-Alert event counter after each comparator counts the output of the comparator and sets the latched flags. The Pre-Alert Event Counter settings are common to the two channels.

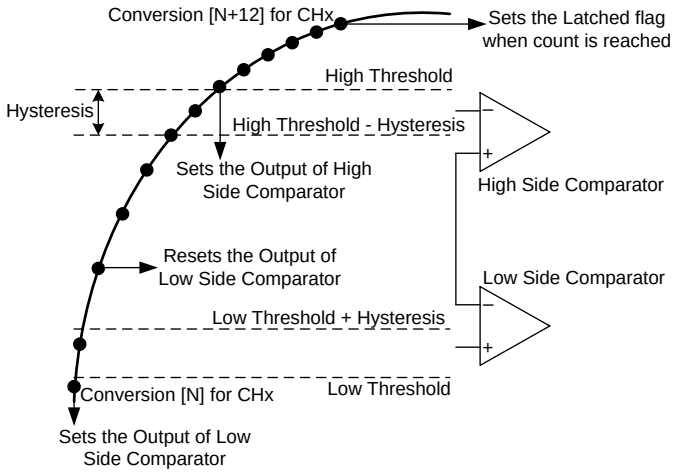


**Figure 10. Thresholds and Hysteresis for Digital Window Comparator**

DWC_BLOCK_EN bit in *ALERT_DWC_EN* register enables/disables the complete Digital Window Comparator block (disabled at power-up) and ALERT_EN_CHx bits in *ALERT_CHEN* register enable Digital Window Comparator for respective channels. Once enabled, whenever a new conversion result is available:

1. the High Side Comparator and the Low Side Comparator compare it with the specified thresholds applicable for that channel
2. the Pre-Alert Event Counter increments if the comparator output is 1, else it resets back to 0

Therefore, the latched flags (high and low) for the channel are updated only if the respective comparator output remains 1 for the specified number of consecutive conversions (set by the Pre-Alert Event Counter).

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The latched flags can be read from the *ALERT_LOW_FLAGS* and *ALERT_HIGH_FLAGS* registers. To clear a latched flag, write 1 to the applicable bit location. The $\overline{\text{ALERT}}$ pin status is re-evaluated whenever an applicable latched flag gets set or is cleared.

### 7.3.9 I²C Protocol Features

#### *7.3.9.1 General Call*

On receiving a general call (00h), the device provides an ACK.

#### *7.3.9.2 General Call with Software Reset*

On receiving a general call (00h) followed with Software Reset (06h), the device resets itself.

#### *7.3.9.3 General Call with Write Software programmable part of slave address*

On receiving a general call (00h) followed by 04h, the device re-evaluates its own I²C address configured by the ADDR pin. During this operation, the device keeps BUSY/$\overline{\text{RDY}}$ Pin high and does not respond to other I²C commands except general call.

#### *7.3.9.4 Configuring Device into High Speed I²C mode*

The device can be configured in High Speed I²C mode by providing an I²C frame with one of the codes listed as follows:

- 09h
- 0Bh
- 0Dh
- 0Fh

After receiving one of the above listed codes, the device sets the HS_MODE bit in *OPMODE_I2CMODE_STATUS* register and remains in High Speed I²C mode until a STOP condition is received in an I²C frame.

### 7.3.10 Device Programming

Table 3 provides the acronyms for different conditions in an I²C Frame.

**Table 3. I²C Frame Acronyms**

| Symbol | Description |
|---|---|
| S | Start condition for I²C Frame |
| Sr | Re-start condition for I²C Frame |
| P | Stop condition for I²C Frame |
| A | ACK (Low) |
| N | NACK (High) |
| R | Read Bit (High) |
| W | Write Bit (Low) |

**Table 4. Opcodes for Commands**

| Opcode | Command Description |
|---|---|
| 00010000b | Single Register Read |
| 00001000b | Single Register Write |
| 00011000b | Set Bit |
| 00100000b | Clear Bit |
| 00110000b | Reading a continuous block of registers |
| 00101000b | Writing a continuous block of registers |

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#### 7.3.10.1 Reading Registers

The I²C master can either read a single register or a continuous block registers from the device as described in *Single Register Read* and in *Reading a continuous block of registers*.

##### 7.3.10.1.1 Single Register Read

To read a single register from the device, the I²C master has to first provide an I²C command with three frames as illustrated in Figure 11 to set the address. The register address is the address of the register which needs to be read. The opcodes for different commands are listed in Table 4.

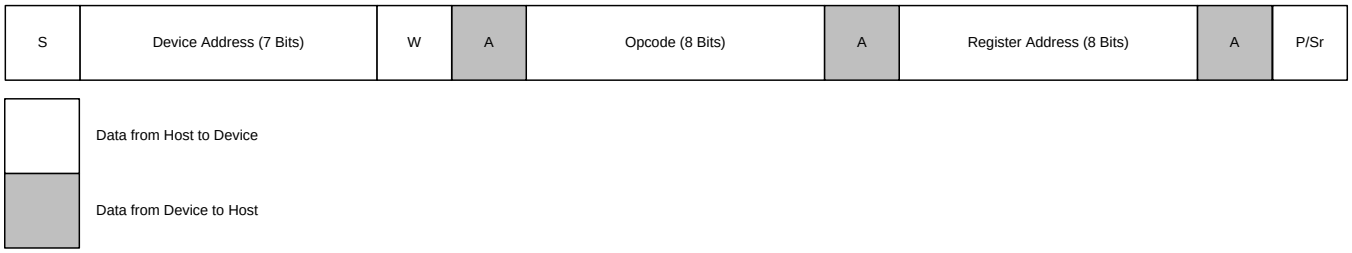


**Figure 11. Setting Register Address for Reading Registers**

After this, the I²C master has to provide another I²C frame containing the device address and read bit as illustrated in Figure 12. After this frame, the device provides register data. if the host provides more clocks, the device provides same register data. To end the register read command, the master has to provide a STOP or a RESTART condition in the I²C frame.

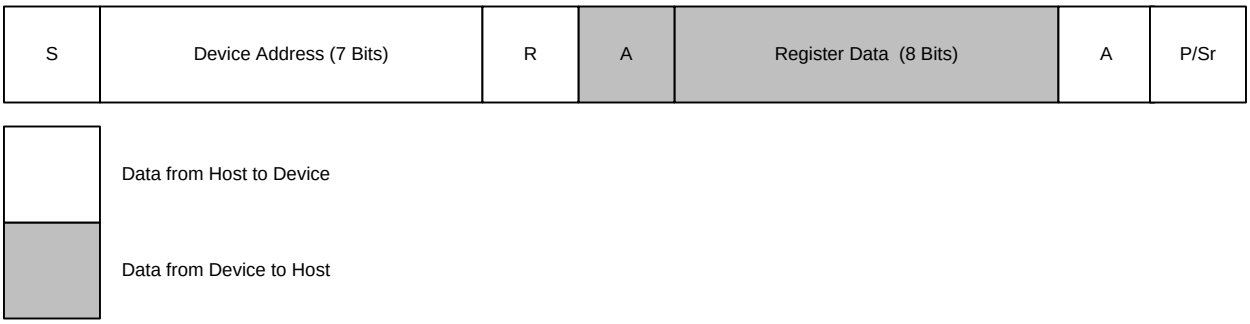


**Figure 12. Reading Register Data**

##### 7.3.10.1.2 Reading a continuous block of registers

To read a continuous block of registers, the I²C master has to first provide an I²C command as illustrated in Figure 11 to set the address. The register address is the address of the first register in the block which needs to be read. The opcodes for different commands are listed in Table 4.

After this, the I²C master has to provide another I²C frame containing the device address and read bit as illustrated in Figure 13. After this frame, the device provides register data. On providing more clocks, the device provides data for next register. On reading data from addresses which does not exist in the *Register Map* of the device, the device returns zeros. If the device does not have any further registers to provide the data, it will provide zeros. To end the register read command, the master has to provide a STOP or a RESTART condition in the I²C frame.

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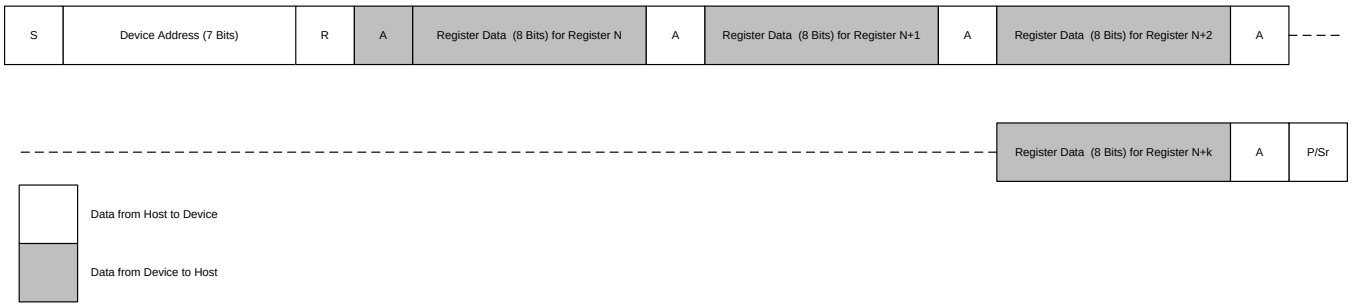


**Figure 13. Reading a continuous block of registers**

### *7.3.10.2 Writing Registers*

The $I^2C$ master can either write a single register or a continuous block registers to the device or set few bits in a register or clear few bits in a register.

#### 7.3.10.2.1 Single Register Write.

To write a single register from the device, the $I^2C$ master has to provide an $I^2C$ command with four frames as illustrated in Figure 14. The register address is the address of the register which needs to be written and register data is the value that needs to be written. The opcodes for different commands are listed in Table 4. To end the register write command, the master has to provide a STOP or a RESTART condition in the $I^2C$ frame.


**Figure 14. Writing a Single Register**

#### 7.3.10.2.2 Set Bit

To set bits in a register without changing the other bits, the $I^2C$ master has to provide an $I^2C$ command with four frames as illustrated in Figure 14. The register address is the address of the register in which the bits needs to be set and register data is the value representing the bits which need to be set. Bits with value as 1 in register data are set and bits with value as 0 in register data are not changed. The opcodes for different commands are listed in Table 4. To end this command, the master has to provide a STOP or RESTART condition in the $I^2C$ frame.

#### 7.3.10.2.3 Clear Bit

To clear bits in a register without changing the other bits, the $I^2C$ master has to provide an $I^2C$ command with four frames as illustrated in Figure 14. The register address is the address of the register in which the bits needs to be cleared and register data is the value representing the bits which need to be cleared. Bits with value as 1 in register data are cleared and bits with value as 0 in register data are not changed. The opcodes for different commands are listed in Table 4. To end this command, the master has to provide a STOP or a RESTART condition in the $I^2C$ frame.

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#### 7.3.10.2.4 Writing a continuous block of registers

To write a continuous block of registers, the $I^2C$ master has to provide an $I^2C$ command as illustrated in Figure 15. The register address is the address of the first register in the block which needs to be written. The $I^2C$ master has to provide data for registers in subsequent $I^2C$ frames in an ascending order of register addresses. Writing data to addresses which does not exist in the *Register Map* of the device has no effect. The opcodes for different commands are listed in Table 4. if the data provided by the $I^2C$ master exceeds the address space of the device, the device will neglect the data beyond the address space. To end the register write command, the master has to provide a STOP or a RESTART condition in the $I^2C$ frame.

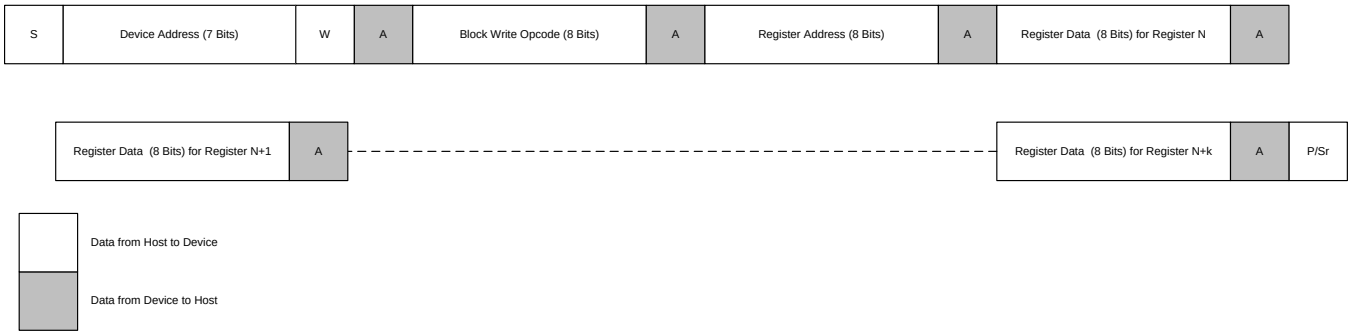


**Figure 15. Writing a continuous block of registers**

### 7.3.11 OFFSET Calibration

The offset can be calibrated by setting TRIG_OFFCAL bit in *OFFSET_CAL* register. During offset calibration, the sampling switches are open (Figure 1) and the device keeps BUSY/$\overline{\text{RDY}}$ pin high. The device calculates its offset error and corrects for this error for subsequent conversions. The device calibrates the offset on power up. To nullify the change in offset due to change in temperature or in AVDD voltage, TI recommends to calibrate the offset of the device.

## 7.4 Device Functional Modes

The device has below functional modes:

- $I^2C$ Command Mode
- Autonomous Mode
  - Autonomous Mode with Threshold Monitoring and Diagnostics.
  - Autonomous Mode with Burst Data
- High Precision Mode

Device powers up in $I^2C$ Command mode and can be configured into either of these modes by writing the configuration registers for the desired mode. Steps for configuring device into different modes are illustrated in Figure 16

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## Device Functional Modes (continued)

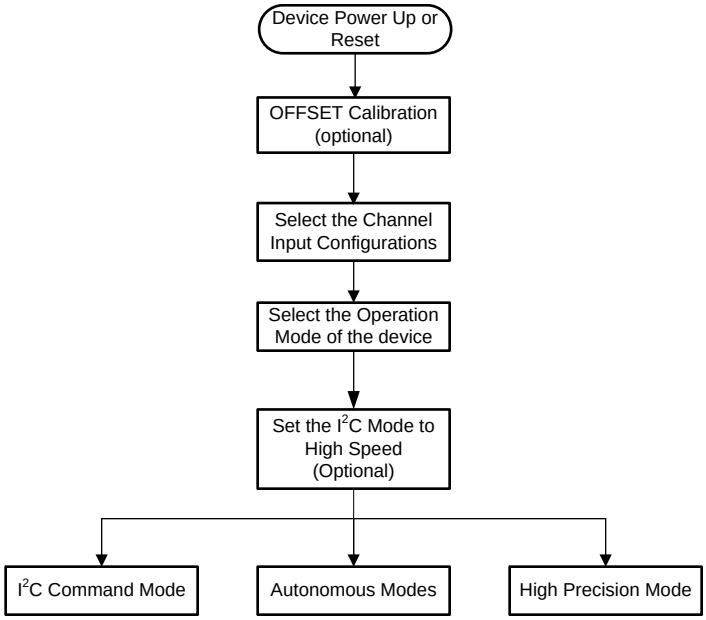


**Figure 16. Configuring Device into different modes**

### 7.4.1 Device Power Up and Reset

On Power Up, the device calibrates its own offset and calculates the address from the resistors connected on ADDR pin. During this time, the device keeps BUSY/$\overline{RDY}$ high.

Device can be reset by recycling power on AVDD pin, by General Call(00h) followed by software reset(06h) or by writing the WKEY followed by setting the DEV_RST bit.

On recycling power on AVDD pin and on General call(00h) followed by software reset(06h), all the device configurations gets reset and device initiates offset calibration and re-evaluates its $I^2C$ address.

On setting the DEV_RST bit, all the device configurations except latched flags for Digital Window Comparator and WKEY get reset and the device does not initiate offset calibration and does not re-evaluate its $I^2C$ address.

### 7.4.2 $I^2C$ Command Mode

$I^2C$ Command Mode allows the external host processor to directly request and control when the data is sampled. The data capture is initiated by an $I^2C$ command from the host processor and the data is then returned over the $I^2C$ bus at a throughput rate of up to 140-kSPS. Applications that could take advantage of this type of functionality include traditional ADC applications that require 1 or 2 channels of continuous data output.

After setting the operation mode to $I^2C$ command mode as illustrated in Figure 16, steps for operating the device to be in $I^2C$ Command mode and reading data are illustrated in Figure 17. On power-up the device is in $I^2C$ Command mode using the single ended and dual channel configuration and starts by sampling the analog input applied on Channel 0 (AINP/AIN0 - GND). In this mode, the device uses the high frequency oscillator for conversions. The host can either configure the device to scan through one channel or both channels by configuring the *CHANNEL_INPUT_CFG* register and *AUTO_SEQ_CFG* register.

- $I^2C$ Command Mode with Default Sequence(CH0)

  Set the *OPMODE_SEL* register to 000b or 001b for $I^2C$ Command Mode with Default Sequence(CH0). The host has to provide device address and read bit to start the conversions. To continue with conversions and reading data, the host to provide continuous SCL (Figure 18). A STOP condition in $I^2C$ frame is required to abort the operation in this mode and then the device operation mode can be changed to another operation mode.
- $I^2C$ Command Mode with Auto Sequence

## Device Functional Modes (continued)

Set the *OPMODE_SEL* register to 100b or 101b for I²C Command Mode with AUTO Sequence. The host has to set the SEQ_START bit in *START_SEQUENCE* register and provide the device address and read bit to start the conversions. To continue with conversions and reading data, the host to provide continuous SCL(Figure 18). SEQ_ABORT bit in *ABORT_SEQUENCE* register needs to be set to abort the operation in this mode and then the device operation mode can be changed to another operation mode. A register read aborts the AUTO sequence in this mode.

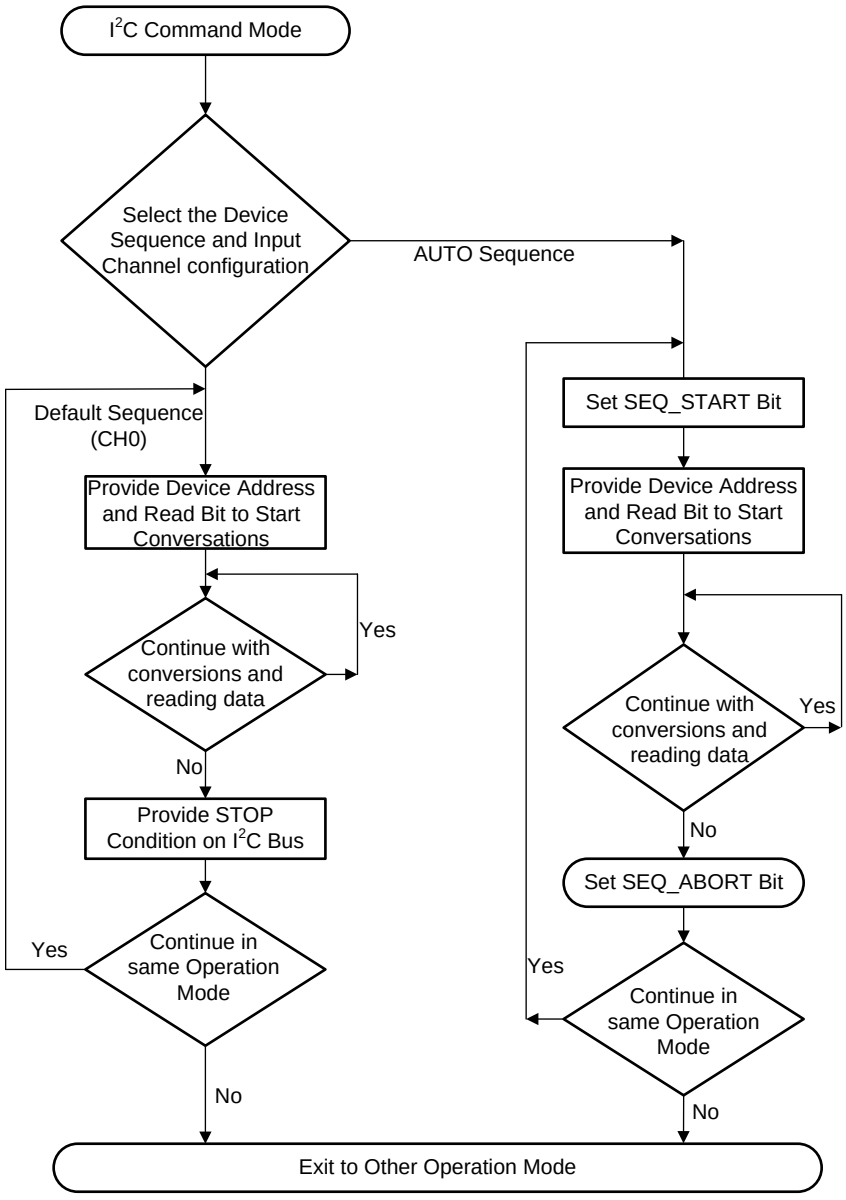


**Figure 17. Device Operation in I²C Command mode**

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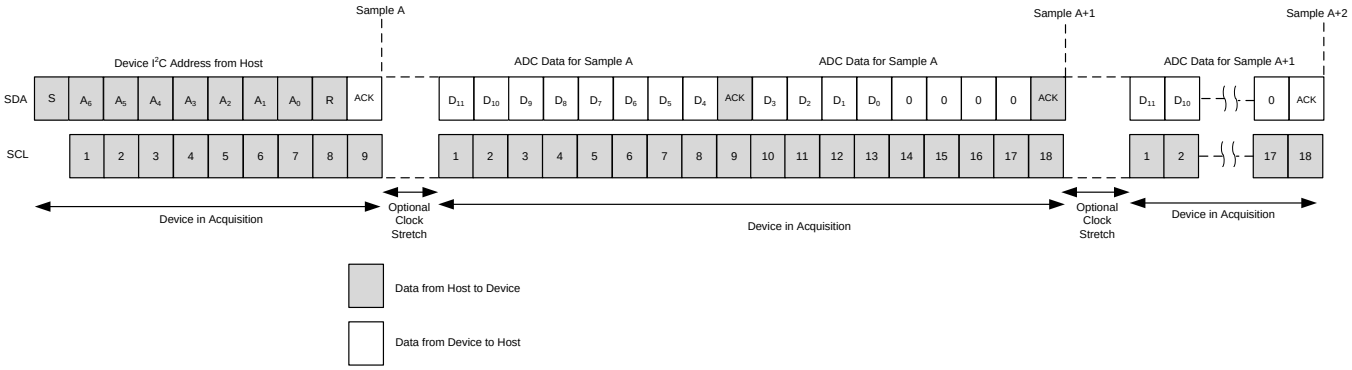
## Device Functional Modes (continued)

Data can be read from the device by providing a device address and read bit followed by continuous SCL as shown in Figure 18.




(1) Refer to Equation 6 for sampling speed in I²C Command mode.

**Figure 18. Starting Conversion and reading data in I²C Command Mode**

In I²C command mode, the device always uses the High Speed Oscillator and the nCLK parameter has no effect. The maximum scan rate is given by Equation 6:

$$f_S = \frac{1000}{\left[18 \times T_{SCL} + k\right]}$$

- $f_s$ = Maximum sampling Speed in kSPS
- $T_{SCL}$= Time period of SCL clock (in µsec)
- if $T_{SCL\text{-}LOW}$ (Low period of SCL) < 1.8.µsec, k = (1.8 - $T_{SCL\text{-}LOW}$ ) and Device stretches clock in I²C Command mode. Not Applicable for Standard I²C Mode (100 kHz).
- if $T_{SCL\text{-}LOW}$ (Low period of SCL) ≥ 1.8.µsec, k = 0 and Device does not stretch clock in I²C Command mode. (6)

### 7.4.3 Autonomous Mode

In Autonomous mode, the device can be programmed to monitor the voltage applied on the analog input pins of the device and generate a signal on the ALERT pin when the programmable high or low threshold values are crossed and store the conversion results in the data buffer after or before the crossing a threshold or after or before the user command.

In Autonomous mode, the device generates the start of conversion using the internal oscillator. The first start of conversion needs to be provided by the host and the device generates the subsequent start of conversions.

After configuring the operation mode to autonomous mode (Set *OPMODE_SEL* register to 110b) as illustrated in Figure 16, steps for operating the device to be in different autonomous modes are illustrated in Figure 19

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## Device Functional Modes (continued)

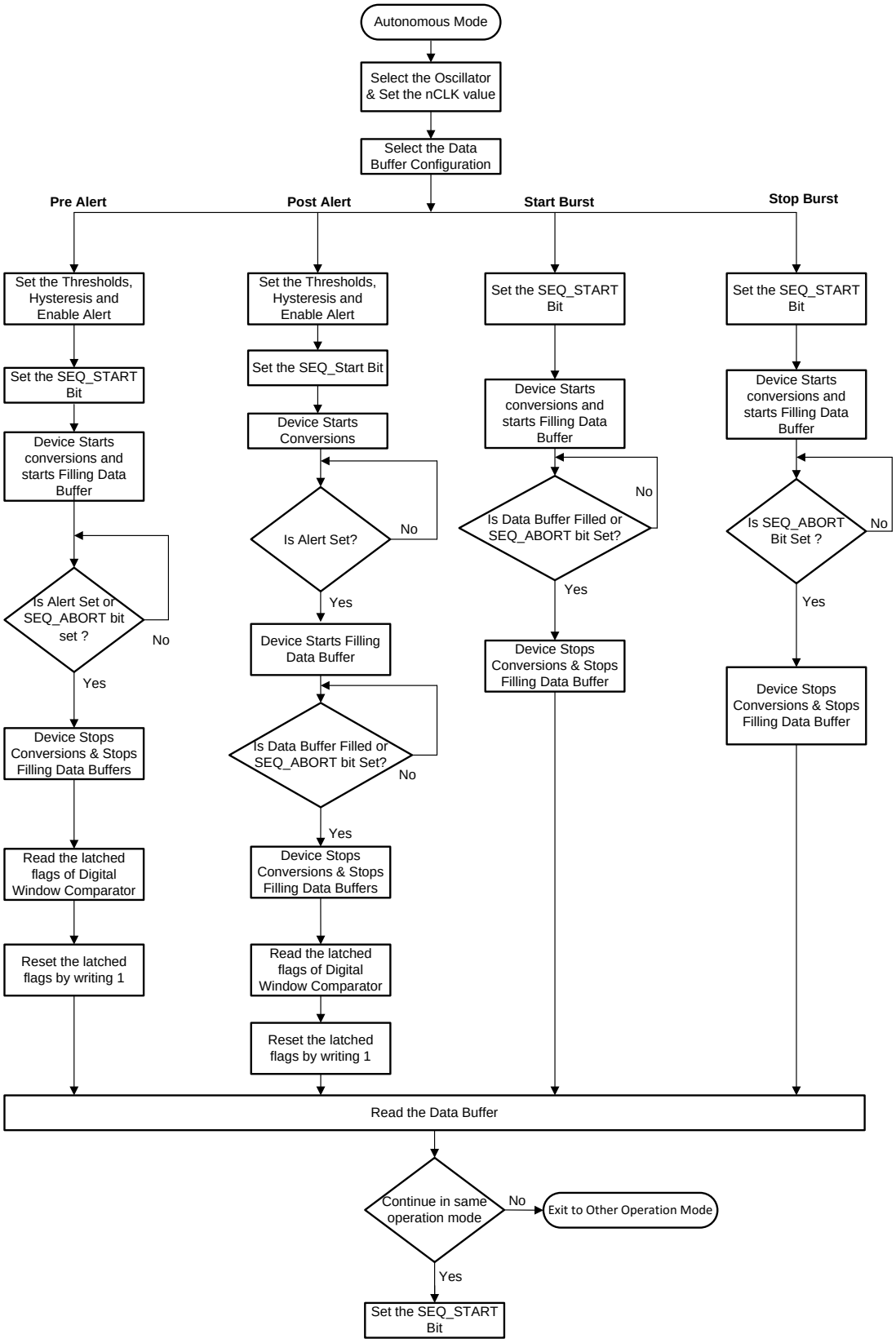


**Figure 19. Configuring Device in Autonomous Modes**

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## Device Functional Modes (continued)

TI recommends to abort the present sequence by setting the SEQ_ABORT bit before changing the device operation mode or device configuration.

### *7.4.3.1 Autonomous Mode with Threshold Monitoring and Diagnostics*

The Threshold Monitoring Mode automatically scans the input voltage on the input channel(s) and generates a signal when the programmable high or low threshold values are crossed. This mode is useful for applications where the output of the sensor needs to be continuously monitored and action only taken when the sensor output deviates outside of an acceptable range. Applications that could take advantage of this type of functionality include wireless sensor nodes, environmental sensors, smoke and heat detectors, motion detectors, and so on.

In this mode, the data buffer can be configured to store the conversion results of the ADC in two different ways.

#### 7.4.3.1.1 Autonomous Mode with Pre Alert Data

For this mode, Set *DATA_BUFFER_OPMODE* to 100b. In this mode, the device starts conversions and starts storing the data on setting the bit in *SEQ_START* register and continues to store the data into the data buffer until one of the digital comparator flags is set for crossing a high threshold or a low threshold for the channels selected in the sequence. If the *SEQ_ABORT* bit is set before the data buffer is filled, the device aborts the sequence and stop storing the conversion results. If more than 16 conversions occur between start of sequence and alert output, the entries written first into the data buffer are discarded.

Figure 20 and Figure 21 illustrates the filling of data buffer in autonomous mode with Pre alert Data.

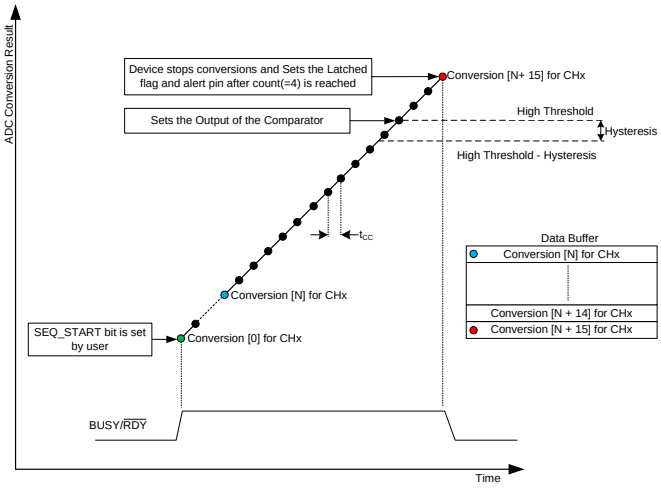


**Figure 20. Pre Alert Data for Single Channel Configurations**

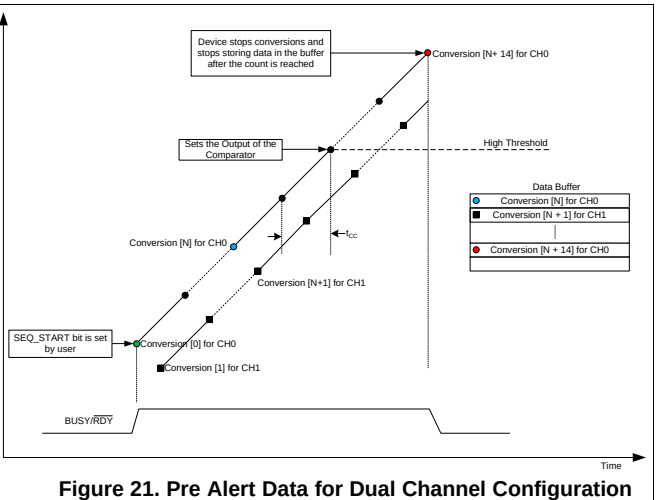


**Figure 21. Pre Alert Data for Dual Channel Configuration**

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## Device Functional Modes (continued)

#### 7.4.3.1.2 Autonomous Mode with Post Alert Data

For this mode, Set DATA_BUFFER_OPMODE to 110b. In this mode, the device starts converting the data on setting the SEQ_START bit and stores the data into the data buffer when one of the digital comparator flags is set after the crossing a high threshold or a low threshold for the channels selected in the sequence. if the *SEQ_ABORT* bit is set before the data buffer is filled, the device aborts the sequence and stop storing the conversion results .

Figure 22 and Figure 23 illustrates the filling of the data buffer in autonomous mode with Post Alert Data.

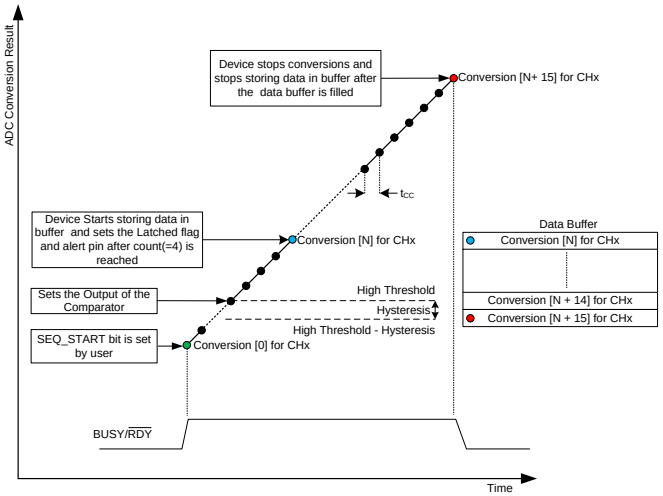


**Figure 22. Post Alert Data for Single Channel Configurations**

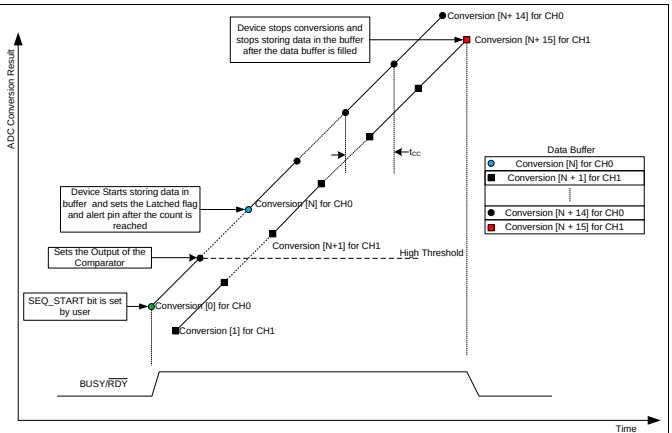


**Figure 23. Post Alert Data for Dual Channel Configuration**

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## Device Functional Modes (continued)

### 7.4.3.2 Autonomous Mode with Burst Data

In this mode the device can be configured to store up-to 16 conversion results in the data buffer based on user command. Applications that could take advantage of this mode are remote data loggers, environmental sensing and patient monitors. In this mode, the user can either start the burst or stop the burst of data as described as follows:

#### 7.4.3.2.1 Autonomous Mode with Start Burst:

For this mode, Set *DATA_BUFFER_OPMODE* to 001b. With Start Burst, the user can configure the device to start the filling of data buffer with conversion results by setting the *SEQ_START* bit and the device stops converting data and filling the data buffer after the data buffer is filled.

Figure 24 and Figure 25 illustrates the filling of the data buffer in autonomous mode with Start Burst.

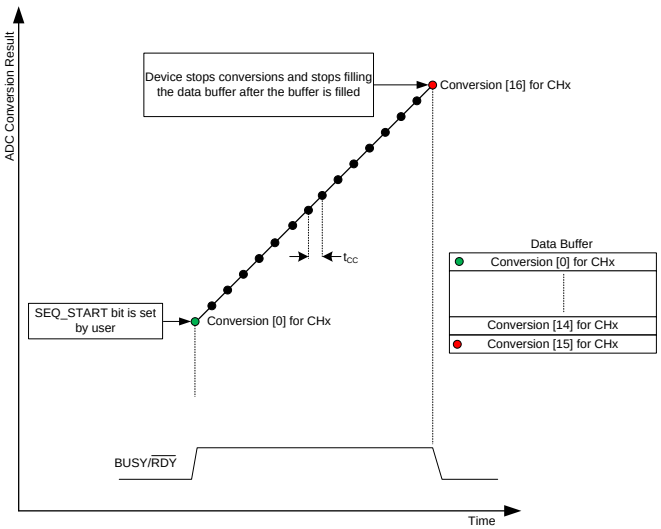


**Figure 24. Start Burst with Single Channel Configurations**

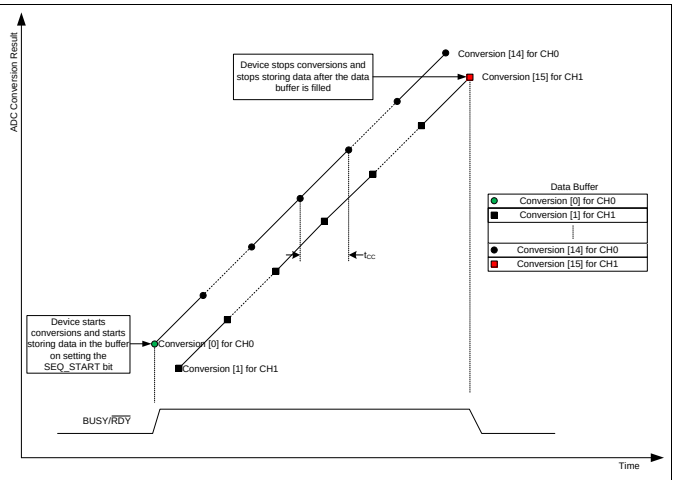


**Figure 25. Start Burst with Dual Channel Configuration**

ADVANCE INFORMATION

## Device Functional Modes (continued)

#### 7.4.3.2.2 Autonomous Mode with Stop Burst

For this mode, Set *DATA_BUFFER_OPMODE* to 000b. With Stop Burst, the user can configure the device to stop filling the data buffer with conversion results by setting the *SEQ_ABORT*bit .If more than 16 conversions occur between start of sequence and abort of sequence, the entries written first into the data buffer are discarded. Figure 26 and Figure 27 illustrate the filling of the data buffer in autonomous mode with Stop Burst .

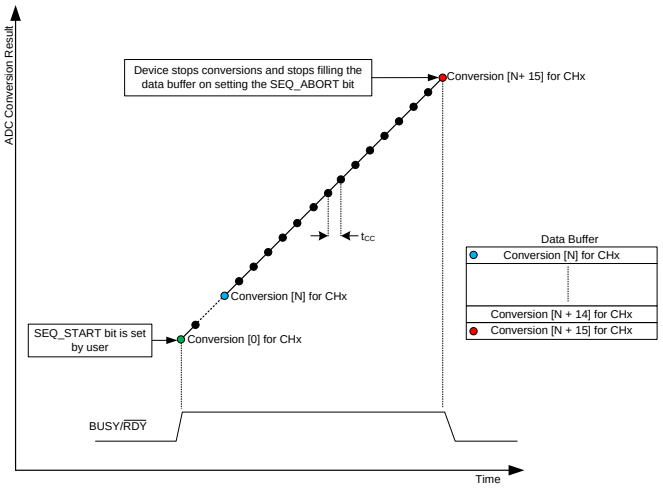


**Figure 26. Stop Burst with Single Channel Configurations**

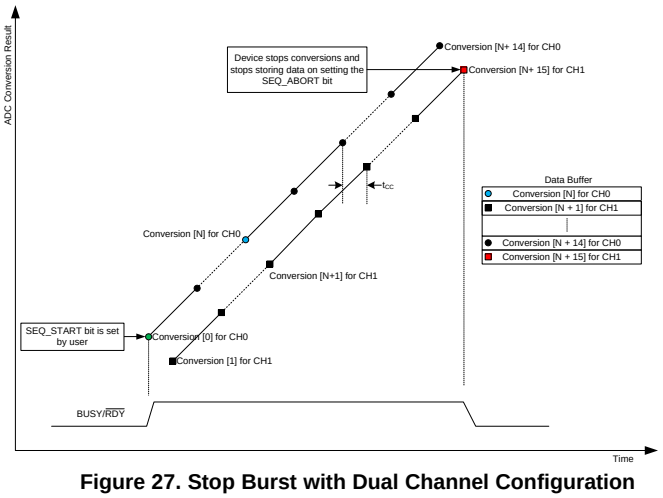


**Figure 27. Stop Burst with Dual Channel Configuration**

### 7.4.4 High Precision Mode

The High Precision Mode increases the accuracy of the data measurement to 16-bit accuracy. This is useful for applications where the level of precision required to accurately measure the sensor output needs to be higher than 12-bits. Applications that could take advantage of this type of functionality include gas detectors, air quality testers, water quality testers, and so on.

For this mode, Set *OPMODE_SEL* register to 111b. In this mode, the device starts converting and starts accumulating the conversion results in an accumulator on setting the *SEQ_START* bit. The device will stop accumulating the conversion results in accumulator after 16 conversions or when the *SEQ_ABORT* bit is set. Device can only function in Auto sequence in High precision mode. If the operation of the device is aborted in high precision mode before the BUSY/RDY pin goes low, the device provides invalid data. In this mode, on providing a device address and read bit for reading data buffer (Figure 8), the device provides zeroes as output. In this mode, the BUSY/RDY can be used to wake up the MCU or host from sleep or hibernation on completion of accumulation. The steps for configuring the device into High Precision Mode are illustrated in Figure 28 .

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## Device Functional Modes (continued)

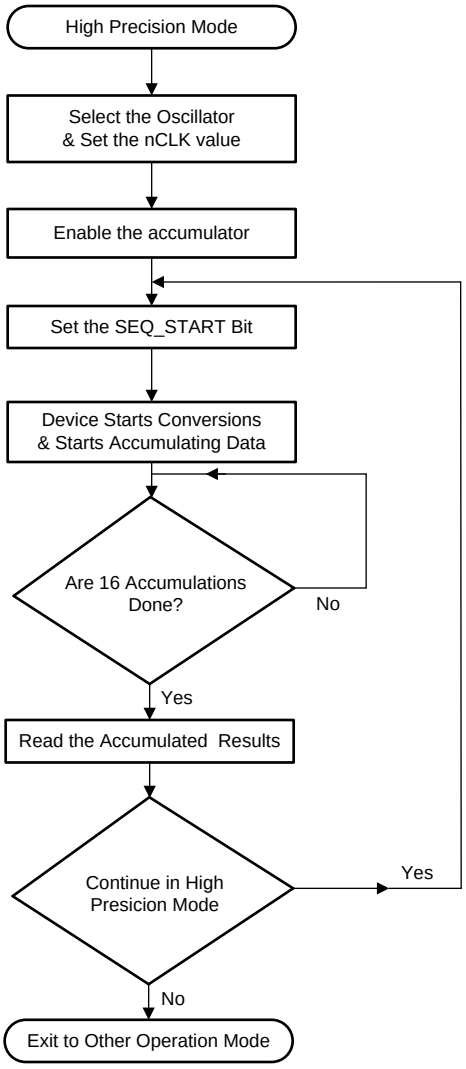


**Figure 28. Configuring Device in High Precision Mode**

TI recommends to abort the present sequence by setting the SEQ_ABORT bit before changing the device operation mode or device configuration.

## Device Functional Modes (continued)

Figure 29 illustrates the accumulation of conversion results in high precision mode.

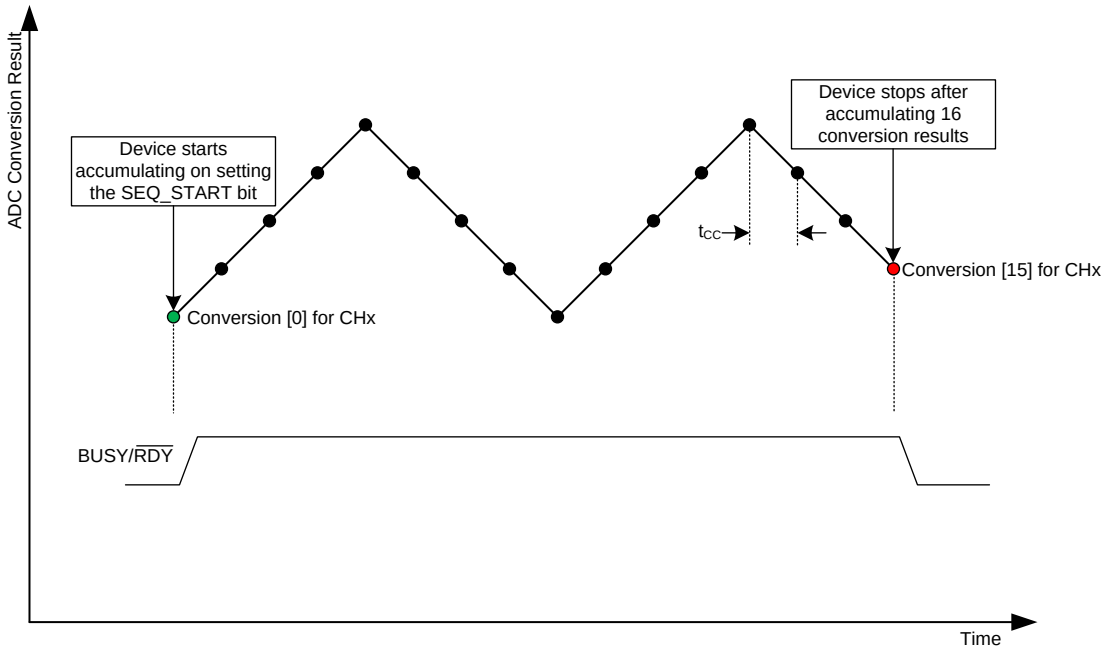


**Figure 29. High Precision Mode**

ADVANCE INFORMATION

## 7.5 Register Map

Table 5 provides the list of registers in the device. All the registers reset to their default values on power up and on receiving a General Call with Software Reset. (See Reset section).

**Table 5. Register Map**

| S.NO. | ADDRESS | REGISTER NAME | REGISTER DESCRIPTION |
|---|---|---|---|
| **RESET REGISTERS** | | | |
| 1 | 17h | WKEY | Write Key for writing into DEVICE_RESET register |
| 2 | 14h | DEVICE_RESET | Resets the device |
| **FUNCTIONAL MODE SELECT REGISTERS** | | | |
| 3 | 15h | OFFSET_CAL | Initiates Internal Offset Calibration Cycle |
| 4 | 1Ch | OPMODE_SEL | Sets the operation mode and enables auto-sequencing |
| 5 | 00h | OPMODE_I2CMODE_STATUS | Provides the present Operating Mode and $I^2C$ mode information |
| **INPUT CONFIG REGISTER** | | | |
| 6 | 24h | CHANNEL_INPUT_CFG | Configures the analog input channels |
| **ANALOG MUX and SEQUENCER REGISTERS** | | | |
| 7 | 20h | AUTO_SEQ_CHEN | Enables Auto sequencing for selected channels |
| 8 | 1Eh | START_SEQUENCE | Starts the channel scanning sequence |
| 9 | 1Fh | ABORT_SEQUENCE | Aborts the channel scanning sequence |
| 10 | 04h | SEQUENCE_STATUS | Provides the status of sequence in device |
| **OSCILLATOR and TIMING CONTROL REGISTERS** | | | |
| 11 | 18h | OSC_SEL | Selects the oscillator for the conversion process |
| 12 | 19h | nCLK_SEL | Sets the nCLK for the device |
| **DATA BUFFER CONTROL REGISTER** | | | |
| 13 | 2Ch | DATA_BUFFER_OPMODE | Selects Data Buffer operation mode |
| 14 | 28h | DOUT_FORMAT_CFG | Configures the data output format for data buffer |
| 15 | 01h | DATA_BUFFER_STATUS | Provides the present status of Data Buffer |
| **ACCUMULATOR CONTROL REGISTERS** | | | |
| 16 | 30h | ACC_EN | Enables the Accumulator |
| 17 | 08h | ACC_CH0_LSB | Provides the LSB of accumulated data for CH0 (Read Only) |
| 18 | 09h | ACC_CH0_MSB | Provides the MSB of accumulated data for CH0 (Read Only) |
| 19 | 0Ah | ACC_CH1_LSB | Provides the LSB of accumulated data for CH0 (Read Only) |
| 20 | 0Bh | ACC_CH1_MSB | Provides the MSB of accumulated data for CH0 (Read Only) |
| 21 | 02h | ACCUMULATOR_STATUS | Provides the present status of Accumulator |
| **DIGITAL WINDOW COMPARATOR REGISTERS** | | | |
| 22 | 37h | ALERT_DWC_EN | Enables the Alert and Digital Window Comparator block |
| 23 | 34h | ALERT_CHEN | Enables Alert functionality for individual channels |
| 24 | 39h | DWC_HTH_CH0_MSB | Sets the MSB for High threshold for CH0 |
| 25 | 38h | DWC_HTH_CH0_LSB | Sets the LSB for High Threshold for CH0 |
| 26 | 3Bh | DWC_LTH_CH0_MSB | Sets the MSB for Low threshold for CH0 |
| 27 | 3Ah | DWC_LTH_CH0_LSB | Sets the LSB for Low threshold for CH0 |
| 28 | 40h | DWC_HYS_CH0 | Sets Hysteresis for CH0 |
| 29 | 3Dh | DWC_HTH_CH1_MSB | Sets the MSB for High threshold for CH1 |
| 30 | 3Ch | DWC_HTH_CH1_LSB | Sets the LSB for High threshold for CH1 |
| 31 | 3Fh | DWC_LTH_CH1_MSB | Sets the MSB for Low threshold for CH1 |
| 32 | 3Eh | DWC_LTH_CH1_LSB | Sets the LSB for Low threshold for CH1 |
| 33 | 41h | DWC_HYS_CH1 | Sets Hysteresis for CH1 |
| 34 | 36h | PRE_ALERT_EVENT_COUNT | Sets the Pre-Alert Event Counter for both channels |
| 35 | 03h | ALERT_TRIG_CHID | Provides the channel ID of channel which was first to set the alert output |
| 36 | 0Ch | ALERT_LOW_FLAGS | Latched flags for Low alert |
| 37 | 0Eh | ALERT_HIGH_FLAGS | Latched flags for High alert |

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### 7.5.1 RESET REGISTERS

These registers control the device reset operation (see Reset section).

#### *7.5.1.1 WKEY Register (address = 17h), [reset = 00h]*

A write to this register enables write access to the DEVICE_RESET register.

**NOTE**

WKEY register is not reset to default value on device reset (see Reset section). After coming out of device reset, write 00h to the WKEY register to prevent erroneous reset.

**Figure 30. WKEY Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | KEYWORD[3:0] | | | |
| R-0b | R-0b | R-0b | R-0b | R/W-0000b | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 6. WKEY Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R | 0000b | Reserved Bits. Do not write. Read returns 0000b |
| 3-0 | KEYWORD[3:0] | R/W | 0000b | Write 1010b into these bits to get write access for the DEVICE_RESET register. |

#### *7.5.1.2 DEVICE_RESET Register (address = 14h), [reset = 00h]*

A write to this register resets the device (see Reset section).

**NOTE**

KEYWORD[3:0] bits in the WKEY register must be programmed to 1010b to enable write into the DEVICE_RESET register.

**Figure 31. DEVICE_RESET Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | DEV_RST |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-0b |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 7. DEVICE_RESET Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R | 0000000b | Reserved Bits. Read returns 0000000b |
| 0 | DEV_RST | R/W | 0b | Writing 1 into this bit resets the device. |

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### 7.5.2 FUNCTIONAL MODE SELECT REGISTERS

These set of registers select the functional mode of the device.

#### *7.5.2.1 OFFSET_CAL Register (address = 15h), [reset = 00h]*

Write to this register initiates internal offset calibration cycle (see Offset Calibration).

**Figure 32. OFFSET_CAL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | TRIG_OFFCAL |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-0b |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 8. OFFSET_CAL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R | 0000000b | Reserved Bits. Read returns 0000000b |
| 0 | TRIG_OFFCAL | R/W | 0b | Writing 1 into this bit triggers internal offset calibration. |

#### *7.5.2.2 OPMODE_SEL Register (address = 1Ch), [reset = 00h]*

Write to this register sets the Operation Mode of the device.

**Figure 33. OPMODE_SEL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | SEL_OPMODE[2:0] | | |
| R-0b | R-0b | R-0b | R-0b | R-0b | R/W-000b | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 9. OPMODE_SEL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | 0 | R | 00000b | Reserved Bits. Read returns 00000b |
| 2-0 | SEL_OPMODE[2:0] | R/W | 000b | These bits set the functional mode for the device<br>000b = I2C Command Mode with Channel 0 (Default Sequence).<br>001b = I2C Command Mode with Channel 0 (Default Sequence).<br>010b = Reserved, Do not use.<br>011b = Reserved, Do not use.<br>100b = I2C Command Mode with Auto Sequencing enabled.<br>101b = I2C Command Mode with Auto Sequencing enabled.<br>110b = Autonomous Monitoring Mode with Auto Sequencing enabled.<br>111b = High Precision Mode with Auto Sequencing enabled. |

#### *7.5.2.3 OPMODE_I2CMODE_STATUS Register (address = 00h), [reset = 00h]*

This register provides the present operation mode and $I^2C$ mode information (Read Only).

**Figure 34. OPMODE_I2CMODE_STATUS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | HS_MODE | DEV_OPMODE[1:0] | |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-00b | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 10. OPMODE_I2CMODE_STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | 0 | R | 00000b | Reserved bits. Reads return 00000b. |
| 2 | HS_MODE | R | 0b | Indicates when device in High speed mode for $I^2C$ Interface.<br>0b = Device is not in High speed mode for $I^2C$ Interface.<br>1b = Device is in High speed mode for $I^2C$ Interface. |

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**Table 10. OPMODE_I2CMODE_STATUS Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 1-0 | DEV_OPMODE[1:0] | R | 00b | Indicates the functional mode of the device.<br>00b = Device is operating in I2C Command Mode<br>01b = Not Used<br>10b = Device is operating in Autonomous Monitoring Mode<br>11b = Device is operating in High Precision Mode |

### 7.5.3 INPUT CONFIG REGISTER

This register configures the analog input pins of the device (see Analog Input and Multiplexer).

#### *7.5.3.1 CHANNEL_INPUT_CFG Register (address = 24h), [reset = 00h]*

Write to this register configures the analog input channels. .

**Figure 35. CHANNEL_INPUT_CFG Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | CH0_CH1_IP_CFG[1:0] | |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-00b | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 11. CHANNEL_INPUT_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R | 000000b | Reserved Bits. Read returns 000000b |
| 1-0 | CH0_CH1_IP_CFG[1:0] | R/W | 00b | Selects configuration for the input pins<br>00b = Two-Channel, Single-Ended configuration<br>01b = Single-Channel, Single-Ended configuration with Remote Ground Sensing<br>10b = Single-Channel, Pseudo-Differential configuration<br>11b = Two-Channel, Single-Ended configuration |

### 7.5.4 ANALOG MUX and SEQUENCER REGISTERS

These registers configure the analog multiplexer and channel sequencing (see Channel Sequencing).

#### *7.5.4.1 AUTO_SEQ_CHEN Register (address = 20h), [reset = 03h]*

This register selects the channels that are scanned when Auto-Sequencing is enabled. By default, both channels are selected at power up.

**Figure 36. AUTO_SEQ_CHEN Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | AUTOSEQ_EN_CH1 | AUTOSEQ_EN_CH0 |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-1b | R/W-1b |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 12. AUTO_SEQ_CHEN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R | 000000b | Reserved Bits. Read returns 000000b |
| 1 | AUTO_SEQ_CH1 | R/W | 1b | 0 = Channel 1 is not selected for auto sequencing<br>1= Channel 1 is selected for auto sequencing |
| 0 | AUTO_SEQ_CH0 | R/W | 1b | 0 = Channel 0 is not selected for auto sequencing<br>1= Channel 0 is selected for auto sequencing |

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### 7.5.4.2 START_SEQUENCE Register (address = 1Eh), [reset = 00h]

A write to this register starts the channel scanning sequence.

**Figure 37. START_SEQUENCE Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | SEQ_START |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | W-0b |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 13. START_SEQUENCE Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R | 0000000b | Reserved Bits. Read returns 0000000b |
| 0 | SEQ_START | W | 0b | Setting this bit = 1 brings the BUSY/$\overline{\text{RDY}}$ pin high and starts the first conversion in the sequence |

### 7.5.4.3 ABORT_SEQUENCE Register (address = 1Fh), [reset = 00h]

A write to this register aborts the channel scanning sequence. Once sequence is aborted using this register, it is recommended to read the status registers to know the last status of the device and then read the output data.

**Figure 38. ABORT_SEQUENCE Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | SEQ_ABORT |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | W-0b |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 14. ABORT_SEQUENCE Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R | 0000000b | Reserved Bits. Read returns 0000000b |
| 0 | SEQ_ABORT | W | 0b | Setting this bit = 1 aborts the ongoing conversion and brings the BUSY/$\overline{\text{RDY}}$ pin low |

### 7.5.4.4 SEQUENCE_STATUS Register (address = 04h), [reset = 00h]

Provides the status of sequence in device (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

**Figure 39. SEQUENCE_STATUS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | SEQ_ERR_ST[1:0] | | 0 |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-00b | | R-0b |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 15. SEQUENCE_STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | 0 | R | 00000b | Reserved bits. Reads return 00000b. |
| 2-1 | SEQ_ERR_ST[1:0] | R | 00b | Status of device sequence<br>00b = Auto Sequencing disabled, no error.<br>01b = Auto Sequencing enabled, no error.<br>10b = Not used<br>11b = Auto Sequencing enabled, device in error. |
| 0 | 0 | R | 0b | Reserved bit. Reads return 0. |

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### 7.5.5 OSCILLATOR and TIMING CONTROL REGISTERS

These registers select the oscillator used for the conversion process and cycle time for a single conversion (see Oscillator and Timing Control section).

#### *7.5.5.1 OSC_SEL Register (address = 18h), [reset = 00h]*

A write to this register selects the oscillator used for the conversion process.

**Figure 40. OSC_SEL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | HSZ_LP |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-0b |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 16. OSC_SEL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R | 0000000b | Reserved Bits. Read returns 0000000b |
| 0 | HSZ_LP | R/W | 0b | 0b = Device uses High Speed Oscillator<br>1b = Device uses Low Power Oscillator |

#### *7.5.5.2 nCLK_SEL Register (address = 19h), [reset = 00h]*

This register controls the cycle time for a single conversion by setting the nCLK parameter. nCLK is the number of clocks of the selected oscillator that the device uses for one conversion cycle.

**Figure 41. nCLK_SEL Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| nCLK[7:0] | | | | | | | |
| R/W-00000000b | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

**Table 17. nCLK_SEL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | nCLK[7:0] | R/W | 00000000b | Sets number of clocks of the oscillator that the device uses for one conversion cycle.<br>When using the High Speed Oscillator:<br>• 00000000b to 00010101b = nCLK is set to 21<br>• 00010110b = nCLK is set to 22<br>• 00010111b = nCLK is set to 23 and so on till<br>• 11111111b = nCLK is set to 255<br>When using the Low Power Oscillator:<br>• 00000000b to 00010010b = nCLK is set to 18<br>• 00010011b = nCLK is set to 19<br>• 00010100b = nCLK is set to 20 and so on till<br>• 11111111b = nCLK is set to 255 |

### 7.5.6 DATA BUFFER CONTROL REGISTER

This register controls the operation of the Data Buffer (see Data Buffer section).

#### *7.5.6.1 DATA_BUFFER_OPMODE Register (address = 2Ch), [reset = 01h]*

A write to this register selects the operation mode of the Data Buffer.

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**Figure 42. DATA_BUFFER_OPMODE Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | STARTSTOP_CNTRL[2:0] | | |
| R-0b | R-0b | R-0b | R-0b | R-0b | R/W-001b | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 18. DATA_BUFFER_OPMODE Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | 0 | R | 00000b | Reserved Bits. Read returns 00000b |
| 2-0 | STARTSTOP_CNTRL [2:0] | R/W | 001b | 000b = Stop Burst Mode<br>001b = Start Burst Mode, default<br>010b = Reserved, do not use<br>011b = Reserved, do not use<br>100b = Pre Alert Data Mode<br>101b = Reserved, do not use<br>110b = Post Alert Data Mode<br>111b = Reserved, do not use |

### *7.5.6.2 DOUT_FORMAT_CFG Register (address = 28h), [reset = 00h]*

This register controls the 16-bit contents of the data word in the data buffer.

**Figure 43. DOUT_FORMAT_CFG Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | DOUT_FORMAT[1:0] | |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-00b | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 19. DOUT_FORMAT_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R | 000000b | Reserved Bits. Read returns 000000b |
| 1-0 | DOUT_FORMAT[1:0] | R/W | 00b | 00b = 12-bit conversion result followed by 0000b<br>01b = 12-bit conversion result followed by 3-bit Channel ID (000b for CH0, 001b for CH1)<br>10b = 12-bit conversion result followed by 3-bit Channel ID (000b for CH0, 001b for CH1) followed by DATA_VALID bit<br>11b = 12-bit conversion result followed by 0000b |

### *7.5.6.3 DATA_BUFFER_STATUS Register (address = 01h), [reset = 00h]*

Provides the present status of Data Buffer (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

**Figure 44. DATA_BUFFER_STATUS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | DATA_WORDCOUNT[4:0] | | | | |
| R-0b | R-0b | R-0b | R-00000b | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 20. DATA_BUFFER_STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | R | 000b | Reserved Bits. Read returns 000b |
| 4-0 | DATA_WORDCOUNT [4:0] | R | 00000b | DATA_WORDCOUNT [00000] to [10000] = Number of entries filled in data buffer (0 to 16) |

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### 7.5.7 ACCUMULATOR CONTROL REGISTERS

These registers control the operation of the Accumulator (see Accumulator section).

#### *7.5.7.1 ACC_EN Register (address = 30h), [reset = 00h]*

This register enables the accumulator.

**Figure 45. ACC_EN Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | EN_ACC[3:0] | | | |
| R-0b | R-0b | R-0b | R-0b | R/W-0000b | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 21. ACC_EN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R | 0000b | Reserved Bits. Read returns 0000b |
| 3-0 | EN_ACC[3:0] | R/W | 0000b | 0000b = Accumulator is disabled<br>0001b to 1110b = Reserved, do not use<br>1111b = Accumulator is enabled |

#### *7.5.7.2 ACC_CH0_LSB Register (address = 08h), [reset = 00h]*

Provides the LSB of accumulated data for CH0 (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

**Figure 46. ACC_CH0_LSB Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CH0_LSB[7:0] | | | | | | | |
| R-00000000b | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

**Table 22. ACC_CH0_LSB Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | CH0_LSB[7:0] | R | 00000000b | LSB of accumulated data for CH0 |

#### *7.5.7.3 ACC_CH0_MSB Register (address = 09h), [reset = 00h]*

Provides the MSB of accumulated data for CH0 (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

**Figure 47. ACC_CH0_MSB Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CH0_MSB[7:0] | | | | | | | |
| R-00000000b | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

**Table 23. ACC_CH0_MSB Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | CH0_MSB[7:0] | R | 00000000b | MSB of accumulated data for CH0 |

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#### 7.5.7.4 ACC_CH1_LSB Register (address = 0Ah), [reset = 00h]

Provides the LSB of accumulated data for CH1 (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

**Figure 48. ACC_CH1 LSB Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CH1_LSB[7:0] | | | | | | | |
| R-00000000b | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Table 24. ACC_CH1 LSB Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | CH1_LSB[7:0] | R | 00000000b | LSB of accumulated data for CH1 |

#### 7.5.7.5 ACC_CH1_MSB Register (address = 0Bh), [reset = 00h]

Provides the MSB of accumulated data for CH1 (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

**Figure 49. ACC_CH1 MSB Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CH1_MSB[7:0] | | | | | | | |
| R-00000000b | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

**Table 25. ACC_CH1 MSB Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | CH1_MSB[7:0] | R | 00000000b | MSB of accumulated data for CH1 |

#### 7.5.7.6 ACCUMULATOR_STATUS Register (address = 02h), [reset = 00h]

Provides the present status of Accumulator (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

**Figure 50. ACCUMULATOR_STATUS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | ACC_COUNT[3:0] | | | |
| R-0b | R-0b | R-0b | R-0b | R-0000b | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 26. ACCUMULATOR_STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R | 0000b | Reserved Bits. Read returns 0000b |
| 3-0 | ACC_COUNT[3:0] | R | 0000b | ACC_COUNT = Number of accumulation completed till last finished conversion. |

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### 7.5.8 DIGITAL WINDOW COMPARATOR REGISTERS

These registers control the operation of the Digital Window Comparator (see Digital Window Comparator section).

#### *7.5.8.1 ALERT_DWC_EN Register (address = 37h), [reset = 00h]*

Write to this register enables the Alert and Digital Window Comparator block.

**Figure 51. ALERT_DWC_EN Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | DWC_BLOCK_EN |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-0b |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 27. ALERT_DWC_EN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R | 0000000b | Reserved Bits. Read returns 0000000b |
| 0 | DWC_BLOCK_EN | R/W | 0b | 0 = Disables Digital Window Comparator<br>1 = Enables Digital Window Comparator |

#### *7.5.8.2 ALERT_CHEN (address = 34h), [reset = 03h]*

This register enables Alert functionality for individual channels.

**Figure 52. ALERT_CHEN Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | ALERT_EN_CH1 | ALERT_EN_CH0 |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-1b | R/W-1b |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 28. ALERT_CHEN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R | 000000b | Reserved Bits. Read returns 000000b |
| 1 | ALERT_EN_CH1 | R/W | 1b | Enables alert functionality for CH1<br>0b = Alert is disabled for CH1<br>1b = Alert is enabled for CH1, default |
| 0 | ALERT_EN_CH0 | R/W | 1b | Enables alert functionality for CH0<br>0b = Alert is disabled for CH0<br>1b = Alert is enabled for CH0, default |

#### *7.5.8.3 DWC_HTH_CH0_MSB Register (address = 39h), [reset = 0Fh]*

This register sets the four most significant bits of high threshold for CH0.

**Figure 53. DWC_HTH_CH0_MSB Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | HTH_CH0_MSB[3:0] | | | |
| R-0b | R-0b | R-0b | R-0b | R/W-1111b | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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**Table 29. DWC_HTH_CH0_LSB Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R | 0000b | Reserved Bits. Read returns 0000b |
| 3-0 | HTH_CH0_MSB[3:0] | R/W | 1111b | 4 most significant bits of high threshold for CH0 |

### *7.5.8.4 DWC_HTH_CH0_LSB Register (address = 38h), [reset = FFh]*

This register sets the eight least significant bits of high threshold for CH0.

**Figure 54. DWC_HTH_CH0_LSB Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| HTH_CH0_LSB[7:0] | | | | | | | |
| R/W-11111111b | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

**Table 30. DWC_HTH_CH0_LSB Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | HTH_CH0_LSB[7:0] | R/W | 11111111b | 8 least significant bits of high threshold for CH0 |

### *7.5.8.5 DWC_LTH_CH0_MSB Register (address = 3Bh), [reset = 00h]*

This register sets the four most significant bits of low threshold for CH0.

**Figure 55. DWC_LTH_CH0_MSB Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | LTH_CH0_MSB[3:0] | | | |
| R-0b | R-0b | R-0b | R-0b | R/W-0000b | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 31. DWC_LTH_CH0_MSB Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R | 0000b | Reserved Bits. Read returns 0000b |
| 3-0 | LTH_CH0_MSB[3:0] | R/W | 0000b | 4 most significant bits of low threshold for CH0 |

### *7.5.8.6 DWC_LTH_CH0_LSB Register (address = 3Ah), [reset = 00h]*

This register sets the eight least significant bits of low threshold for CH0.

**Figure 56. DWC_LTH_CH0_LSB Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LTH_CH0_LSB[7:0] | | | | | | | |
| R/W-00000000b | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

**Table 32. DWC_LTH_CH0_LSB Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | LTH_CH0_LSB[7:0] | R/W | 00000000b | 8 least significant bits of low threshold for CH0 |

### *7.5.8.7 DWC_HYS_CH0 (address = 40h), [reset = 00h]*

This register sets the hysteresis for both comparators for CH0.

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**Figure 57. DWC_HYS_CH0 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | HYS_CH0[5:0] | | | | | |
| R-0b | R-0b | R/W-000000b | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 33. DWC_HYS_CH0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 0 | R | 00b | Reserved Bits. Read returns 0000000b |
| 5-0 | HYS_CH0[5:0] | R/W | 000000b | Hysteresis for both comparators for CH0 |

### *7.5.8.8 DWC_HTH_CH1_MSB Register (address = 3Dh), [reset = 0Fh]*

This register sets the four most significant bits of high threshold for CH1.

**Figure 58. DWC_HTH_CH1_MSB Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | HTH_CH1_MSB[3:0] | | | |
| R-0b | R-0b | R-0b | R-0b | R/W-1111b | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 34. DWC_HTH_CH1_LSB Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R | 0000b | Reserved Bits. Read returns 0000b |
| 3-0 | HTH_CH1_MSB[3:0] | R/W | 1111b | 4 most significant bits of high threshold for CH1 |

### *7.5.8.9 DWC_HTH_CH1_LSB Register (address = 3Ch), [reset = FFh]*

This register sets the eight least significant bits of high threshold for CH1.

**Figure 59. DWC_HTH_CH1_LSB Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| HTH_CH1_LSB[7:0] | | | | | | | |
| R/W-11111111b | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

**Table 35. DWC_HTH_CH1_LSB Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | HTH_CH1_LSB[7:0] | R/W | 11111111b | 8 least significant bits of high threshold for CH1 |

### *7.5.8.10 DWC_LTH_CH1_MSB Register (address = 3Fh), [reset = 00h]*

This register sets the four most significant bits of low threshold for CH1.

**Figure 60. DWC_LTH_CH1_MSB Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | LTH_CH1_MSB[3:0] | | | |
| R-0b | R-0b | R-0b | R-0b | R/W-0000b | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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**Table 36. DWC_LTH_CH1_MSB Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R | 0000b | Reserved Bits. Read returns 0000b |
| 3-0 | LTH_CH1_MSB[3:0] | R/W | 0000b | 4 most significant bits of low threshold for CH1 |

### *7.5.8.11 DWC_LTH_CH1_LSB Register (address = 3Eh), [reset = 00h]*

This register sets the eight least significant bits of low threshold for CH1.

**Figure 61. DWC_LTH_CH1_LSB Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LTH_CH1_LSB[7:0] | | | | | | | |
| R/W-00000000b | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

**Table 37. DWC_LTH_CH1_LSB Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | LTH_CH1_LSB[7:0] | R/W | 00000000b | 8 least significant bits of low threshold for CH1 |

### *7.5.8.12 DWC_HYS_CH1 (address = 41h), [reset = 00h]*

This register sets the hysteresis for both comparators for CH1.

**Figure 62. DWC_HYS_CH1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | HYS_CH1[5:0] | | | | | |
| R-0b | R-0b | R/W-000000b | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 38. DWC_HYS_CH1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 0 | R | 00b | Reserved Bits. Read returns 0000000b |
| 5-0 | HYS_CH1[5:0] | R/W | 000000b | Hysteresis for both comparators for CH1 |

### *7.5.8.13 PRE_ALERT_EVENT_COUNT Register (address = 36h), [reset = 00h]*

This register sets the Pre-Alert Event Count for both, high and low comparators, for both the channels.

**Figure 63. PRE_ALERT_EVENT_COUNT Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PREALERT_COUNT[3:0] | | | | 0 | 0 | 0 | 0 |
| R/W-0000b | | | | R-0b | R-0b | R-0b | R-0b |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 39. PRE_ALERT_EVENT_COUNT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | PREALERT_COUNT[3:0] | R/W | 0000b | Sets the Pre-Alert Event Count = PREALERT_COUNT[3:0] + 1 |
| 3-0 | 0 | R | 0000b | Reserved Bits. Read returns 0000b |

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### 7.5.8.14 ALERT_TRIG_CHID Register (address = 03h), [reset = 00h]

Provides the channel ID of channel which was first to set the alert output (Read Only).

This register is cleared at power-up, on receiving general call reset, on device reset or when SEQ_START bit in START_SEQUENCE register is set to 1.

**Figure 64. ALERT_TRIG_CHID Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ALERT_TRIG_CHID[3:0] | | | | 0 | 0 | 0 | 0 |
| R-0000b | | | | R-0b | R-0b | R-0b | R-0b |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 40. ALERT_TRIG_CHID Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | ALERT_TRIG_CHID[3:0] | R | 0000b | Provides the channel ID of channel which was first to set the alert output<br>0000b = Channel 0<br>0001b = Channel 1<br>0010b to 1111b = Not used |
| 3-0 | 0 | R | 0000b | Reserved bits. Reads return 0000b. |

### 7.5.8.15 ALERT_LOW_FLAGS Register (address = 0C), [reset = 00h]

This register provides the status of latched flags for low alert. All flags are cleared at power up, on general call reset (General Call with Software Reset ), or by writing FFh to this register. To clear individual alert flag, write 1 to the corresponding bit location.

**Figure 65. ALERT_LOW_FLAGS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | ALERT_LOW_CH1 | ALERT_LOW_CH0 |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-0b | R/W-0b |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 41. ALERT_LOW_FLAGS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R | 000000b | Reserved Bits. Read returns 000000b |
| 1 | ALERT_LOW_CH1 | R/W | 0b | Indicates alert on low side comparator for CH1<br>0b = Alert is not set for low side comparator for CH1<br>1b = Alert is set for low side comparator for CH1. |
| 0 | ALERT_LOW_CH0 | R/W | 0b | Indicates alert on low side comparator for CH0<br>0b = Alert is not set for low side comparator for CH0<br>1b = Alert is set for low side comparator for CH0. |

### 7.5.8.16 ALERT_HIGH_FLAGS Register (address = 0Eh), [reset = 00h]

This register provides the status of latched flags for high alert. All flags are cleared at power up, on general call reset (General Call with Software Reset ), or by writing FFh to this register. To clear individual alert flag, write 1 to the corresponding bit location.

**Figure 66. ALERT_HIGH_FLAGS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | ALERT_HIGH_CH1 | ALERT_HIGH_CH0 |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R/W-0b | R/W-0b |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

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**Table 42. ALERT_HIGH_FLAGS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R | 000000b | Reserved Bits. Read returns 000000b |
| 1 | ALERT_HIGH_CH1 | R/W | 0b | Indicates alert on high side comparator for CH1<br>0b = Alert is not set for high side comparator for CH1<br>1b = Alert is set for high side comparator for CH1. |
| 0 | ALERT_HIGH_CH0 | R/W | 0b | Indicates alert on high side comparator for CH0<br>0b = Alert is not set for high side comparator for CH0<br>1b = Alert is set for high side comparator for CH0. |

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

In an increasing number of industrial applications, data acquisition sub-systems are collecting more data about the environment in which the system is operating and applying deep learning algorithms in order to improve system reliability, implement preventative maintenance, and/or enhance the quality of data collected by the system. The ADS7142 can be used to connect to a variety of sensors and can provide deeper data analytics at lower power levels than existing solutions. The depth of analysis that can be performed on the data collected by the ADS7142 is enhanced by the internal data buffer, programmable alarm thresholds and hysteresis, event counter, and internal calibration circuitry. The applications circuits described in this section highlight specific use-cases of the ADS7142 for data collection that can further increase the depth and quality of the data being measured by the system.

## 8.2 Typical Applications

### 8.2.1 ADS7142 as a Programmable Comparator with False Trigger Prevention and Diagnostics

#### *8.2.1.1 Design Requirements*

In many applications such as industrial alarms, sensor monitors, and level sensors there is a need to make a decision at the system-level when the input signal crosses a predefined threshold. Analog window comparators are being used extensively in such applications.

An analog window comparator has a set of comparators. The external input signal is connected to the inverting terminal of one comparator and the noninverting terminal of the other comparator. The remaining input of each comparator is connected to the internal reference. The outputs are tied together and are often connected to a reset or general-purpose input of a processor (such as a digital signal processor, field-programmable gate array, or application-specific integrated circuit) or the enable input of a voltage regulator (such as a DC-DC or low-dropout regulator). Figure 67 shows the circuit diagram for an analog window comparator.

Though analog comparators are easy to design, there are certain disadvantages associated with analog comparators.

- Higher Power Consumption: If the voltage that is monitored is greater than the window comparator supply voltage, then there is a need for a resistive divider ladder to scale down that voltage. This resistive ladder draws a constant current and adds to the power consumption of the system. In battery powered applications, this becomes a challenge and can adversely affect the battery life.
- Fixed Threshold Voltages: The window comparator thresholds cannot be changed on-the-fly since these are set by hardware (typically with a resistive ladder). This may add a limitation if user wants to change the comparator thresholds during operation without switching in a new resistor ladder.

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## Typical Applications (continued)

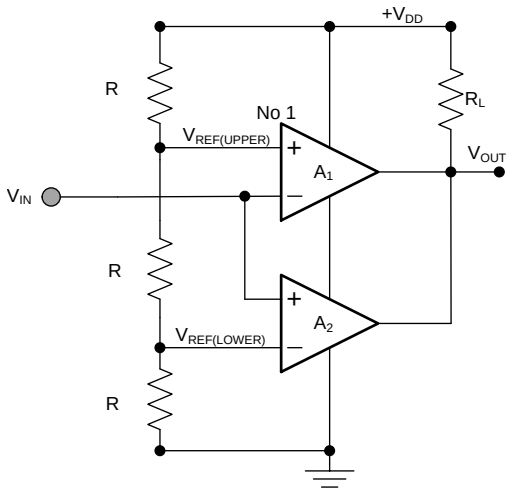





**Figure 67. Analog Window Comparator**

Many applications in the field of preventive maintenance, building automation, and Internet of Things (IoT) require a sensor monitor which operates autonomously and gives an alert/interrupt to the host MCU only when the sensor output crosses a predefined, programmable threshold. Typically battery-operated, wireless sensor nodes like smoke detectors, temperature monitors, ambient light sensors, proximity sensors and gas sensors fall under this category. The ADS7142 is an excellent fit for such sensor monitoring systems due to its ability to autonomously monitor sensor output and wake up the host controller whenever the sensor output crosses pre-defined thresholds. Additionally, the ADS7142 has an internal data buffer which can store 16 sample data which the user can read in case further analysis is required. Figure 68 shows typical block diagram of ADS7142 as sensor monitor. As is shown in this figure, the sensor can be connected directly to the input of the ADC (depending on the sensor output signal characteristics).

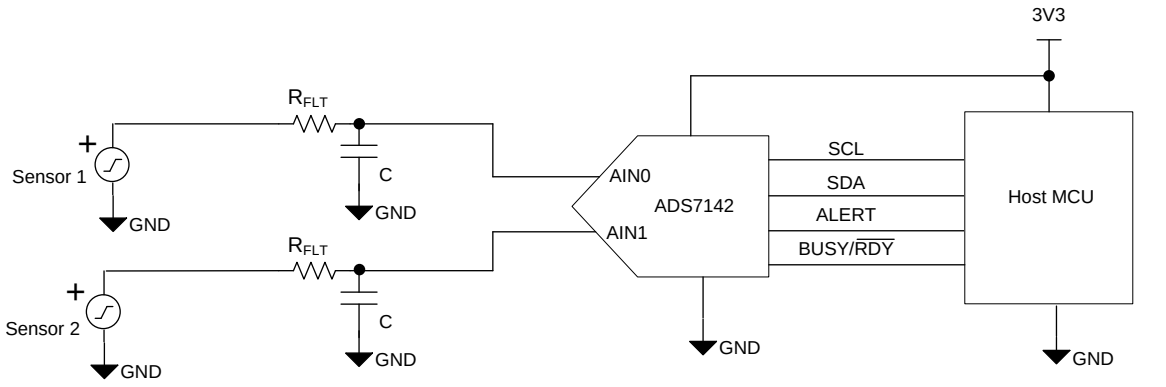





**Figure 68. Sensor Monitor Circuit with ADS7142**

### *8.2.1.2 Detailed Design Procedure*

#### 8.2.1.2.1 Programmable Thresholds and Hysteresis

The ADS7142 can be programmed to monitor sensor output voltages and generate an ALERT signal for the host controller if the sensor output voltage crosses a threshold.

## Typical Applications (continued)

The device can be configured to monitor for signals rising above a programmed threshold. Figure 69 illustrates the operation of the device when monitoring for signal crossings on the low threshold by setting the high threshold to 0xFFF. In this case, the output of the low-side comparator is set whenever the ADC conversion result is less than or equal to the low threshold, and the output of the high-side comparator is only set when the ADC conversion result is equal to 0xFFF.

The device can also be configured to monitor for signals falling below a programmed threshold. Figure 70 illustrates the operation of the device when monitoring for signal crossings on the high threshold by setting the low threshold to 0x000. In this case, the output of high-side comparator is set whenever the ADC conversion result is greater than or equal to the high threshold and the output of the low-side comparator will only be set when the ADC conversion result is equal to 0x000.

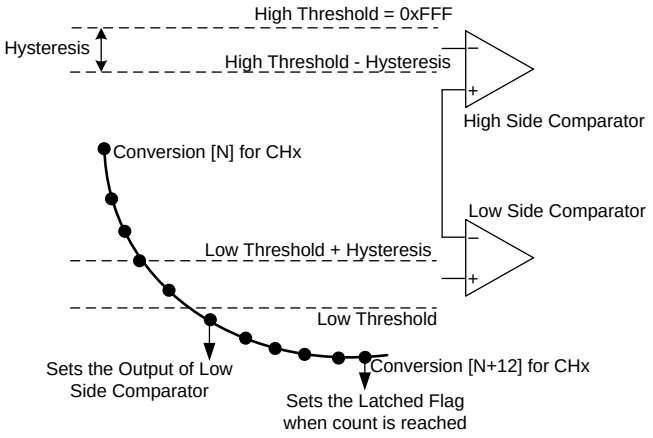



**Figure 69. Low Alert with ADS7142**

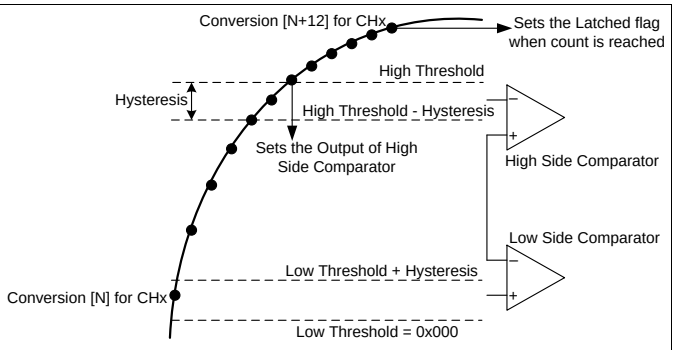



**Figure 70. High Alert with ADS7142**

The device can also be configured to monitor for signals falling outside of a programmed window. Figure 71 illustrates the operation of the device for an out-of-range alert where the signal leaves the pre-defined window and crosses either the high or low threshold. In this case, the output of low side comparator is set whenever the ADC conversion result is less than or equal to the low threshold, and the output of high side comparator is set when the ADC conversion result is greater than or equal to the high threshold.

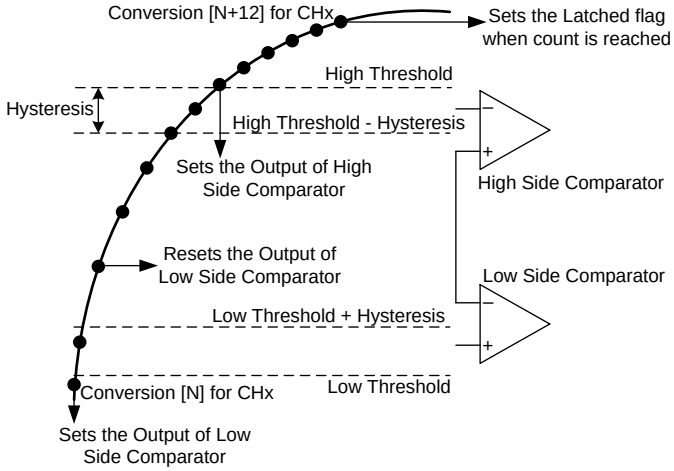



**Figure 71. Out of Range Alert with ADS7142**

#### 8.2.1.2.2 False Trigger Prevention with Event Counter

The Pre-Alert event counter in the *Digital Window Comparator* helps to prevent false triggers. The alert output is not set until the output of the comparator remains set for a pre-defined number (count) of consecutive conversions.

ADVANCE INFORMATION

## Typical Applications (continued)

#### 8.2.1.2.3 Fault Diagnostics with Data Buffer

The modes which are specifically designed for autonomous sensor monitor applications are Pre-Alert mode and Post-Alert mode. In Pre-Alert mode, the ADS7142 can be configured to monitor sensor outputs and continuously fill the internal data buffer until a threshold crossing occurs. The ADS7142 will generate an ALERT signal when the sensor output falls outside of the predefined window of operation. In this particular mode, the ADS7142 stops filling the data buffer when the threshold is crossed and provides the last 16 samples (15 sample data preceding the sample at which the ALERT is generated and 1 sample data for which the ALERT is generated). Figure 72 shows the ADS7142 operation in Pre-Alert mode showing 16 data samples before the sensor output crosses the low threshold. This is useful for applications where the state of the signal before the threshold is crossed is important to capture. Using the data captured before the alert, deep data analysis can be performed to determine the state of the system before the alert. This type of data is not available with analog comparators.

In Post-Alert mode, ADS7142 can be configured to monitor sensor outputs and start filling the internal data buffer after a threshold crossing occurs. The ADS7142 generates an ALERT signal when the sensor output falls outside of the predefined window of operation. In this particular mode, the ADS7142 continues to fill the data buffer after the threshold is crossed for a total of 16 samples (1 sample data for which ALERT is generated and 15 sample data after the sample at which ALERT is generated). Figure 73 shows the ADS7142 operation in Post-Alert mode showing 16 data samples after the sensor output crosses the high threshold. This is useful for applications where the state of the signal after the threshold is crossed is important to capture. Using the data captured after the alert, deep data analysis can be performed for to determine the state of the system after the alert to detect system-level events such as saturation. This data is not available with analog comparators.

## Typical Applications (continued)

### 8.2.1.3 Application Curve


**Figure 72. Pre-Alert Data Capture**


**Figure 73. Post Alert Data Capture**

ADVANCE INFORMATION

## Typical Applications (continued)

### 8.2.2 Event-triggered PIR sensing with ADS7142

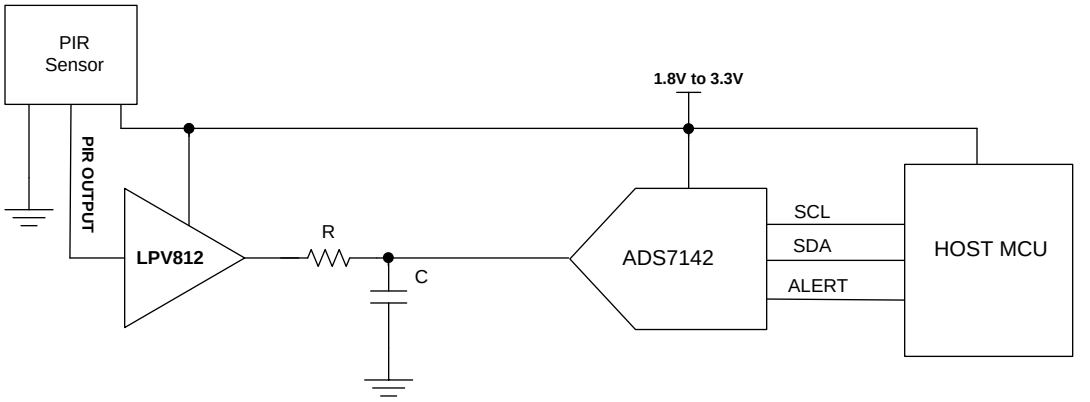





**Figure 74. PIR Sensor with ADS7142**

#### *8.2.2.1 Design Requirements*

A passive infrared (PIR) sensor is a commonly used sensor to detect motion by measuring infrared light emitted from any object that generates heat. PIR sensors are small, inexpensive, low-power, rugged, have a wide lens range, and are easy to use. PIR sensors are commonly used in security lighting and alarm systems used in indoor environments. When there is no motion or heat-emitting object in the vicinity of the sensor, the PIR sensor output is a DC voltage which is typically specified in the PIR datasheet. When a source of heat, such as a person or animal, comes into the sensor's field of view, then the PIR sensor output changes. The amplitude of this signal is proportional to the speed and distance of the object relative to the sensor and is in the range of millivolts peak-to-peak. PIR sensors are often followed by a signal conditioning stage which amplifies the IR sensor output. A PIR sensor can be interfaced with the ADS7142 to make an ultra-low-power, autonomous PIR motion detector. The Autonomous Mode of the ADS7142 with threshold monitoring enables the system to put the host MCU into a low-power sleep mode and wake up the MCU only when motion is detected by the PIR sensor. Figure 74 shows a typical block diagram for an autonomous PIR motion detector using the ADS7142.

#### *8.2.2.2 Detailed Design Procedure*

The analog signal conditioning circuit is shown in the schematic in Figure 75. The first stage of the amplifier filter acts as a bandpass filter while the second stage applies an inverting gain. Components R10 and C5 serve as a low-pass filter to stabilize the supply voltage at the input to the sensor. Resistor R5 sets the bias current in the JFET output transistor of the PIR motion sensor. To save power, R5 is larger than recommended and essentially current starves the sensor. This comes at the expense of decreased sensitivity and higher output noise at the sensor output, which is a fair tradeoff for increased battery lifetime. Some of the loss in sensitivity at the sensor output can be compensated by a gain increase in the filter stages. Stage 1 of Figure 75 is arranged as a non-inverting gain filter stage. This provides a high-impedance load to the sensor so its bias point remains fixed. Because this stage has an effective DC gain of one due to C2, the sensor output bias voltage provides the DC bias for the first filter stage. Feedback diodes D1 and D2 provide clamping so that the op amps in both filter stages stay out of saturation for motion events which are close to the sensor. Stage 1 has a low and high cutoff frequency of 0.7 Hz and 10.6 Hz respectively and a gain of 220. Stage 2 is arranged as an inverting summer gain stage and is AC-coupled to Stage 1. A DC bias of VCC/2 is connected to the non-inverting input of the amplifier in this stage. Due to the higher gain in the filter stages and higher output noise from the sensor, care must be taken to optimize the placement of the high-frequency filter pole and the window comparator thresholds to avoid false detection.

## Typical Applications (continued)

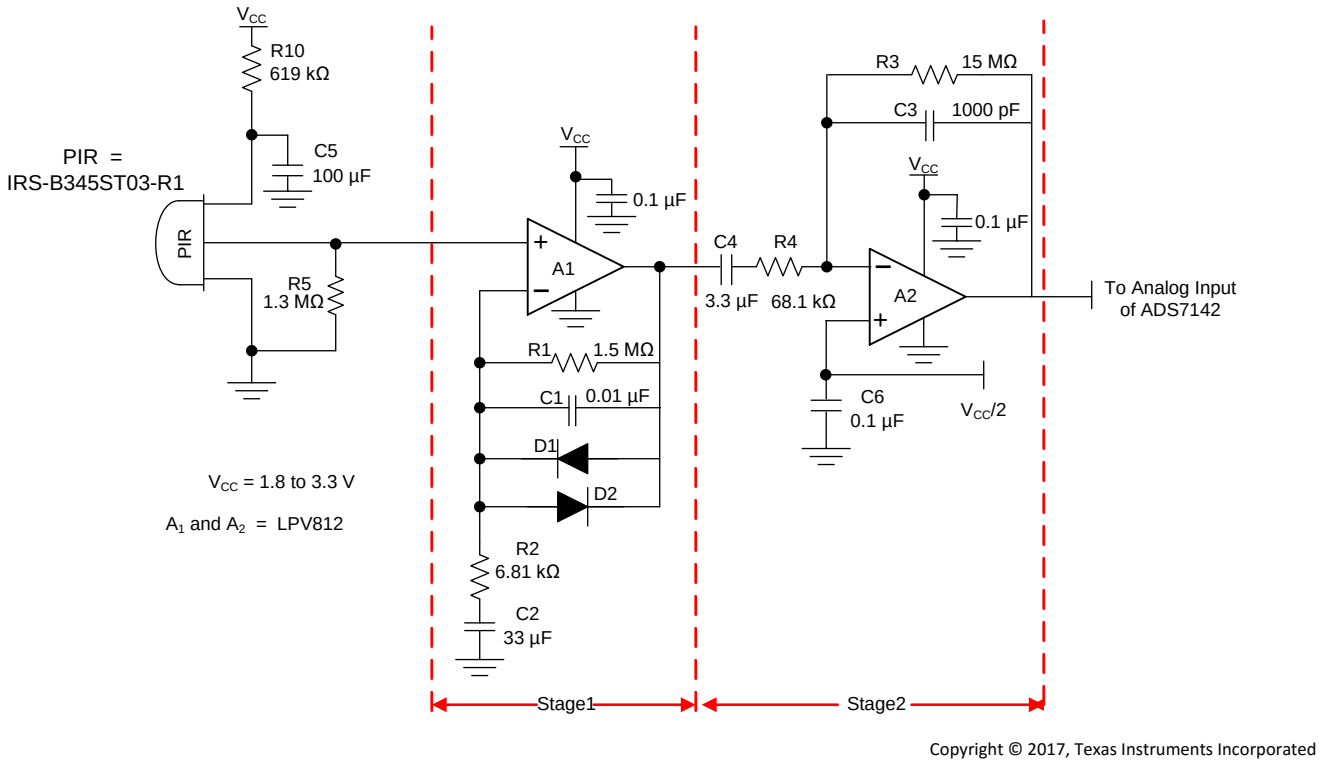



**Figure 75. Signal Conditioning Circuit for PIR Sensor**

ADVANCE INFORMATION

## Typical Applications (continued)

### 8.2.2.3 Application Curves

When the PIR sensor detects motion, its output crosses the threshold and is detected by the ADS7142 as shown on Channel 1 in Figure 76.

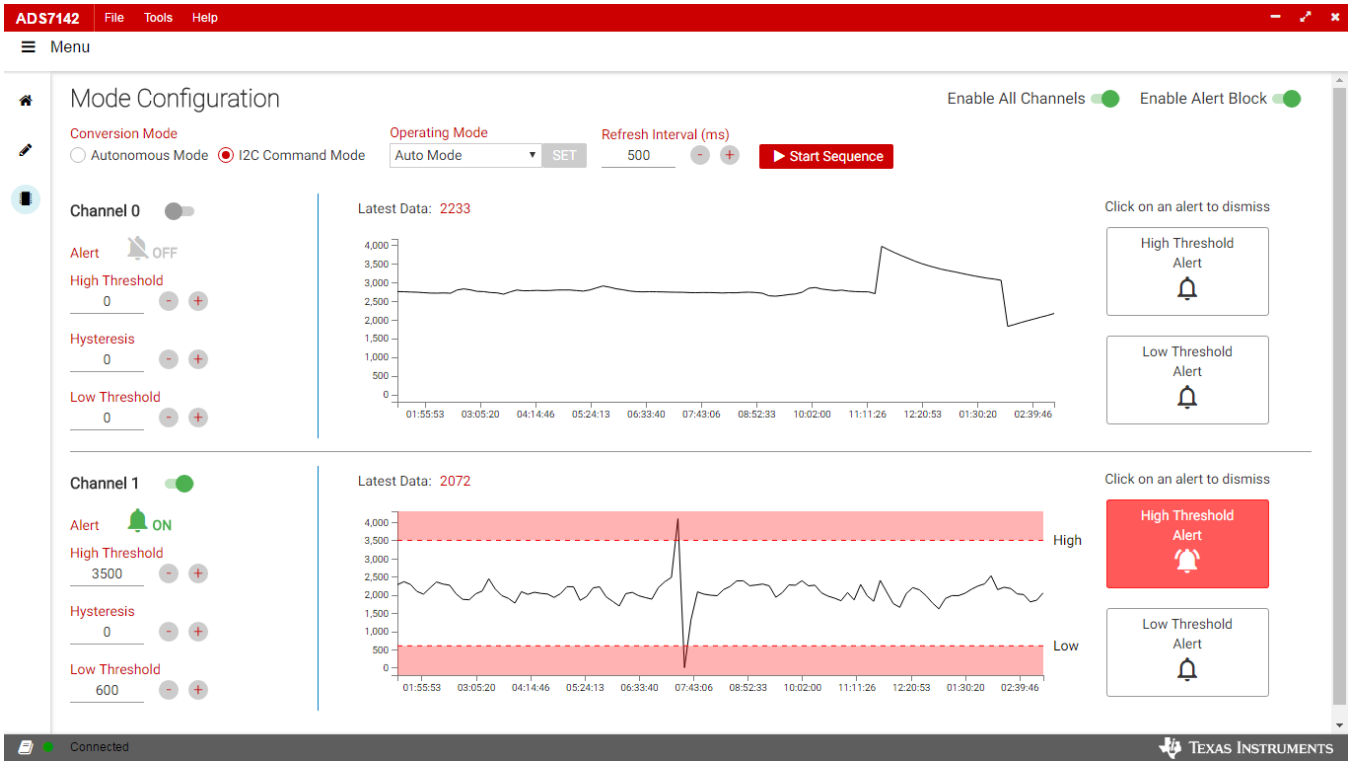



**Figure 76. Alert Output from ADS7142 with PIR Sensor**

ADVANCE INFORMATION

# 9 Power-Supply Recommendations

## 9.1 AVDD and DVDD Supply Recommendations

The ADS7142 has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges. The AVDD supply also defines the full-scale input range of the device. Always set the AVDD supply to be greater than or equal to the maximum input signal to avoid saturation of codes. Decouple the AVDD and DVDD pins respectively with 220-nF and 100-nF ceramic decoupling capacitors, as shown in Figure 77 .

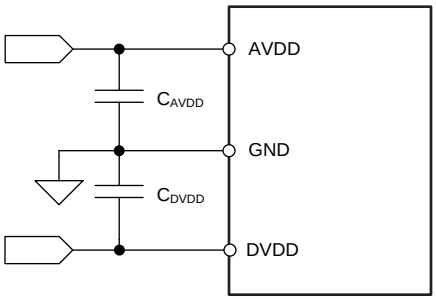





**Figure 77. Power-Supply Decoupling**

# 10 Layout

## 10.1 Layout Guidelines

Figure 78 shows a board layout example for the ADS7142. The key considerations for layout are:

- Use a solid ground plane underneath the device and partition the PCB into analog and digital sections.
- Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources.
- The power sources to the device must be clean and well-bypassed. Use $C_{AVDD}$ decoupling capacitors in close proximity to the analog (AVDD) power supply pin.
- Use a $C_{DVDD}$ decoupling capacitor close to the digital (DVDD) power-supply pin.
- Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors.
- Connect the ground pin to the ground plane using a short, low-impedance path.
- Place the charge kickback filter components close to the device.

Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors are recommended because these components provide the most stable electrical properties over voltage, frequency, and temperature changes.

## 10.2 Layout Example

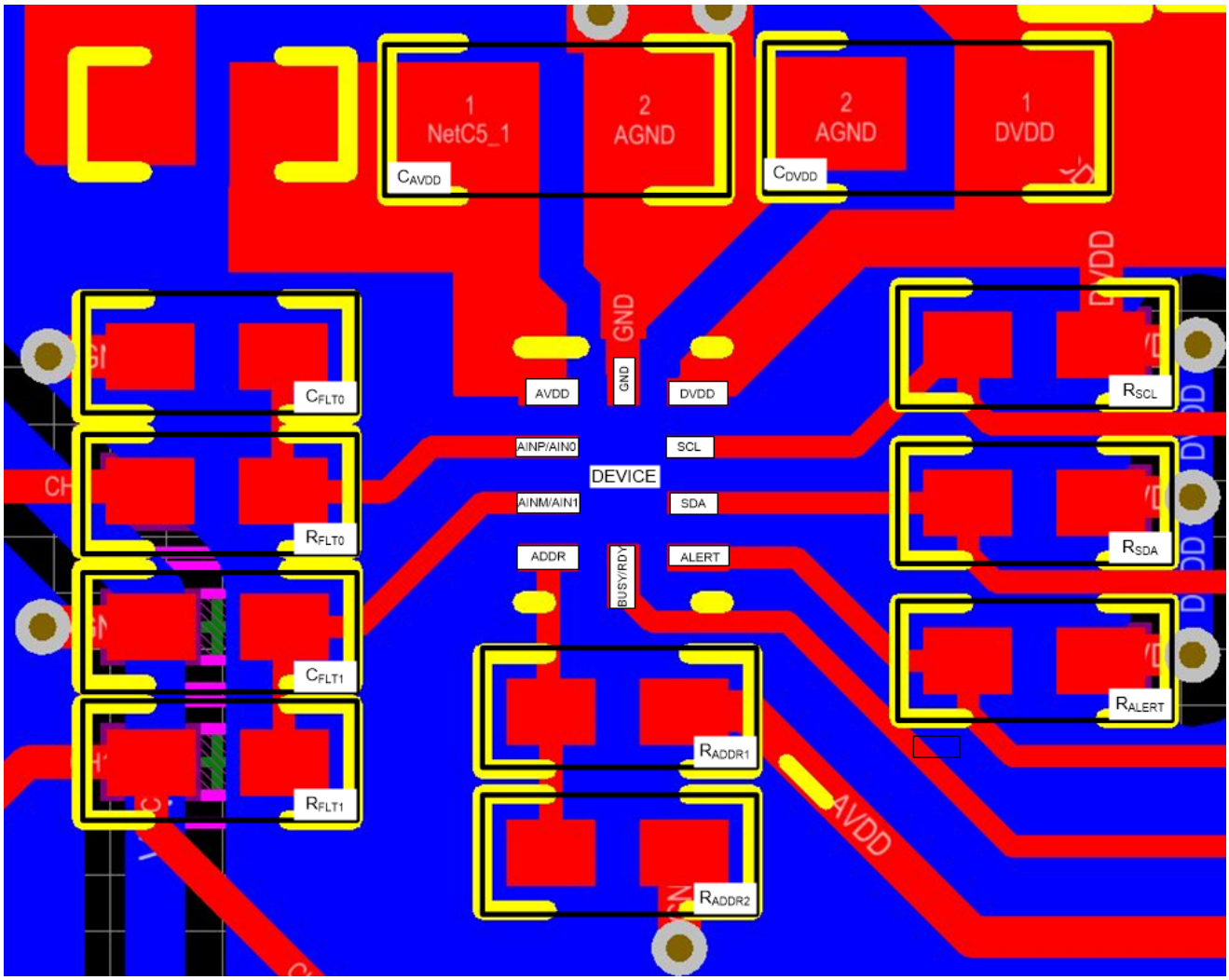



**Figure 78. Example Layout**

# 11 Device and Documentation Support

## 11.1 Documentation Support

## 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

## 11.4 Trademarks

E2E is a trademark of Texas Instruments.

## 11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| XADS7142IRUGR | ACTIVE | X2QFN | RUG | 10 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

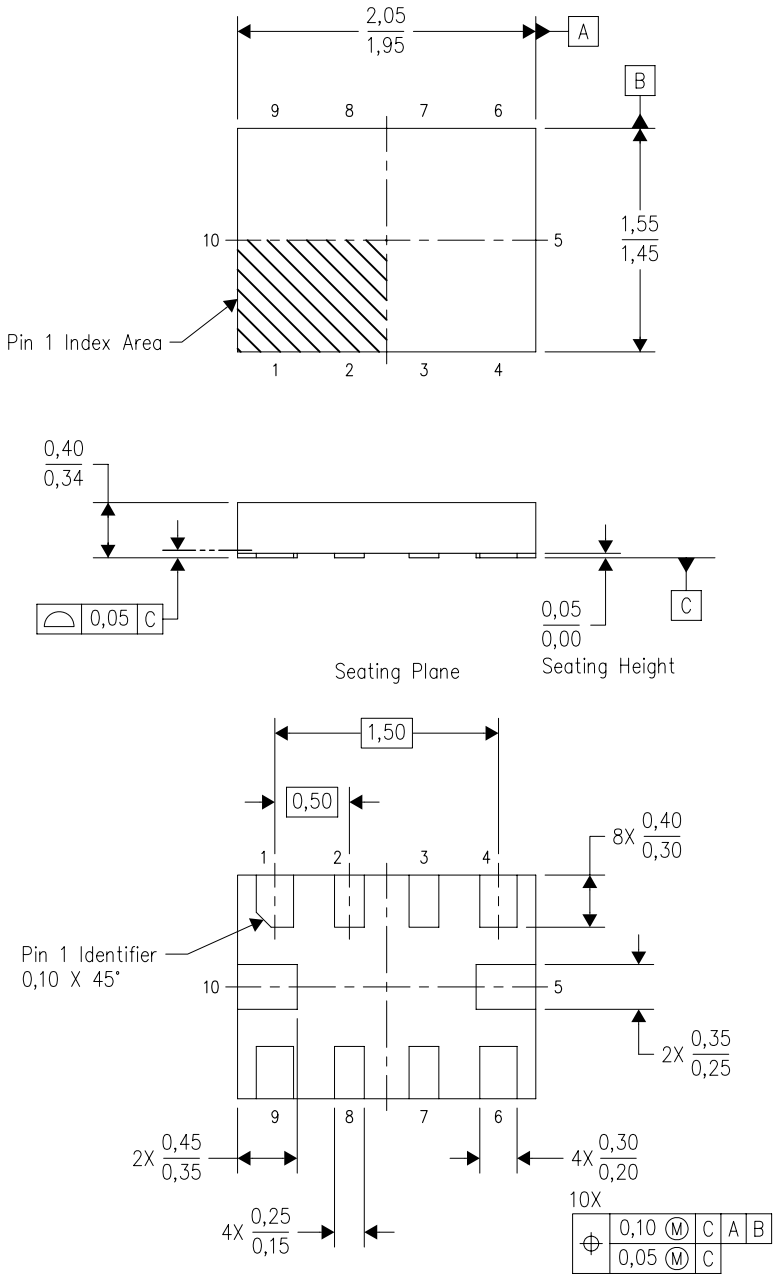
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK




4208528–3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

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