SBAS111C – JANUARY 1998 – REVISED JULY 2004

12-Bit, 8-Channel, Parallel Output ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 2.5V INTERNAL REFERENCE
- 8 INPUT CHANNELS
- 500kHz SAMPLING RATE
- SINGLE 5V SUPPLY
- ±1LSB: INL, DNL
- NO MISSING CODES
- 70dB SINAD
- LOW POWER: 13mW
- TQFP-32 PACKAGE

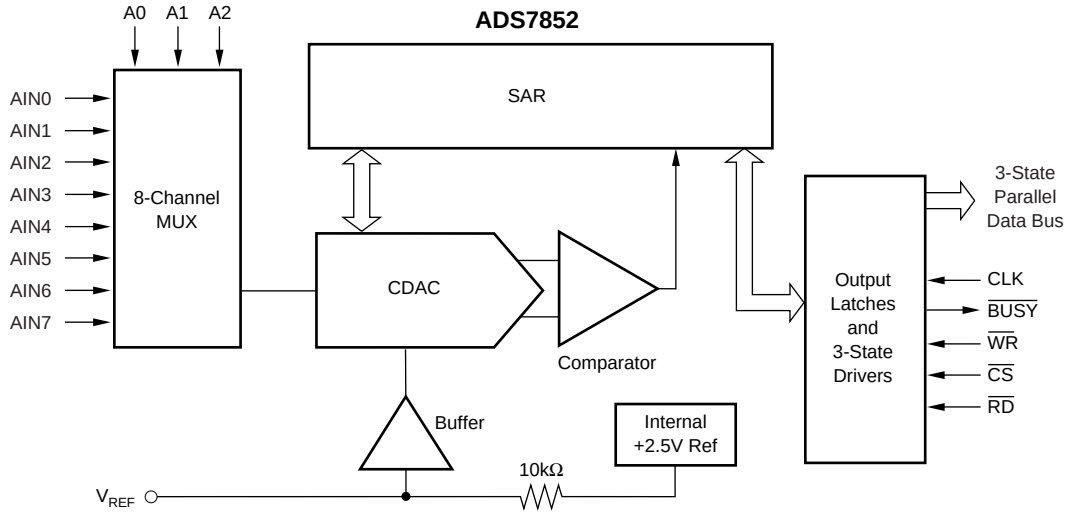
APPLICATIONS

- DATA ACQUISITION
- TEST AND MEASUREMENT
- INDUSTRIAL PROCESS CONTROL
- MEDICAL INSTRUMENTS

DESCRIPTION

The ADS7852 is an 8-channel, 12-bit Analog-to-Digital (A/D) converter complete with sample-and-hold, internal 2.5V reference and a full 12-bit parallel output interface. Typical power dissipation is 13mW at 500kHz throughput rate. The ADS7852 features both a nap mode and a sleep mode, further reducing the power consumption to 2mW. The input range is from 0V to twice the reference voltage. The reference voltage can be overdriven by an external voltage.

The ADS7852 is ideal for multi-channel applications where low power and small size are critical. Medical instrumentation, high-speed data acquisition and laboratory equipment are just a few of the applications that would take advantage of the special features offered by the ADS7852. The ADS7852 is available in an TQFP-32 package and is fully specified and ensured over the –40°C to +85°C temperature range.



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ABSOLUTE MAXIMUM RATINGS(1)

Analog Inputs to AGND, Any Channel Input	–0.3V to (V_D + 0.3V)
REF_{IN}	–0.3V to (V_D + 0.3V)
Digital Inputs to DGND	–0.3V to (V_D + 0.3V)
Ground Voltage Differences: AGND, DGND	±0.3V
$+V_{SS}$ to AGND	–0.3V to 6V
Power Dissipation	325mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MAXIMUM RELATIVE ACCURACY (LSB)	MAXIMUM GAIN ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7852Y	±2	±40	TQFP-32	PBS	–40°C to +85°C	A52Y	ADS7852Y/250	Tape and Reel, 250
ADS7852Y	"	"	"	"	"	"	ADS7852Y/2K	Tape and Reel, 2000
ADS7852YB	±1	±25	TQFP-32	PBS	–40°C to +85°C	A52YB	ADS7852YB/250	Tape and Reel, 250
ADS7852YB	"	"	"	"	"	"	ADS7852YB/2K	Tape and Reel, 2000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

ADS7852 CHANNEL SELECTION

A2	A1	A0	CHANNEL SELECTED
0	0	0	Channel 0
0	0	1	Channel 1
0	1	0	Channel 2
0	1	1	Channel 3
1	0	0	Channel 4
1	0	1	Channel 5
1	1	0	Channel 6
1	1	1	Channel 7

ELECTRICAL CHARACTERISTICS

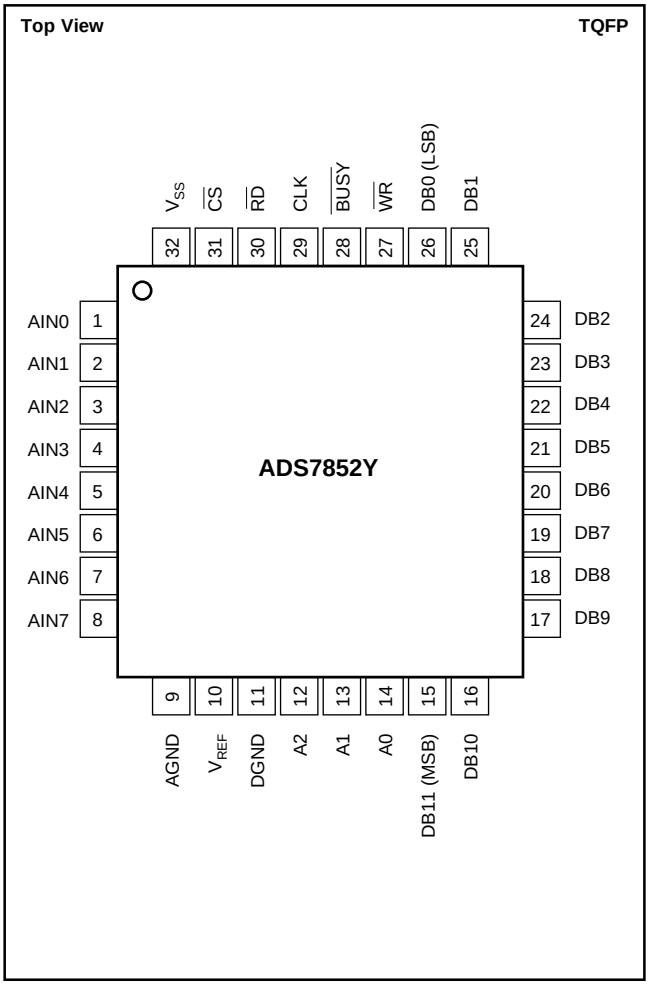
At T_A = –40°C to +85°C, f_S = 500kHz, f_{CLK} = 16 • f_S, and V_{SS} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7852Y			ADS7852YB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				12			*	Bits
ANALOG INPUT								
Input Voltage Range		0		5	*		*	V
Input Impedance			5M			*		Ω
Input Capacitance			15			*		pF
Input Leakage Current			±1			*		µA
DC ACCURACY								
No Missing Codes		12			*			Bits
Integral Linearity Error				±2			±1	LSB(1)
Differential Linearity Error			±1			±0.5	±1	LSB
Offset Error			±2	±5		±1	*	LSB
Offset Error Drift			±4			*		ppm/°C
Offset Error Match				±1			*	LSB
Gain Error(1)	Ext Ref = 2.5000V			±15			±10	LSB
Gain Error	Int Ref			±40			±25	LSB
Gain Error Drift			±25			*		ppm/°C
Gain Error Match				±1			*	LSB
Noise			150			*		µVrms
Power Supply Rejection Ratio	Worst-Case Δ, $+V_{SS}$ = 5V ±5%		1.2			*		LSB
SAMPLING DYNAMICS								
Conversion Time				13.5			*	Clk Cycles
Acquisition Time		1.5			*			Clk Cycles
Throughput Rate				500			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			5			*		ns
Aperture Jitter			30			*		ps
AC ACCURACY								
Signal-to-Noise Ratio			72			*		dB
Total Harmonic Distortion(3)	V_{IN} = 5Vp-p at 50kHz		–74	–72		–77	–76	dB
Signal-to-(Noise+Distortion)	V_{IN} = 5Vp-p at 50kHz	68	70		71	72		dB
Spurious Free Dynamic Range	V_{IN} = 5Vp-p at 50kHz	76	74		78	77		dB
Channel-to-Channel Isolation	V_{IN} = 5Vp-p at 50kHz		95			*		dB
REFERENCE OUTPUT								
Internal Reference Voltage		2.48	2.50	2.52	*	*	*	V
Internal Reference Drift			30			*		ppm/°C
Input Impedance	$\overline{CS}$ = GND		5			*		GΩ
	$\overline{CS}$ = V_{SS}		5			*		GΩ
Source Current(4)	Static Load			50			*	µA
REFERENCE INPUT								
Range		2.0		2.55	*		*	V
Resistance(5)	to Internal Reference Voltage		10			*		kΩ
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels:								
V_{IH}	I_{IH} = +5µA	3		$+V_{SS}$ + 0.3	*		*	V
V_{IL}	I_{IL} = +5µA	–0.3		0.8	*		*	V
V_{OH}	I_{OH} = 250µA	3.5			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENT								
$+V_{SS}$	Specified Performance	4.75		5.25	*		*	V
Quiescent Current			2.6	3.5		*	*	mA
Normal Power			13	17.5		*	*	mW
Nap Mode Current(6)			600	800		*	*	µA
Sleep Mode Current(6)			10	30		*	*	µA
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C
Storage		–65		+150	*		*	°C

* Specifications same as ADS7852Y.

NOTES: (1) LSB means Least Significant Bit, with V_{REF} equal to +2.5V, one LSB is 1.22mV. (2) Measured relative to an ideal, full-scale input of 4.999V. Thus, gain error includes the error of the internal voltage reference. (3) Calculated on the first nine harmonics of the input frequency. (4) If the internal reference is required to source current to an external load, the reference voltage will change due to the internal 10kΩ resistor. (5) Can vary ±30%. (6) See Timing Characteristics for further detail.

PIN CONFIGURATION



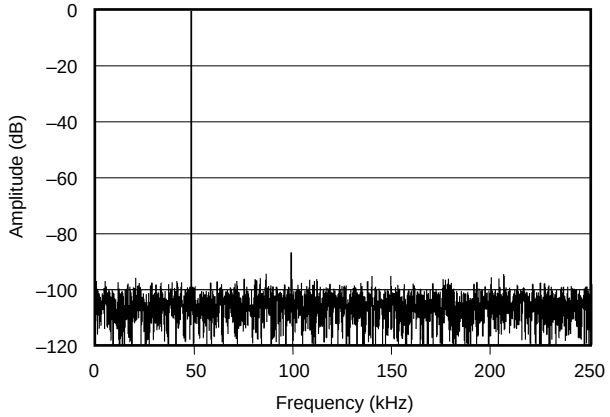
PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	AIN0	Analog Input Channel 0
2	AIN1	Analog Input Channel 1
3	AIN2	Analog Input Channel 2
4	AIN3	Analog Input Channel 3
5	AIN4	Analog Input Channel 4
6	AIN5	Analog Input Channel 5
7	AIN6	Analog Input Channel 6
8	AIN7	Analog Input Channel 7
9	AGND	Analog Ground, GND = 0V
10	V_{REF}	Voltage Reference Input and Output. See Electrical Characteristics table for ranges. Decouple to ground with a 0.1µF ceramic capacitor and a 2.2µF tantalum capacitor.
11	DGND	Digital Ground, GND = 0V
12	A2	Channel Address. See Channel Selection Table for details.
13	A1	Channel Address. See Channel Selection Table for details.
14	A0	Channel Address. See Channel Selection Table for details.
15	DB11	Data Bit 11 (MSB)
16	DB10	Data Bit 10
17	DB9	Data Bit 9
18	DB8	Data Bit 8
19	DB7	Data Bit 7
20	DB6	Data Bit 6
21	DB5	Data Bit 5
22	DB4	Data Bit 4
23	DB3	Data Bit 3
24	DB2	Data Bit 2
25	DB1	Data Bit 1
26	DB0	Data Bit 0 (LSB)
27	$\overline{WR}$	Write Input. Active LOW. Use to start a new conversion and to select an analog channel via address inputs A0, A1 and A2 in combination with $\overline{CS}$.
28	$\overline{BUSY}$	$\overline{BUSY}$ output goes LOW and stays LOW during a conversion. $\overline{BUSY}$ rises when a conversion is complete.
29	CLK	External Clock Input. The clock speed determines the conversion rate by the equation: $f_{CLK} = 16 \bullet f_{SAMPLE}$.
30	$\overline{RD}$	Read Input. Active LOW. Use to read the data outputs in combination with $\overline{CS}$. Also use (in conjunction with A0 or A1) to place device in power-down mode.
31	$\overline{CS}$	Chip Select Input. Active LOW. The combination of $\overline{CS}$ taken LOW and $\overline{WR}$ taken LOW initiates a new conversion and places the outputs in tri-state mode.
32	V_{SS}	Voltage Supply Input. Nominally +5V. Decouple to ground with a 0.1µF ceramic capacitor and a 10µF tantalum capacitor.

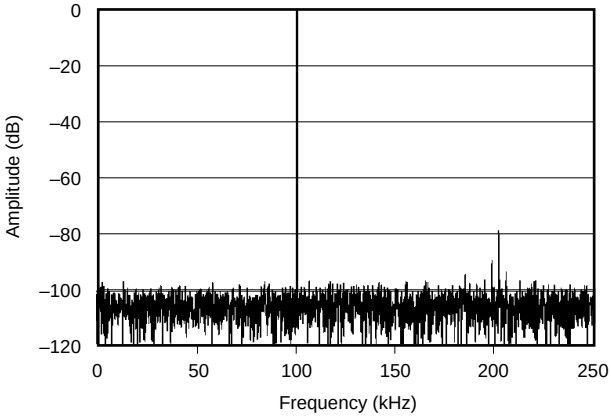
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{SS} = +5V, f_{SAMPLE} = 500kHz, f_{CLK} = 16 • f_{SAMPLE}, and internal reference, unless otherwise specified.

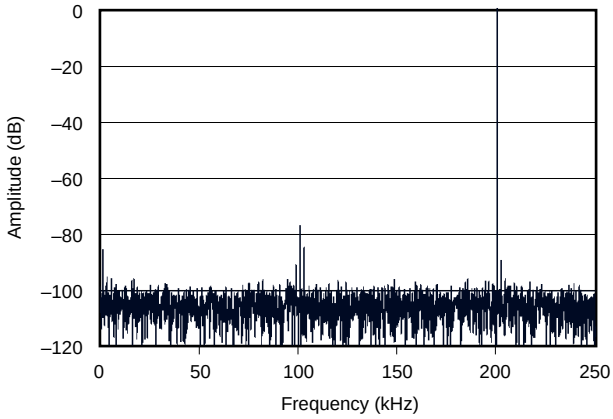
SPECTRAL PERFORMANCE
(4096 Point FFT, f_{IN} = 49.561kHz, –0.5dB)



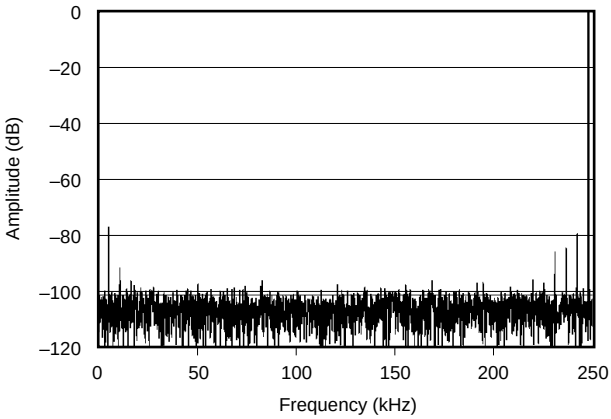
SPECTRAL PERFORMANCE
(4096 Point FFT, f_{IN} = 100.7081kHz, –0.5dB)



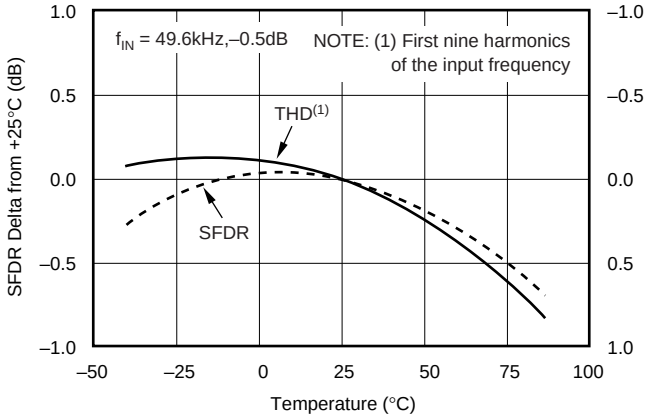
SPECTRAL PERFORMANCE
(4096 Point FFT, f_{IN} = 199.5851kHz, –0.5dB)



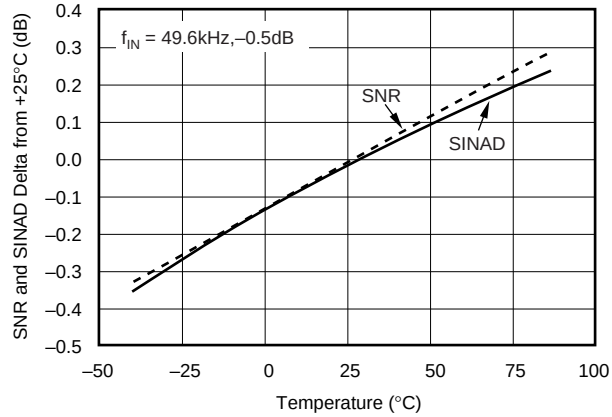
SPECTRAL PERFORMANCE
(4096 Point FFT, f_{IN} = 247.1921kHz, –0.5dB)



CHANGE IN SPURIOUS FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION vs TEMPERATURE



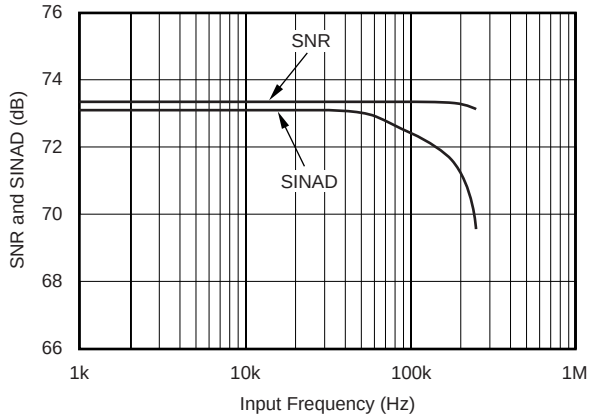
CHANGE IN SIGNAL-TO-NOISE RATIO AND
SIGNAL-TO-(NOISE+DISTORTION) vs TEMPERATURE



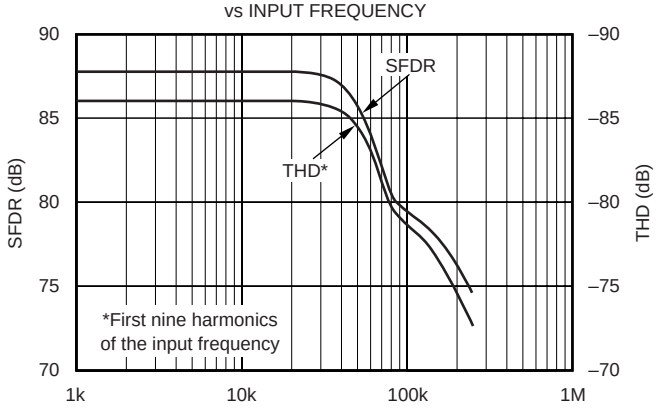
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{SS} = +5V, f_{SAMPLE} = 500kHz, f_{CLK} = 16 • f_{SAMPLE}, and internal reference, unless otherwise specified.

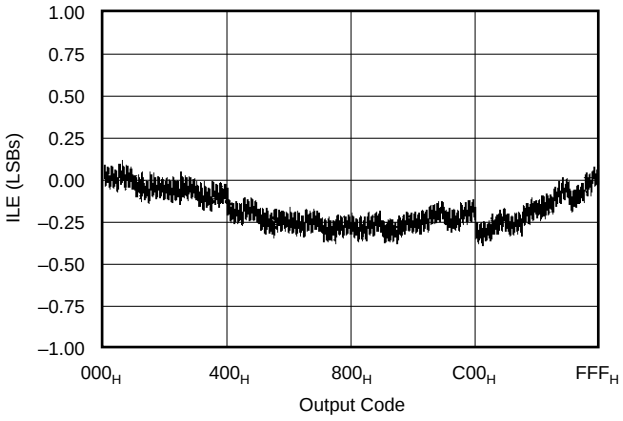
SIGNAL-TO-NOISE and
SIGNAL-TO-(NOISE+DISTORTION)
vs INPUT FREQUENCY



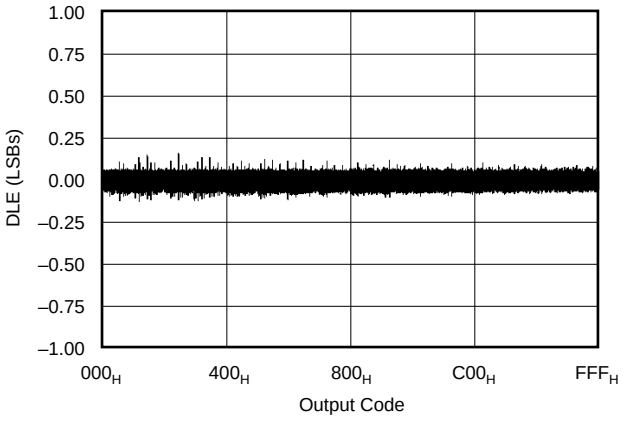
SPURIOUS FREE DYNAMIC RANGE and
TOTAL HARMONIC DISTORTION
vs INPUT FREQUENCY



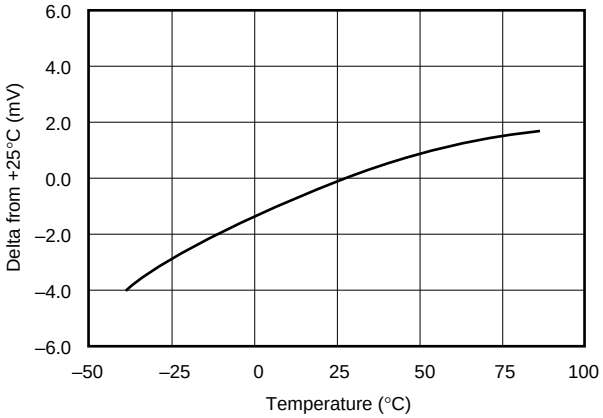
INTEGRAL LINEARITY ERROR vs CODE



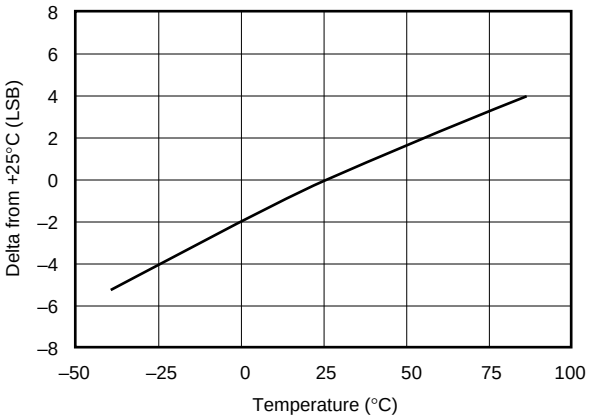
DIFFERENTIAL LINEARITY ERROR vs CODE



CHANGE IN INTERNAL REFERENCE VOLTAGE
vs TEMPERATURE



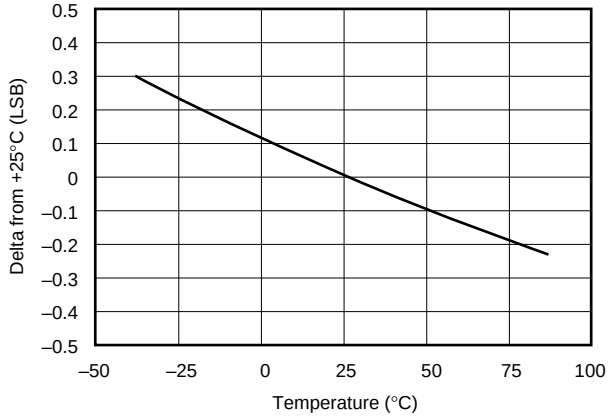
CHANGE IN GAIN ERROR vs TEMPERATURE



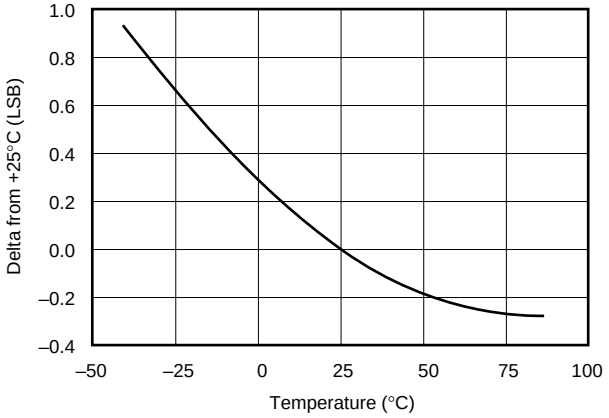
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{SS} = +5V, f_{SAMPLE} = 500kHz, f_{CLK} = 16 • f_{SAMPLE}, and internal reference, unless otherwise specified.

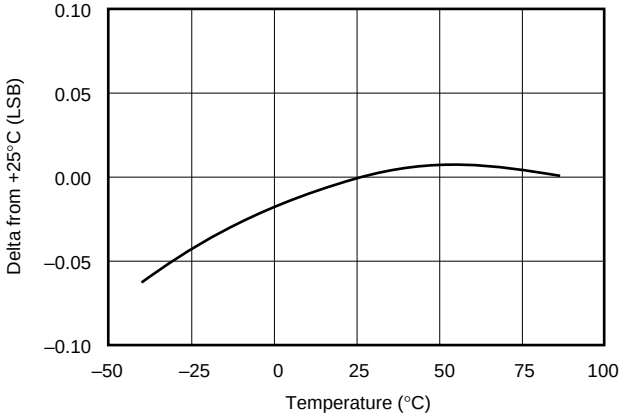
CHANGE IN GAIN ERROR vs TEMPERATURE
(With External 2.5V Reference)



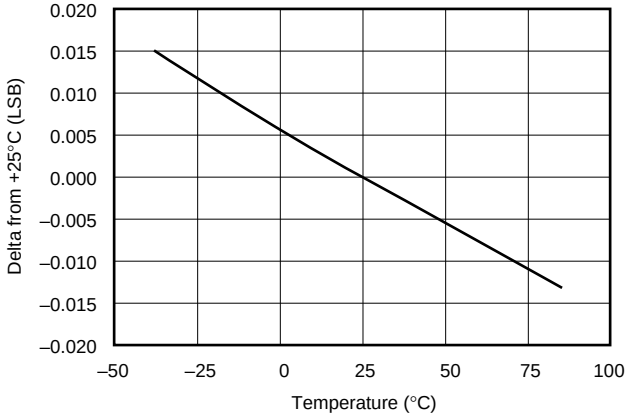
CHANGE IN OFFSET vs TEMPERATURE



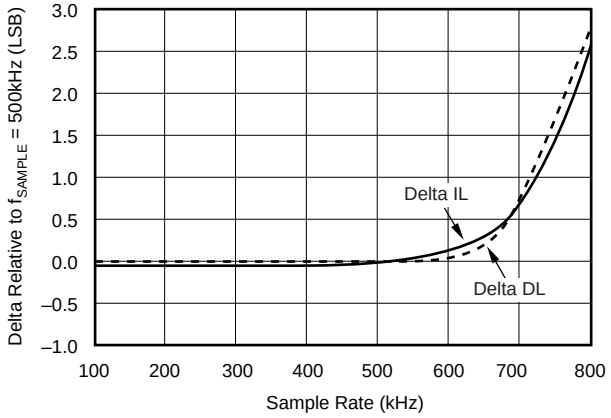
CHANGE IN WORST-CASE CHANNEL-TO-CHANNEL
OFFSET MISMATCH vs TEMPERATURE



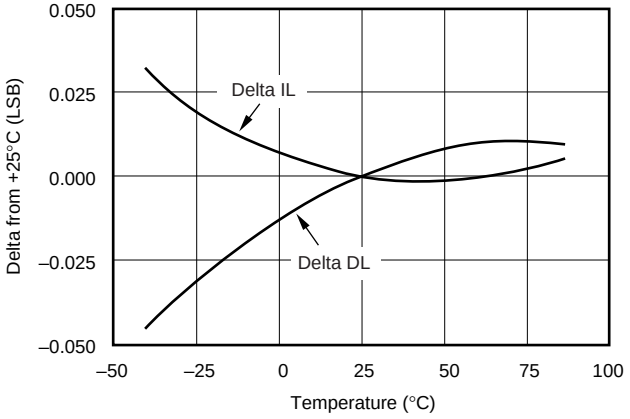
CHANGE IN WORST-CASE CHANNEL-TO-CHANNEL
GAIN MISMATCH vs TEMPERATURE



CHANGE IN WORST-CASE INTEGRAL LINEARITY
AND DIFFERENTIAL LINEARITY vs SAMPLE RATE



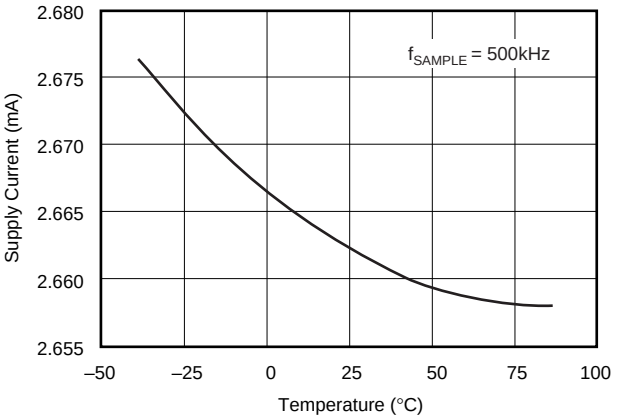
CHANGE IN WORST-CASE INTEGRAL LINEARITY
AND DIFFERENTIAL LINEARITY vs TEMPERATURE



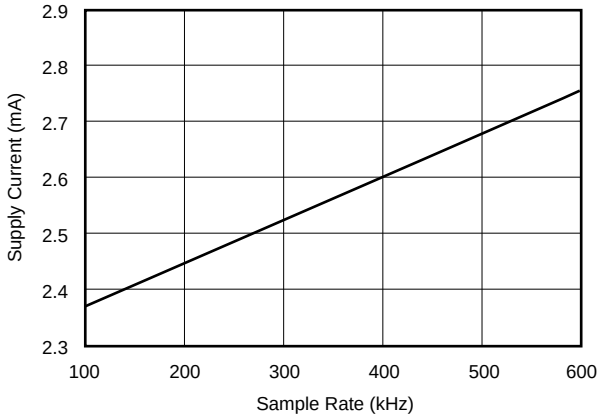
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_{SS} = +5V, f_{SAMPLE} = 500kHz, f_{CLK} = 16 • f_{SAMPLE}, and internal reference, unless otherwise specified.

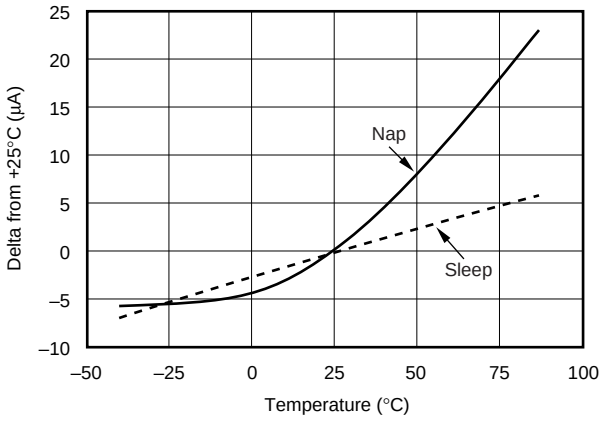
SUPPLY CURRENT vs TEMPERATURE



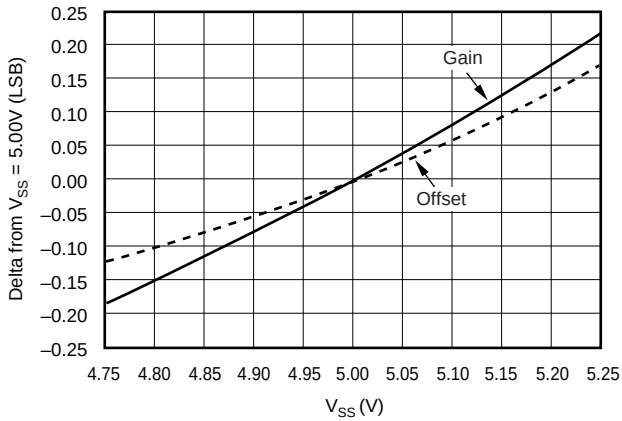
SUPPLY CURRENT vs SAMPLE RATE



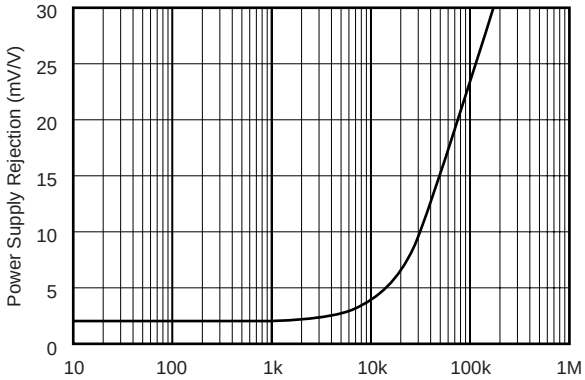
CHANGE IN NAP CURRENT AND SLEEP CURRENT vs TEMPERATURE



CHANGE IN GAIN AND OFFSET vs SUPPLY VOLTAGE



POWER SUPPLY REJECTION vs POWER SUPPLY RIPPLE FREQUENCY



THEORY OF OPERATION

The ADS7852 is a high-speed successive approximation register (SAR) Analog-to-Digital (A/D) converter with an internal 2.5V bandgap reference. The architecture is based on capacitive redistribution, which inherently includes a sample/hold function. The converter is fabricated on a 0.6micron CMOS process. Figure 1 shows the basic operating circuit for the ADS7852.

The ADS7852 requires an external clock to run the conversion process. This clock can vary between 200kHz (12.5Hz throughput) and 8MHz (500kHz throughput). The duty cycle of the clock is unimportant as long as the minimum HIGH and LOW times are at least 50ns and the clock period is at least 125ns. The minimum clock frequency is governed by the parasitic leakage of the Capacitive Digital-to-Analog (CDAC) capacitors internal to the ADS7852.

The front-end input multiplexer of the ADS7852 features eight single-ended analog inputs. Channel selection is performed using the address pins A0 (pin 14), A1 (pin 13), and A2 (pin 12). When a conversion is initiated, the input voltage is sampled on the internal capacitor array. While a conversion is in progress, all channel inputs are disconnected from any internal function.

The range of the analog input is set by the voltage on the V_{REF} pin. With the internal 2.5V reference, the input range is 0V to 5V. An external reference voltage can be placed on V_{REF}, overdriving the internal voltage. The range for the external voltage is 2.0V to 2.55V, giving an input voltage range of 4.0V to 5.1V.

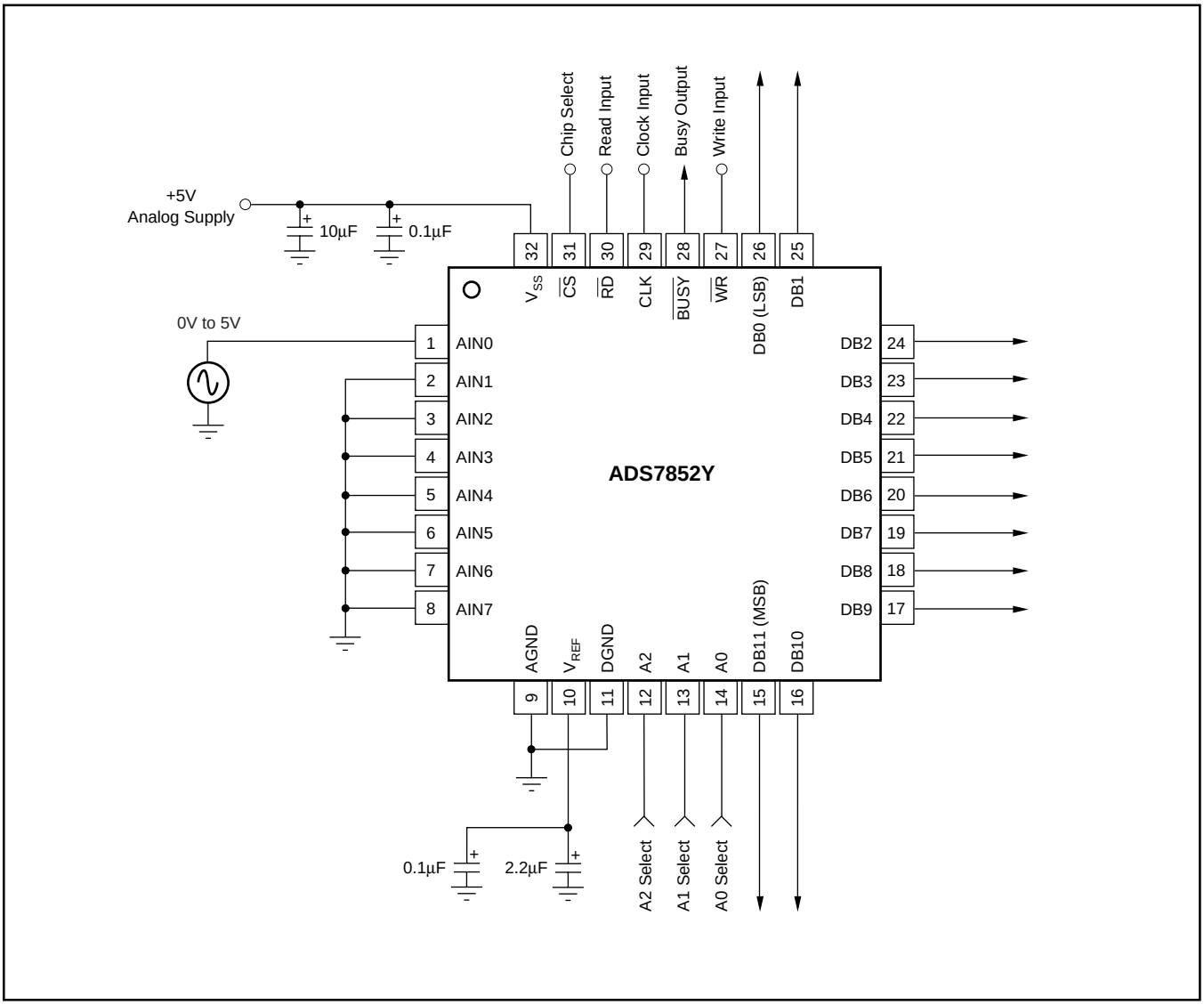


FIGURE 1. Typical Circuit Configuration.

ANALOG INPUTS

The ADS7852 features eight single-ended inputs. While the static current into each analog input is basically zero, the dynamic current depends on the input voltage and sample rate. The current into the device must charge the internal hold capacitor during the sample period. After this capacitor has been fully charged, no further input current is required. For optimum performance, the source driving the analog inputs must be capable of charging the input capacitance to a 12-bit settling level within the sample period. This can be as little as 350ns in some operating modes. While the converter is in the hold mode, or after the sampling capacitor has been fully charged, the input impedance of the analog input is greater than 1GΩ.

REFERENCE

The reference voltage on the V_{REF} pin establishes the full-scale range of the analog input. The ADS7852 can operate with a reference in the range of 2.0V to 2.55V corresponding to a full-scale range of 4.0V to 5.1V.

The voltage at the V_{REF} pin is internally buffered, and this buffer drives the capacitor DAC portion of the converter. This feature is important because the buffer greatly reduces the dynamic load placed on the reference source. Since the voltage at V_{REF} will be unavoidably affected by noise and glitches generated during the conversion process, it is highly recommended that the V_{REF} pin be bypassed to ground as outlined in the sections that follow.

INTERNAL REFERENCE

The ADS7852 contains an onboard 2.5V reference, resulting in a 0V to 5V input range on the analog input. The Specifications Table gives the various specifications for the internal reference. This reference can be used to supply a small amount of source current to an external load but the load should be static. Due to the internal 10kΩ resistor, a dynamic load will cause variations in the reference voltage, and will dramatically affect the conversion result. Note that even a static load will reduce the internal reference voltage seen at the buffer input. The amount of reduction depends on the load and the actual value of the internal 10kΩ resistor. The value of this resistor can vary by ±30%.

The V_{REF} pin should be bypassed with a 0.1µF ceramic capacitor placed as close to the ADS7852 as possible. In addition, a 2.2µF tantalum capacitor should be used in parallel with the ceramic capacitor.

EXTERNAL REFERENCE

The internal reference is connected to the V_{REF} pin and to the internal buffer via an on-chip 10kΩ series resistor. Because of this configuration, the internal reference voltage can easily be overridden by an external reference voltage. The voltage range for the external voltage is 2.00V to 2.55V, corresponding to an analog input range of 4.0V to 5.1V.

While the external reference will not have to provide significant dynamic current to the V_{REF} in, it does have to drive the series 10kΩ resistor that is connected to the 2.5V internal reference. Accounting for the maximum difference between the external reference voltage and the internal reference voltage, and the processing variations for the on-chip 10kΩ resistor, this current can be as high as 75µA. In addition, the V_{REF} pin should still be bypassed to ground with at least a 0.1µF ceramic capacitor placed as close to the ADS7852 as possible. Depending on the particular reference and A/D conversion speed, additional bypass capacitance may be required, such as the 2.2µF tantalum capacitor shown in the Typical Circuit Configuration (Figure 1). Close attention should be paid to the stability of any external reference source that is driving the large bypass capacitors present at the V_{REF} pin.

BASIC OPERATION

Figure 1 shows the simple circuit required to operate the ADS7852 with Channel 0 selected. A conversion can be initiated by bringing the $\overline{WR}$ pin (pin 27) LOW for a minimum of 35ns. $\overline{BUSY}$ (pin 28) will output a LOW during the conversion process and rises only after the conversion is complete. The 12 bits of output data will be valid on pins 15 through 26 following the rising edge of $\overline{BUSY}$.

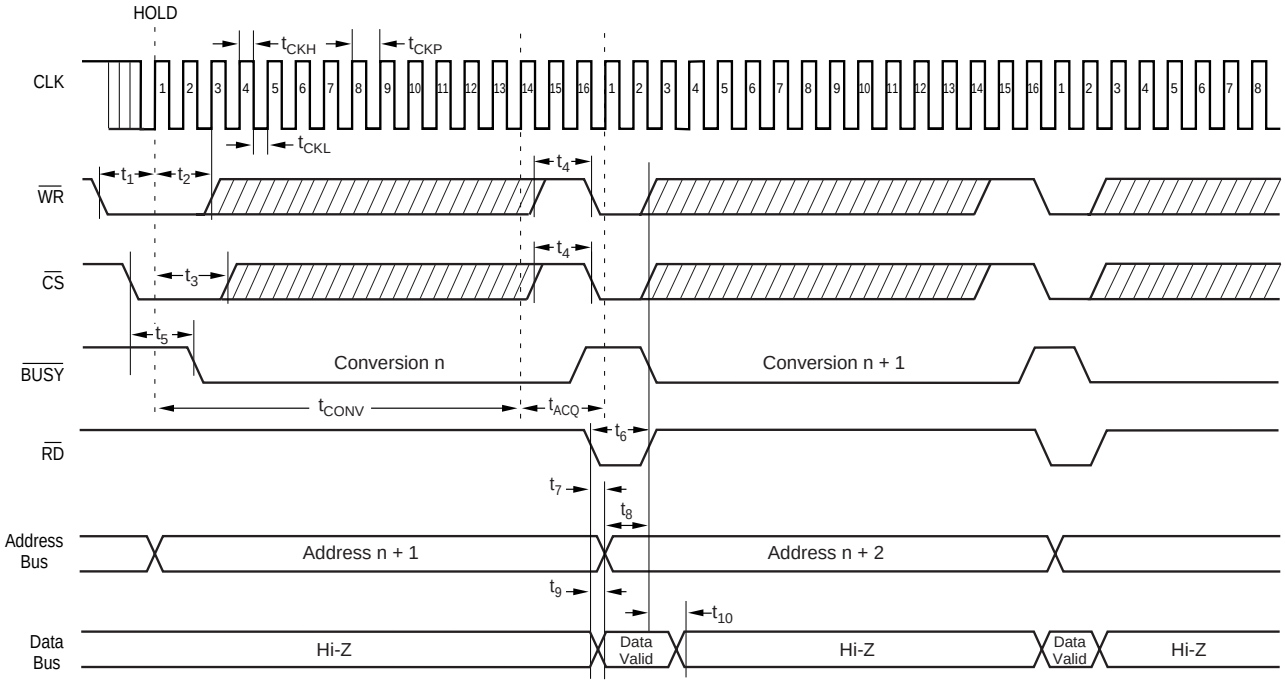
STARTING A CONVERSION

A conversion is initiated on the falling edge of the $\overline{WR}$ input, with valid signals on A0, A1, A2, and $\overline{CS}$. The ADS7852 will enter the conversion mode on the first rising edge of the external clock following the $\overline{WR}$ pin going LOW. The conversion process takes 13.5 clock cycles (1.5 cycles for the DB0 decision, 2 clock cycles for the DB5 decision, and 1 clock cycle for each of the other bit decisions). This allows 2.5 clock cycles for sampling. Upon initiating a conversion, the $\overline{BUSY}$ output will go LOW approximately 20ns after the falling edge of the $\overline{WR}$ pin. The $\overline{BUSY}$ output will return HIGH just after the ADS7852 has finished a conversion and the output data will be valid on pins 15 through 26. The rising edge of $\overline{BUSY}$ can be used to latch the output data into an external device. It is recommended that the data be read immediately after each conversion since the switching noise of the asynchronous data transfer can cause digital feedthrough degrading the converter performance (see Figure 2).

CHANNEL ADDRESSING

The selection of the analog input channel to be converted is controlled by address pins A0, A1, and A2. This channel becomes active on the rising edge of $\overline{WR}$ with $\overline{CS}$ held LOW. The data on the address pins should be stable for at least 10ns prior to $\overline{WR}$ going HIGH.

The address pins are also used to control the power-down functions of the ADS7852. Careful attention must be paid to the status of the address pins following each conversion. If the user does not want the ADS7852 to enter either of the power-down modes following a conversion, the A0 and A1 pins must be LOW when $\overline{RD}$ and $\overline{CS}$ are returned HIGH after reading the data at the end of a conversion (see the Power-Down Mode section of this data sheet for more details).



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time			1.75	µs
t_{ACQ}	Acquisition Time			0.25	µs
t_{CKP}	Clock Period	125		5000	ns
t_{CKL}	Clock LOW	40			ns
t_{CKH}	Clock HIGH	40			ns
t_1	$\overline{WR}$ LOW Prior to Rising Edge of CLK	35			ns
t_2	$\overline{WR}$ LOW After Rising Edge of CLK	20			ns
t_3	$\overline{CS}$ LOW After Rising Edge of CLK	20			ns
t_4	$\overline{CS}$ and $\overline{RD}$ HIGH	25			ns
t_5	$\overline{BUSY}$ Delay After $\overline{CS}$ LOW	20			ns
t_6	$\overline{RD}$ LOW	25			ns
t_7	Address Hold Time	5			ns
t_8	Address Setup Time	5			ns
t_9	Bus Access Time	30			ns
t_{10}	Bus Relinquish Time	5			ns
t_{11}	$\overline{CS}$ to $\overline{RD}$ Setup Time	0			ns
t_{12}	$\overline{RD}$ to $\overline{CS}$ Hold Time	0			ns
t_{13}	CLK LOW to $\overline{BUSY}$ HIGH	10			ns
t_{14}	$\overline{BUSY}$ to $\overline{RD}$ Delay	0			ns
t_{15}	$\overline{RD}$ HIGH to CLK LOW	50			ns

FIGURE 2. ADS7852 Write/Read Timing.

READING DATA

Data from the ADS7852 will appear at pins 15 through 26. The MSB will output on pin 15 while the LSB will output on pin 26. The outputs are coded in Straight Binary (with 0V = 000_H and 5V = FFF_H). Following a conversion, the $\overline{BUSY}$ pin will go HIGH. After $\overline{BUSY}$ has been HIGH for at least t_{14} seconds, the $\overline{CS}$ and $\overline{RD}$ pins may be brought LOW to enable the 12-bit output bus. $\overline{CS}$ and $\overline{RD}$ must be held LOW for at least 25ns following $\overline{BUSY}$ HIGH. Data will be valid 30ns after the falling edge of both $\overline{CS}$ and $\overline{RD}$. The output data will remain valid for 20ns following the rising edge of both $\overline{CS}$ and $\overline{RD}$ (see Figure 2 for the read cycle timing diagram).

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT STRAIGHT BINARY	
		BINARY CODE	HEX CODE
Least Significant Bit (LSB)	1.2207mV		
Full Scale	4.99878V	1111 1111 1111	FFF
Midscale	2.5V	1000 0000 0000	800
Midscale –1LSB	2.49878V	0111 1111 1111	7FF
Zero Full Scale	0V	0000 0000 0000	000

Table I. Ideal Input Voltages and Output Codes.

POWER-DOWN MODE

The ADS7852 has two different power-down modes: the Nap mode and the Sleep mode. In Nap mode, all analog and digital circuitry is powered off, with the exception of the voltage reference. In Sleep mode, the device is completely powered off.

While the Sleep mode affords the lowest power consumption, the time to come out of Sleep mode can be considerable since it takes the internal reference voltage a finite amount of time to power up and reach a stable value. This latency can result in spurious output data for a minimum of ten conversion cycles at a 500kHz sampling rate. It should also be noted that any external load connected to the V_{REF} pin will increase this effect since a discharge path for the V_{REF} bypass capacitor is provided during the Sleep cycle. Even the parasitic leakage of the bypass capacitor itself should be considered if the unit is left in the Sleep mode for an extended period. After power-up, this capacitor must be recharged by the internal reference voltage and the on-chip 10kΩ series resistor. Under worst-case conditions (for example, the bypass capacitor is completely discharged), the output data can be invalid for several hundred milliseconds.

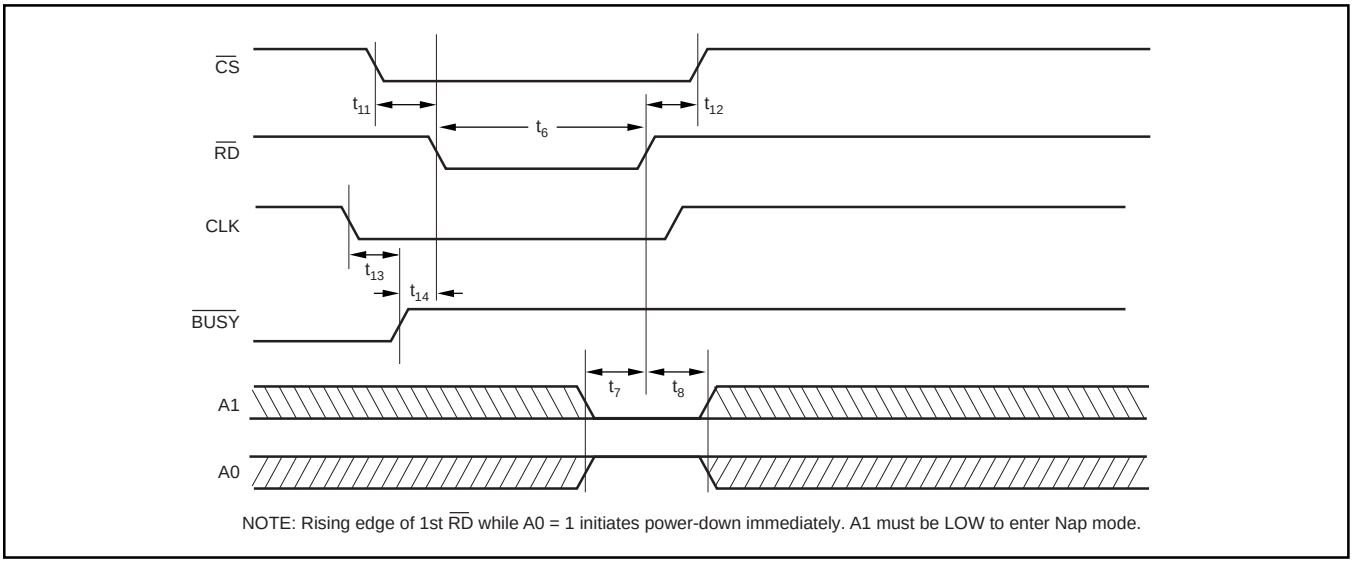
Since the Nap mode maintains the voltage on the V_{REF} pin by keeping the internal reference powered-up, valid conversions are available immediately after the Nap mode is terminated.

The simplest way to use the power-down mode is following a conversion. After a conversion has finished and $\overline{BUSY}$ has returned HIGH, $\overline{CS}$ and $\overline{RD}$ must be brought LOW for a minimum of 25ns. When $\overline{RD}$ and $\overline{CS}$ are returned HIGH, the ADS7852 will enter the power-down mode on the rising edge of $\overline{RD}$. If $\overline{CS}$ is always kept LOW, the power-down mode will be controlled exclusively by $\overline{RD}$. Depending on the status of the A0 and A1 address pins, the ADS7852 will either enter the Nap mode, the Sleep mode, or be returned to normal operation in the sampling mode. See Table II and Figures 3 and 4 for further details.

$\overline{RD}$	A2	A1	A0	POWER-DOWN MODE
↓	X	0	0	None
↓	X	1	0	Sleep
↓	X	0	1	Nap
↓	X	1	1	Sleep

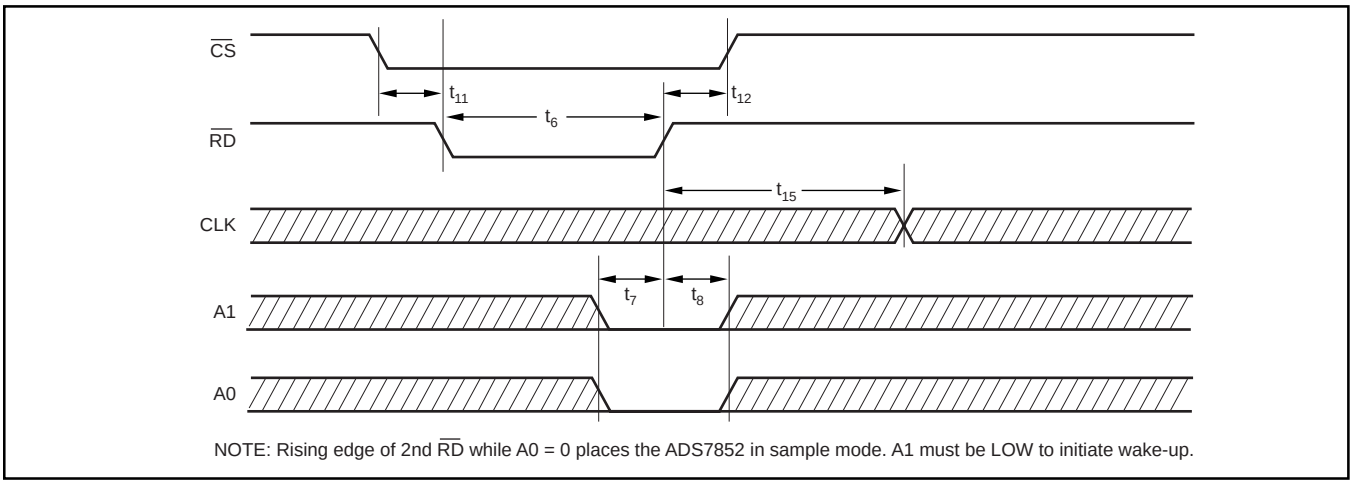
↓ = Signifies rising edge of $\overline{RD}$ pin. X = Don't care

TABLE II. ADS7852 Power-Down Mode.



NOTE: Rising edge of 1st $\overline{RD}$ while A0 = 1 initiates power-down immediately. A1 must be LOW to enter Nap mode.

FIGURE 3. Entering Nap Using $\overline{RD}$ and A0.



NOTE: Rising edge of 2nd $\overline{RD}$ while A0 = 0 places the ADS7852 in sample mode. A1 must be LOW to initiate wake-up.

FIGURE 4. Initiating Wake-Up Using $\overline{RD}$ and A0.

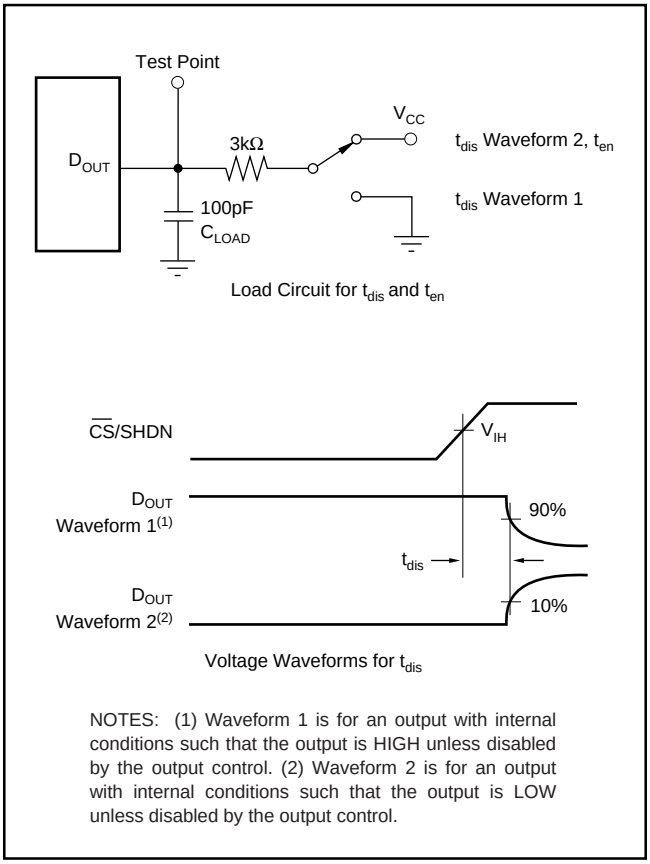


FIGURE 5. Timing Diagram and Test Circuits for Parameters in Figure 2.

In addition to using the address pins in conjunction with $\overline{RD}$, the power-down mode can also be terminated implicitly by starting a new conversion (for example, taking $\overline{WR}$ LOW while $\overline{CS}$ is LOW). If it is desired to keep the ADS7852 in a power-down state for a period that is greater than dictated by the sampling rate, the convert signal driving the $\overline{WR}$ pin must be disabled.

The typical supply current of the ADS7852 is 2.6mA, with a 5V supply and a 500kHz sampling rate. In the Nap mode, the typical supply current is 600µA. In the Sleep mode, the current is typically reduced to 10µA.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7852 circuitry. This is particularly true if the CLK input is approaching the maximum throughput rate.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, driving any single conversion for an n-bit SAR converter, there are n "windows" in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. This error can change if the external event changes in times with respect to the CLK input.

With this effect in mind, power to the ADS7852 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor may be used to low pass filter a noisy supply. The ADS7852 draws very little current from an external reference on average as the reference voltage is internally buffered. However, glitches from the conversion process appear at the V_{REF} input and the reference source must be able to handle this. Whether the reference is internal or external, the V_{REF} pin should be bypassed with a 0.1µF capacitor. An additional larger capacitor may also be used, if desired. If the reference voltage is external and originates from an op amp, make sure it can drive the bypass capacitor or capacitors without oscillation.

The GND pin should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections which are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7852Y/250	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	A52Y	Samples
ADS7852Y/250G4	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	A52Y	Samples
ADS7852Y/2K	ACTIVE	TQFP	PBS	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		A52Y	Samples
ADS7852YB/250	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		A52Y B	Samples
ADS7852YB/250G4	ACTIVE	TQFP	PBS	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		A52Y B	Samples
ADS7852YB/2K	ACTIVE	TQFP	PBS	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		A52Y B	Samples

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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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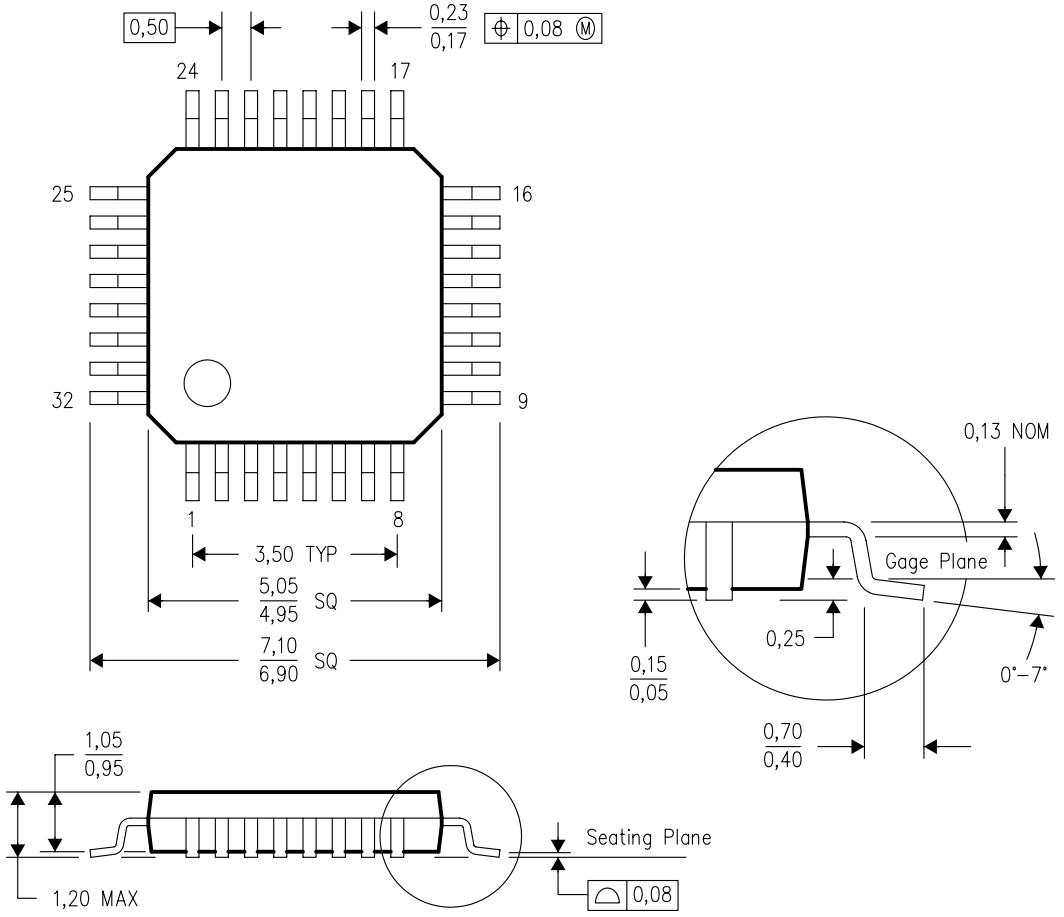

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

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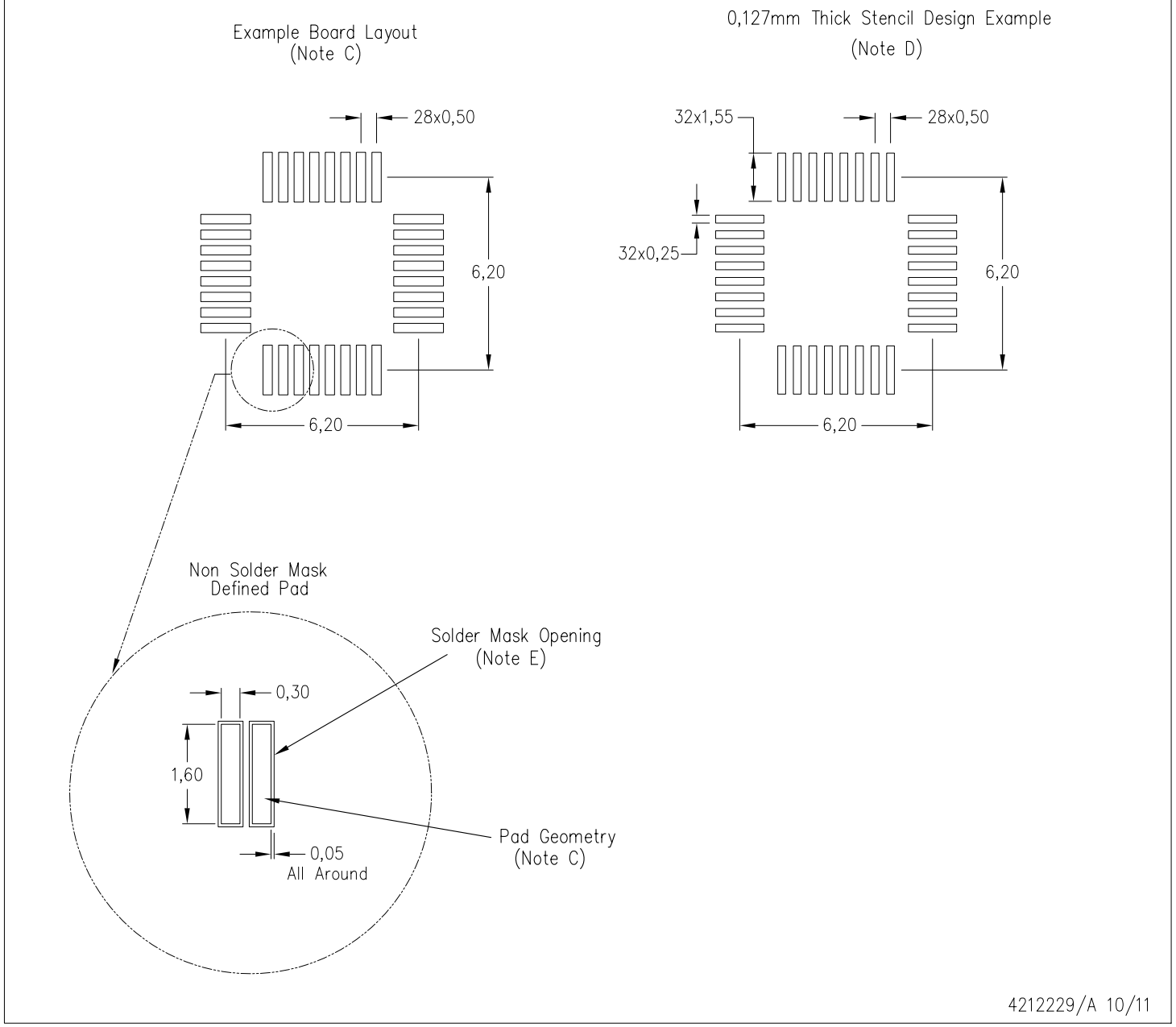

NOTES:
A. All linear dimensions are in millimeters.
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D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
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