



用于桥式传感器的 24 位模数转换器

 查询样片: [ADS1231](#)

特性

- 针对桥式传感器的完整前端
- 内部放大器, **128** 增益
- 内部振荡器
- 针对桥式传感器的低侧电源开关
- 低噪声: **35nVrms**
- 可选数据速率: **10SPS** 或 **80SPS**
- **10SPS** 时, 同时 **50Hz** 和 **60Hz** 抑制
- 输入电磁干扰 (EMI) 滤波器
- 针对比例式测量的高达 **5V** 的外部电压基准
- 简单、引脚驱动控制
- 两线制串行数字接口
- 电源范围: **3V** 至 **5.3V**
- 封装: 小外形尺寸集成电路 (SOIC)-16
- 温度范围: **-40°C** 至 **+85°C**

应用范围

- 衡器
- 应力计
- 测压元件
- 工业过程控制

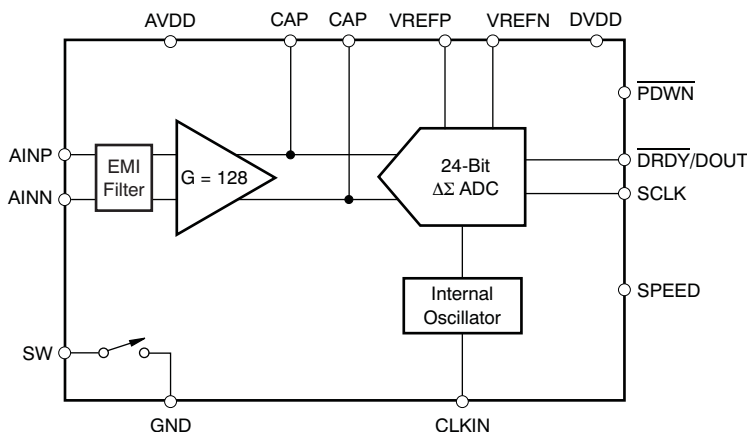
说明

ADS1231 是一款精密 24 位模数转换器 (ADC)。借助于板载低噪声放大器和振荡器, 精密型三阶 $\Delta\Sigma$ 调制器以及桥式电源开关, ADS1231 为包括衡器、应力计和测压元件在内的桥式传感器应用提供一个完整的前端解决方案。

此噪声放大器具有 128 的增益, 从而支持 $\pm 19.5\text{mV}$ 的满量程差分输入。此 $\Delta\Sigma$ ADC 具有 24 位分辨率, 并且包含一个三阶调制器和四阶数字滤波器。支持两个数据速率: 10SPS (具有 50Hz 和 60Hz 抑制) 以及 80SPS。ADS1231 可被置于低功耗待机模式, 或者在断电模式中完全关闭。

ADS1231 由专用引脚控制; 没有编程用的数字寄存器。数据通过直接接至 MSP430 或其它微控制器的一个易于隔离的串行接口输出。

ADS1231 采用小外形尺寸 (SO)-16 封装, 额定温度范围 -40°C 至 $+85^\circ\text{C}$ 。



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range, unless otherwise noted.

		ADS1231	UNIT
AVDD to GND		-0.3 to +6	V
DVDD to GND		-0.3 to +6	V
Input current		100, momentary	mA
		10, continuous	mA
Analog input voltage to GND		-0.3 to AVDD + 0.3	V
Digital input voltage to GND		-0.3 to DVDD + 0.3	V
ESD ⁽²⁾	Human body model (HBM) JEDEC standard 22, test method A114-C.01, all pins	±2000	V
	Charged device model (CDM) JEDEC standard 22, test method C101, all pins	±500	V
Maximum junction temperature		+150	°C
Operating temperature range		-40 to +85	°C
Storage temperature range		-60 to +150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) CAUTION: ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		ADS1231	UNITS
		SOIC (D)	
		16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	79.5	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance	37.5	
θ_{JB}	Junction-to-board thermal resistance	37.1	
Ψ_{JT}	Junction-to-top characterization parameter	5.6	
Ψ_{JB}	Junction-to-board characterization parameter	36.7	
θ_{JCbott}	Junction-to-case (bottom) thermal resistance	n/a	

(1) 有关传统和全新热度的更多信息，请参阅 IC 封装热度量 应用报告 (文献号: ZHCA543)。

ELECTRICAL CHARACTERISTICS

Minimum/maximum limit specifications apply from -40°C to $+85^{\circ}\text{C}$. Typical specifications at $+25^{\circ}\text{C}$.

All specifications at $\text{AVDD} = \text{DVDD} = \text{VREFP} = +5\text{V}$, $\text{V}_{\text{CM}} = 2.5\text{V}$ and $\text{VREFN} = \text{GND}$, unless otherwise noted.

PARAMETER	CONDITIONS	ADS1231			UNIT	
		MIN	TYP	MAX		
ANALOG INPUTS						
Full-scale input voltage (AINP – AINN)			$\pm 0.5V_{\text{REF}} / 128$		V	
	$V_{\text{REF}} = \text{AVDD} = 5\text{V}$		± 19.5		mV	
	$V_{\text{REF}} = \text{AVDD} = 3\text{V}$		± 11.7		mV	
Common-mode input range		$\text{GND} + 1.5$		$\text{AVDD} - 1.5$	V	
Differential input current			± 2		nA	
LOW-SIDE POWER SWITCH						
On-resistance (R_{ON})	$\text{AVDD} = 5\text{V}$, $I_{\text{SW}} = 30\text{mA}$		3.5	5	Ω	
	$\text{AVDD} = 3\text{V}$, $I_{\text{SW}} = 30\text{mA}$		4	7	Ω	
Current through switch				30	mA	
SYSTEM PERFORMANCE						
Resolution	No missing codes	24			Bits	
Data rate	Internal oscillator, SPEED = high		80		SPS	
	Internal oscillator, SPEED = low		10		SPS	
	External clock, SPEED = high		$f_{\text{CLKIN}} / 61,440$		SPS	
	External clock, SPEED = low		$f_{\text{CLKIN}} / 491,520$		SPS	
Digital filter settling time	Full settling		4		Conversions	
Noise	$f_{\text{DATA}} = 10\text{SPS}$, $\text{AVDD} = V_{\text{REF}} = 5\text{V}$		35		nV, rms	
	$f_{\text{DATA}} = 80\text{SPS}$, $\text{AVDD} = V_{\text{REF}} = 5\text{V}$		102		nV, rms	
	$f_{\text{DATA}} = 10\text{SPS}$, $\text{AVDD} = V_{\text{REF}} = 5\text{V}$		232		nV, P-P	
	$f_{\text{DATA}} = 80\text{SPS}$, $\text{AVDD} = V_{\text{REF}} = 5\text{V}$		622		nV, P-P	
Integral nonlinearity (INL)	Differential input, end-point fit		± 8		ppm	
Input offset error			10		μV	
Input offset drift			± 20		$\text{nV}/^{\circ}\text{C}$	
Gain error			1		%	
Gain drift			± 2		$\text{ppm}/^{\circ}\text{C}$	
Normal-mode rejection ⁽¹⁾	$f_{\text{IN}} = 50\text{Hz}$ or $60\text{Hz} \pm 1\text{Hz}$, $f_{\text{DATA}} = 10\text{SPS}$, internal oscillator	80	100		dB	
	$f_{\text{IN}} = 50\text{Hz}$ or $60\text{Hz} \pm 1\text{Hz}$, $f_{\text{DATA}} = 10\text{SPS}$, external clock ⁽²⁾	90	110		dB	
Common-mode rejection	At dc		110		dB	
Power-supply rejection	At dc	90	100		dB	
VOLTAGE REFERENCE INPUT						
Voltage reference input (V_{REF})	$V_{\text{REF}} = \text{VREFP} - \text{VREFN}$	1.5	AVDD	$\text{AVDD} + 0.1$	V	
Negative reference input (VREFN)		$\text{GND} - 0.1$		$\text{VREFP} - 1.5$	V	
Positive reference input (VREFP)		$\text{VREFN} + 1.5$		$\text{AVDD} + 0.1$	V	
Voltage reference input current			10		nA	
DIGITAL INPUT/OUTPUT (DVDD = 3V to 5.3V)						
Logic levels	V_{IH}		0.8 DVDD		$\text{DVDD} + 0.1$	V
	V_{IL}		GND		0.2 DVDD	V
	V_{OH}	$I_{\text{OH}} = 500\mu\text{A}$	$\text{DVDD} - 0.4$			V
	V_{OL}	$I_{\text{OL}} = 500\mu\text{A}$			0.2 DVDD	V
Input leakage	$0 < V_{\text{DIGITAL INPUT}} < \text{DVDD}$			± 10	μA	
External clock input frequency (f_{CLKIN})		1	4.9152	6	MHz	
Serial clock input frequency (f_{SCLK})				5	MHz	

(1) Specification is assured by the combination of design and final test.

(2) $f_{\text{CLKIN}} = 4.9152\text{MHz}$.

ELECTRICAL CHARACTERISTICS (continued)

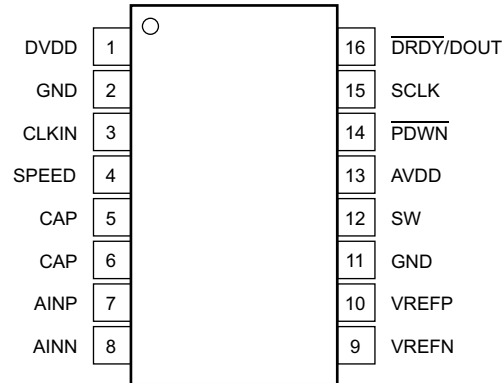
Minimum/maximum limit specifications apply from –40°C to +85°C. Typical specifications at +25°C.

All specifications at AVDD = DVDD = VREFP = +5V, V_{CM} = 2.5V and VREFN = GND, unless otherwise noted.

PARAMETER	CONDITIONS	ADS1231			UNIT
		MIN	TYP	MAX	
POWER SUPPLY					
Power-supply voltage (AVDD, DVDD)		3		5.3	V
Analog supply current	Normal mode, AVDD = 3V		900		μA
	Normal mode, AVDD = 5V		900		μA
	Standby mode		0.1		μA
	Power-down		0.1		μA
Digital supply current	Normal mode, DVDD = 3V		60		μA
	Normal mode, DVDD = 5V		95		μA
	Standby mode, SCLK = high, DVDD = 3V		45		μA
	Standby mode, SCLK = high, DVDD = 5V		65		μA
	Power-down		0.2		μA
Power dissipation, total	Normal mode, AVDD = DVDD = 3V		2.9		mW
	Normal mode, AVDD = DVDD = 5V		5		mW
TEMPERATURE					
Operating temperature range		–40		+85	°C
Specified temperature range		–40		+85	°C

PIN CONFIGURATION

**D PACKAGE
SO-16
(TOP VIEW)**



PIN DESCRIPTIONS

NAME	TERMINAL	ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION	
DVDD	1	Digital	Digital power supply	
GND	2	Supply	Ground for digital and analog supplies	
CLKIN	3	Digital input	External clock input: typically 4.9152MHz. Tie low to activate internal oscillator.	
SPEED	4	Digital input	Data rate select:	
			SPEED	DATA RATE
			0	10SPS
			1	80SPS
CAP	5	Analog	Gain amplifier bypass capacitor connection	
CAP	6	Analog	Gain amplifier bypass capacitor connection	
AINP	7	Analog input	Positive analog input	
AINN	8	Analog input	Negative analog input	
VREFN	9	Analog input	Negative reference input	
VREFP	10	Analog input	Positive reference input	
GND	11	Supply	Ground for digital and analog supplies	
SW	12	Analog	Low-side power switch	
AVDD	13	Supply	Analog power supply	
PDWN	14	Digital input	Power-down: holding this pin low powers down the entire converter and resets the ADC.	
SCLK	15	Digital input	Serial clock: clock out data on the rising edge. Also used to initiate Standby mode. See the Standby Mode section for more details.	
DRDY/DOUT	16	Digital output	Dual-purpose output: Data ready: indicates valid data by going low. Data output: outputs data, MSB first, on the first rising edge of SCLK.	

NOISE PERFORMANCE

The ADS1231 offers outstanding noise performance. [Table 1](#) summarizes the typical noise performance with inputs shorted externally for different data rates and voltage reference values.

The RMS and Peak-to-Peak noise are referred to the input. The effective number of bits (ENOB) is defined as:

$$\text{ENOB} = \ln(\text{FSR}/\text{RMS noise})/\ln(2)$$

The Noise-Free Bits are defined as:

$$\text{Noise-Free Bits} = \ln(\text{FSR}/\text{Peak-to-Peak Noise})/\ln(2)$$

Where:

$$\text{FSR (Full-Scale Range)} = V_{\text{REF}}/\text{Gain}.$$

Table 1. Noise Performance

DATA RATE	AVDD and V _{REF} (V)	RMS NOISE ⁽¹⁾ (nV)	PEAK-TO-PEAK NOISE ⁽¹⁾ (nV)	ENOB (RMS)	NOISE-FREE BITS
10	5	35.2	231.9	20.1	17.4
	3	33.5	199.2	19.4	16.8
80	5	102.1	622.1	18.5	15.9
	3	80.3	549.6	18.2	15.4

(1) Noise specifications are based on direct measurement of 1024 consecutive samples.

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $AV_{DD} = DV_{DD} = REFP = 5\text{V}$, $REFN = \text{GND}$, and $V_{CM} = 2.5\text{V}$ unless otherwise noted.

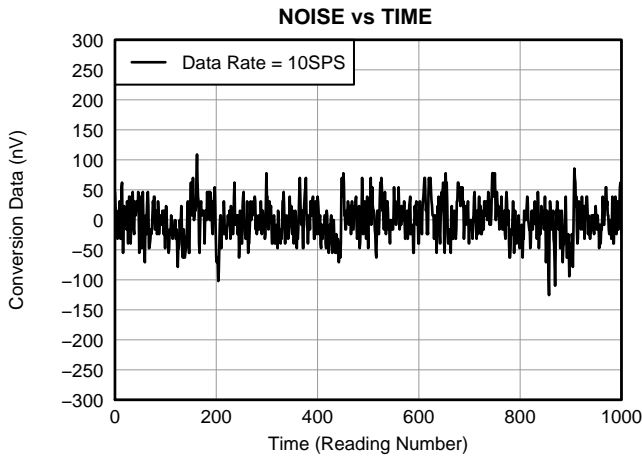


Figure 1.

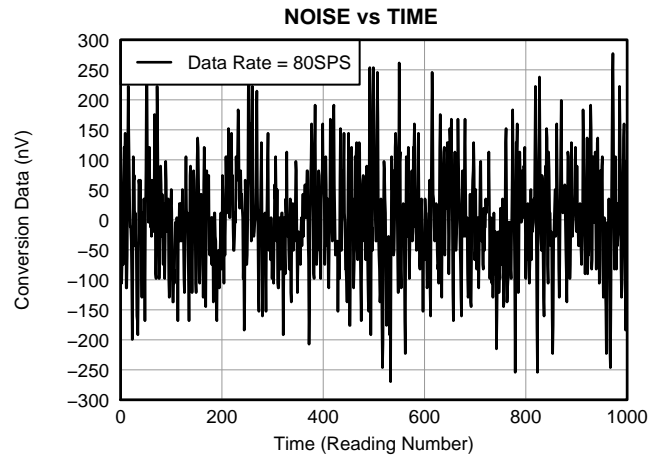


Figure 2.

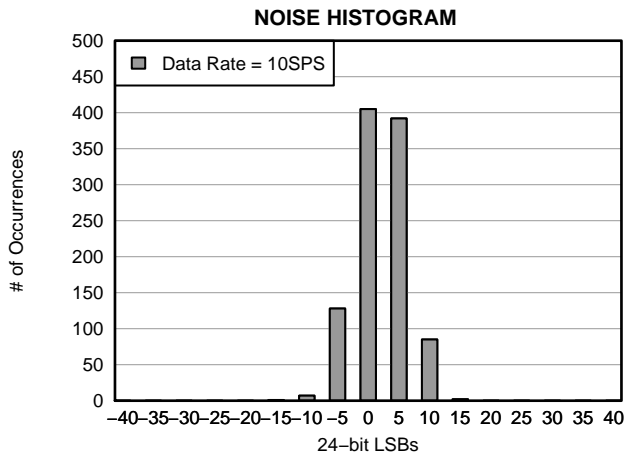


Figure 3.

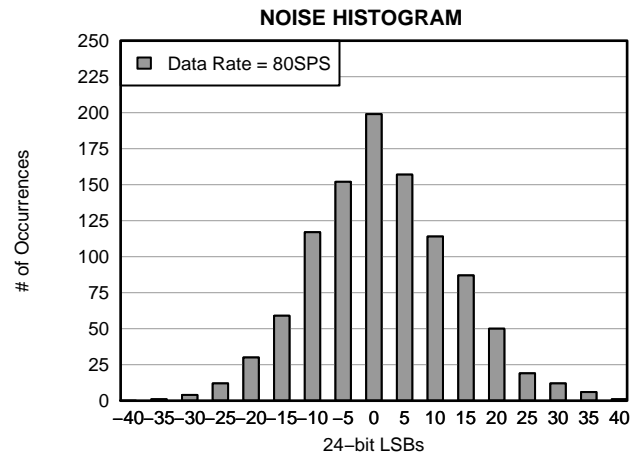


Figure 4.

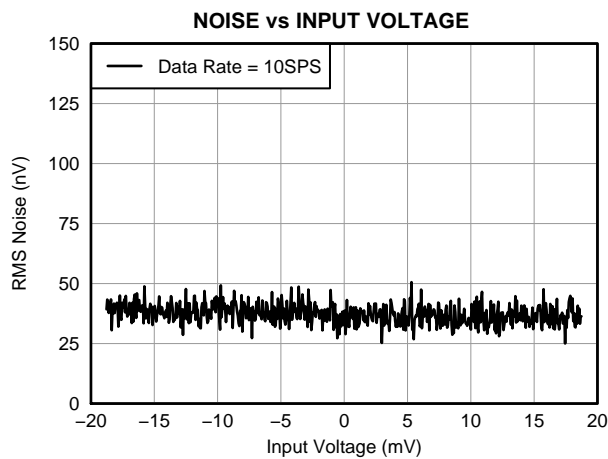


Figure 5.

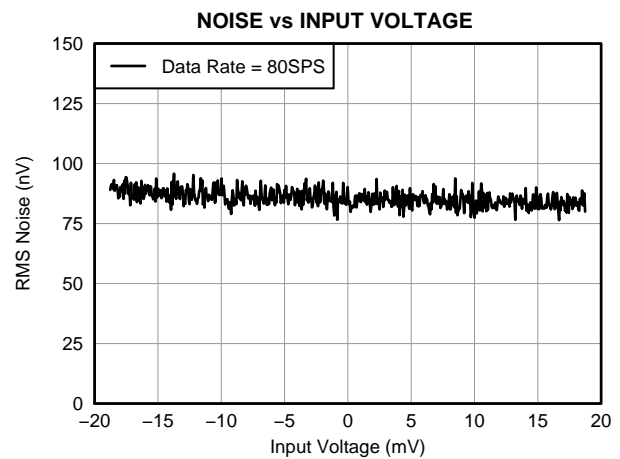


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $AV_{DD} = DV_{DD} = REFP = 5\text{V}$, $REFN = \text{GND}$, and $V_{CM} = 2.5\text{V}$ unless otherwise noted.

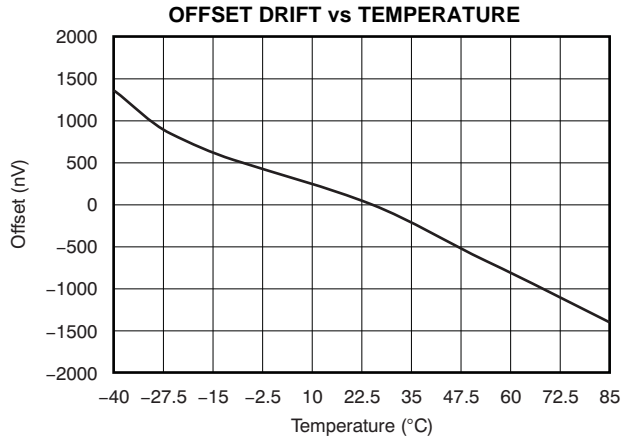


Figure 7.

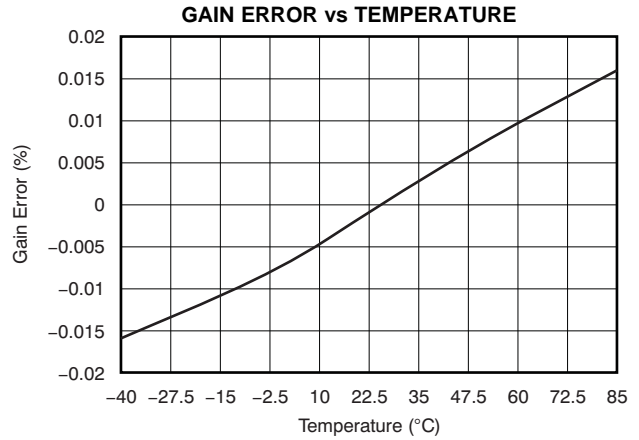


Figure 8.

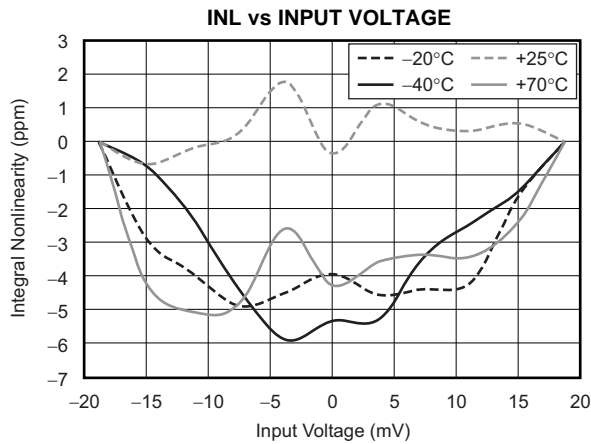


Figure 9.

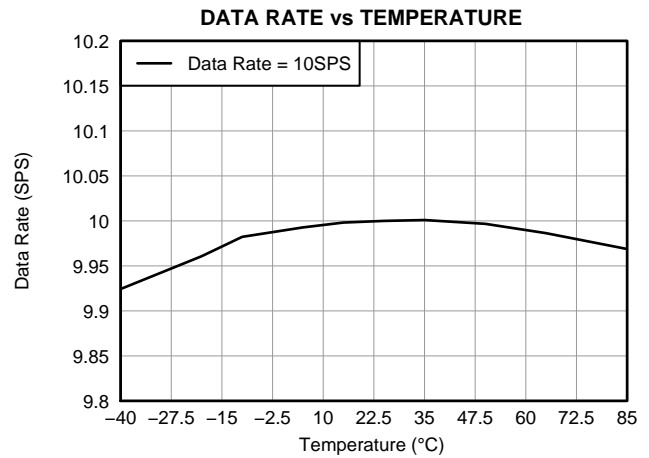


Figure 10.

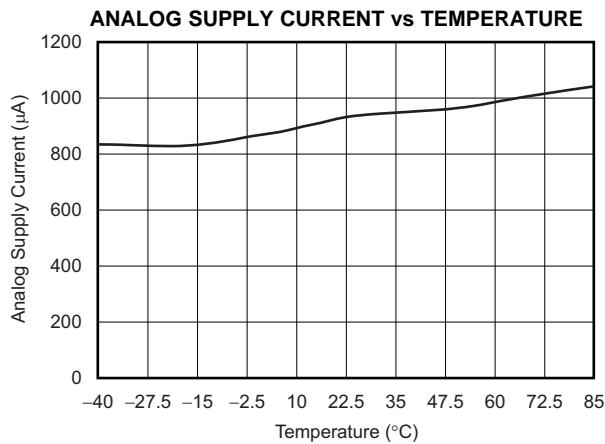


Figure 11.

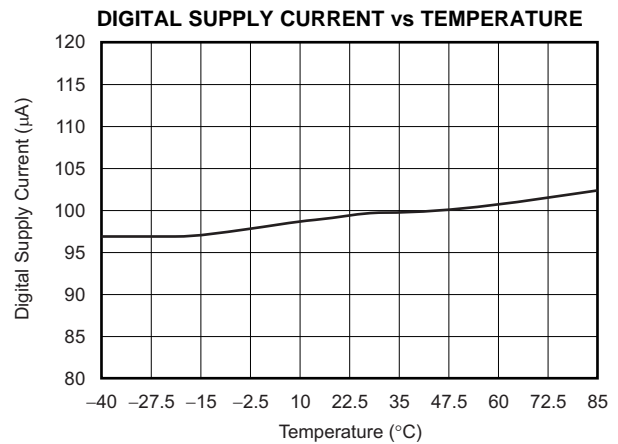


Figure 12.

OVERVIEW

The ADS1231 is a precision, 24-bit ADC that includes a low-noise PGA, internal oscillator, third-order delta-sigma ($\Delta\Sigma$) modulator, and fourth-order digital filter. The ADS1231 provides a complete front-end solution for bridge sensor applications such as weigh scales, strain gauges, and pressure sensors.

Data can be output at 10SPS for excellent 50Hz and 60Hz rejection, or at 80SPS when higher speeds are needed. The ADS1231 is easy to configure, and all digital control is accomplished through dedicated pins; there are no registers to program. A simple two-wire serial interface retrieves the data.

ANALOG INPUTS (AINP, AINN)

The input signal to be measured is applied to the input pins AINP and AINN. The ADS1231 accepts differential input signals, but can also measure unipolar signals.

LOW-NOISE AMPLIFIER

The ADS1231 features a low-drift, low-noise amplifier that provides a complete front-end solution for bridge sensors. A simplified diagram of the amplifier is shown in Figure 13. It consists of two chopper-stabilized amplifiers (A1 and A2) and three accurately matched resistors (R_1 , R_{F1} , and R_{F2}) that construct a differential front-end stage with a gain of 128, followed by gain stage A3 (Gain = 1). The inputs are equipped with an EMI filter, as shown in Figure 13. The cutoff frequency of the EMI filter is 20MHz. By using AVDD as the reference input, the bipolar input ranges from -19.5mV to $+19.5\text{mV}$. The inputs of the ADS1231 are protected with internal diodes connected to the power-supply rails. These diodes clamp the applied signal to prevent it from damaging the input circuitry.

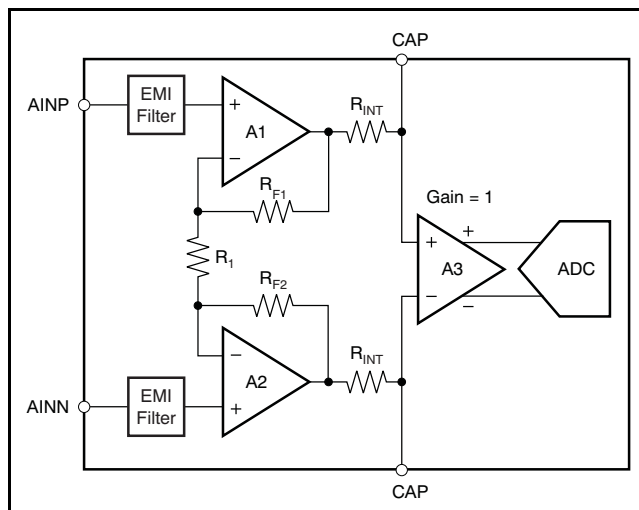


Figure 13. Simplified Diagram of the Amplifier

External Capacitor

An external capacitor (C_{EXT}) across the two ADS1231 CAP pins combines with the internal resistor R_{INT} (on-chip) to create a low-pass filter. The recommended value for C_{EXT} is $0.1\mu\text{F}$ which provides a corner frequency of 720Hz. This low-pass filter serves two purposes. First, the input signal is bandlimited to prevent aliasing by the ADC and to filter out the high-frequency noise. Second, it attenuates the chopping residue from the amplifier to improve temperature drift performance. NPO or C0G capacitors are recommended. For optimal performance, place the external capacitor very close to the CAP pins.

VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference used by the modulator is generated from the voltage difference between VREFP and VREFN: $V_{REF} = V_{REFP} - V_{REFN}$. The reference inputs use a structure similar to that of the analog inputs. In order to increase the reference input impedance, switching buffer circuitry is used to reduce the input equivalent capacitance. The reference drift and noise impact ADC performance. In order to achieve best results, pay close attention to the reference noise and drift specifications. A simplified diagram of the circuitry on the reference inputs is shown in Figure 14. The switches and capacitors can be modeled approximately using an effective impedance of $Z_{EFF} = 500\text{M}\Omega$.

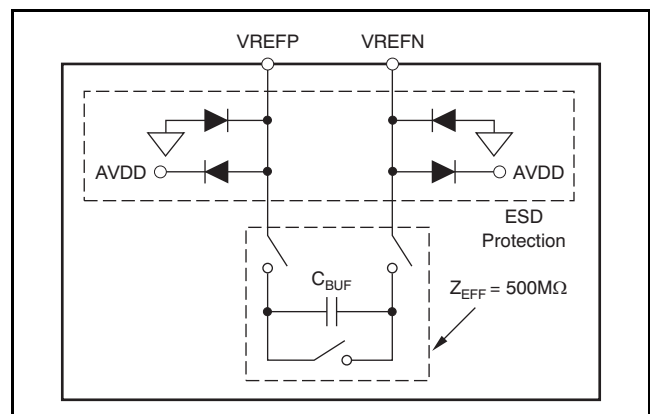


Figure 14. Simplified Reference Input Circuitry

ESD diodes protect the reference inputs. To prevent these diodes from turning on, make sure the voltages on the reference pins do not go below GND by more than 100mV, and likewise, do not exceed AVDD by 100mV:

$$\text{GND} - 100\text{mV} < (V_{REFP} \text{ or } V_{REFN}) < \text{AVDD} + 100\text{mV}$$

LOW-SIDE POWER SWITCH (SW)

The ADS1231 incorporates an internal switch for use with an external bridge sensor, as shown in Figure 15. The switch can be used in a return path for the bridge power. By opening the switch, power dissipation in the bridge is eliminated.

The switch is controlled by the ADS1231 conversion status. During normal conversions, the switch is closed (the SW pin is connected to GND). During standby or power-down modes, the switch is opened (the SW pin is high impedance). When using the switch, it is recommended that the negative reference input (VREFN) be connected directly to the bridge ground terminal, as shown in Figure 15 for best performance.

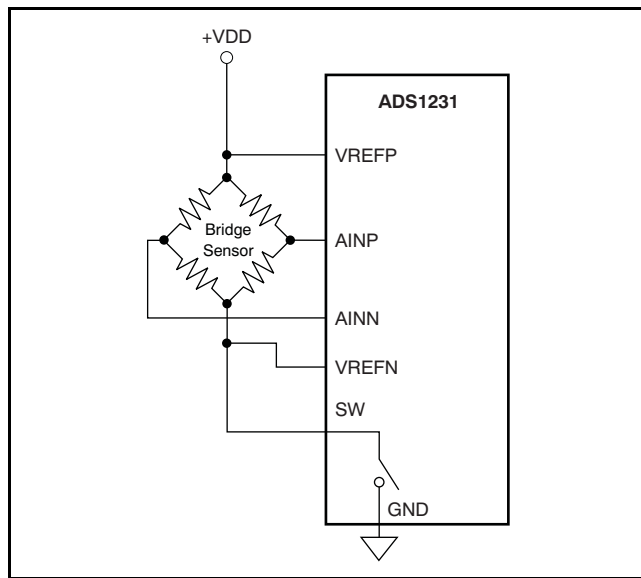


Figure 15. Low-Side Power Switch

CLOCK SOURCE

The ADS1231 can use the internal oscillator or an external clock source to accommodate a wide variety of applications. Figure 16 shows the equivalent circuitry of the clock module. The CLK_DETECT block determines whether an external clock signal is applied to the CLKIN pin so that the internal oscillator is bypassed or activated. When the CLKIN pin frequency is above ~200kHz, the CLK_DETECT circuit shuts down the internal oscillator and passes the external clock signal to the ADC. When the CLKIN pin frequency is below ~200kHz, the CLK_DETECT block activates the internal oscillator. When the internal oscillator is chosen, make sure to connect the CLKIN pin to GND.

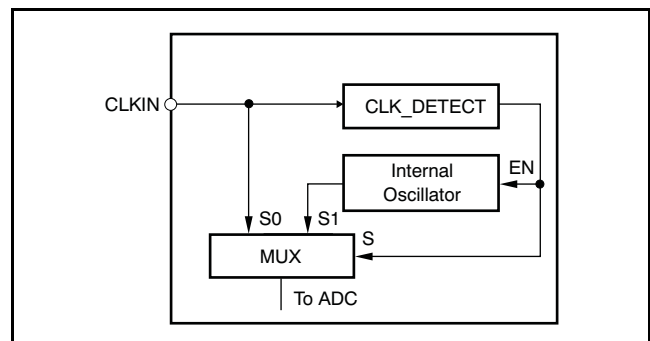


Figure 16. Equivalent Circuitry of the Clock Source

The allowable frequency range for the external clock signal f_{CLKIN} is specified in the Electrical Characteristics table.

FREQUENCY RESPONSE

The ADS1231 uses a sinc⁴ digital filter with the frequency response shown in Figure 17 for $f_{CLKIN} = 4.9152\text{MHz}$. The frequency response repeats at multiples of the modulator sampling frequency of 76.8kHz. The overall response is that of a low-pass filter with a -3dB cutoff frequency of 3.32Hz with the SPEED pin tied low (10SPS data rate) and 11.64Hz with the SPEED pin tied high (80SPS data rate).

To help see the response at lower frequencies, Figure 17(a) illustrates the nominal response out to 100Hz, when the data rate = 10SPS. Notice that signals at multiples of 10Hz are rejected, and therefore simultaneous rejection of 50Hz and 60Hz is achieved.

The benefit of using a sinc⁴ filter is that every frequency notch has four zeros on the same location, thus providing excellent normal-mode rejection of line-cycle interference.

Figure 17(b) zooms in on the 50Hz and 60Hz notches with the SPEED pin tied low (10SPS data rate).

The ADS1231 data rate and frequency response scale directly with clock frequency. For example, if f_{CLKIN} increases from 4.9152MHz to 5.5296MHz when the SPEED pin is tied high, the data rate increases from 80SPS to 90SPS, while the notch also increases from 80Hz to 90Hz. Note that these changes are only possible when an external clock source is applied.

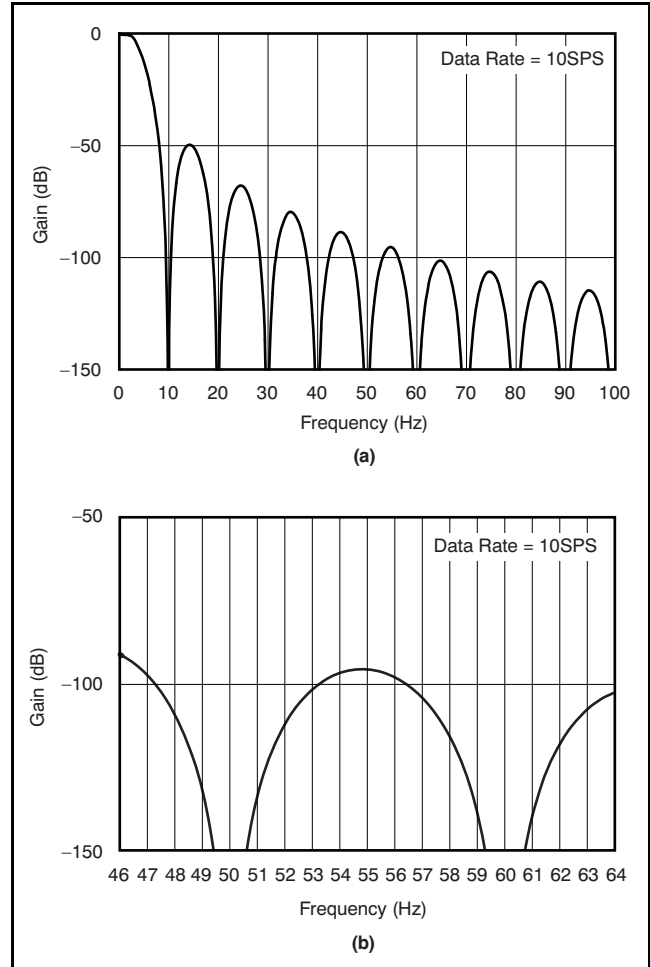


Figure 17. Nominal Frequency Response Out To 100Hz

SETTLING TIME

Fast changes in the input signal require time to settle. For example, an external multiplexer in front of the ADS1231 can generate abrupt changes in input voltage by simply switching the multiplexer input channels. These sorts of changes in the input require four data conversion cycles to settle. When continuously converting, five readings may be necessary in order to settle the data. If the change in input occurs in the middle of the first conversion, four more full conversions of the fully-settled input are required to obtain fully-settled data. Discard the first four readings because they contain only partially-settled data. Figure 18 illustrates the settling time for the ADS1231.

DATA RATE

The ADS1231 data rate is set by the SPEED pin, as shown in Table 2. When SPEED is low, the data rate is nominally 10SPS. This data rate provides the lowest noise, and also has excellent rejection of both 50Hz and 60Hz line-cycle interference. For applications requiring fast data rates, setting SPEED high selects a data rate of nominally 80SPS.

Table 2. Data Rate Settings

SPEED PIN	DATA RATE	
	Internal Oscillator	External Clock
0	10SPS	$f_{CLKIN} / 491,520$
1	80SPS	$f_{CLKIN} / 61,440$

DATA FORMAT

The ADS1231 outputs 24 bits of data in binary two's complement format. The least significant bit (LSB) has a weight of $(0.5V_{REF}/128)(2^{23} - 1)$. The positive full-scale input produces an output code of 7FFFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 3 summarizes the ideal output codes for different input signals.

Table 3. Ideal Output Code vs Input Signal

INPUT SIGNAL V_{IN} (AINP – AINN)	IDEAL OUTPUT
$\geq +0.5V_{REF}/128$	7FFFFFFh
$(+0.5V_{REF}/128)/(2^{23} - 1)$	000001h
0	000000h
$(-0.5V_{REF}/128)/(2^{23} - 1)$	FFFFFFFh
$\leq -0.5V_{REF}/128$	800000h

1. Excludes effects of noise, INL, offset, and gain errors.

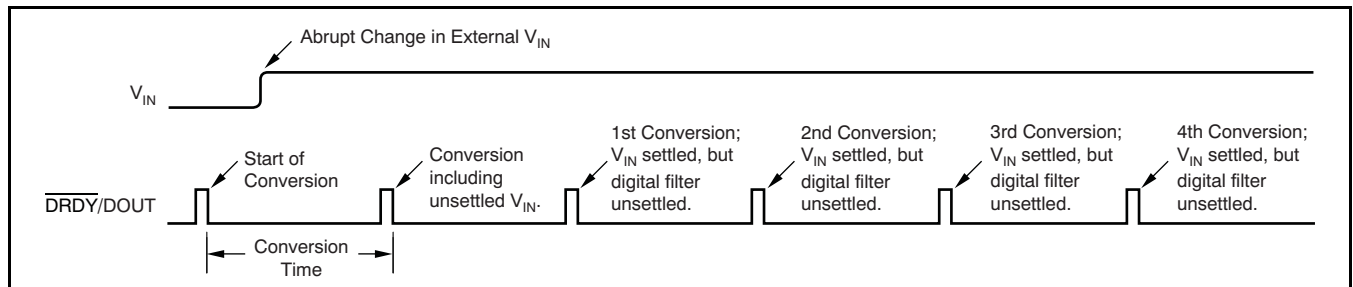


Figure 18. Settling Time in Continuous Conversion Mode

DATA READY/DATA OUTPUT ($\overline{\text{DRDY}}/\text{DOUT}$)

This digital output pin serves two purposes. First, it indicates when new data are ready by going low. Afterwards, on the first rising edge of SCLK, the $\overline{\text{DRDY}}/\text{DOUT}$ pin changes function and begins outputting the conversion data, most significant bit (MSB) first. Data are shifted out on each subsequent SCLK rising edge. After all 24 bits have been retrieved, the pin can be forced high with an additional SCLK. It then stays high until new data are ready. This configuration is useful when polling on the status of $\overline{\text{DRDY}}/\text{DOUT}$ to determine when to begin data retrieval.

SERIAL CLOCK INPUT (SCLK)

This digital input shifts serial data out with each rising edge. This input has built-in hysteresis, but care should still be taken to ensure a clean signal. Glitches or slow-rising signals can cause unwanted additional shifting. For this reason, it is best to make sure the rise and fall times of SCLK are both less than 50ns.

DATA RETRIEVAL

The ADS1231 continuously converts the analog input signal. To retrieve data, wait until $\overline{\text{DRDY}}/\text{DOUT}$ goes low, as shown in Figure 19. After $\overline{\text{DRDY}}/\text{DOUT}$ goes low, begin shifting out the data by applying SCLKs. Data are shifted out MSB first. It is not required to shift out all 24 bits of data, but the data must be retrieved before new data are updated (within t_{CONV}) or else the data will be overwritten. Avoid data retrieval during the update period (t_{UPDATE}). If only 24 SCLKs have been applied, $\overline{\text{DRDY}}/\text{DOUT}$ remains at the state of the last bit shifted out until it is taken high (see t_{UPDATE}), indicating that new data are being updated. To avoid having $\overline{\text{DRDY}}/\text{DOUT}$ remain in the state of the last bit, the 25th SCLK can be applied to force $\overline{\text{DRDY}}/\text{DOUT}$ high, as shown in Figure 20. This technique is useful when a host controlling the device is polling $\overline{\text{DRDY}}/\text{DOUT}$ to determine when data are ready.

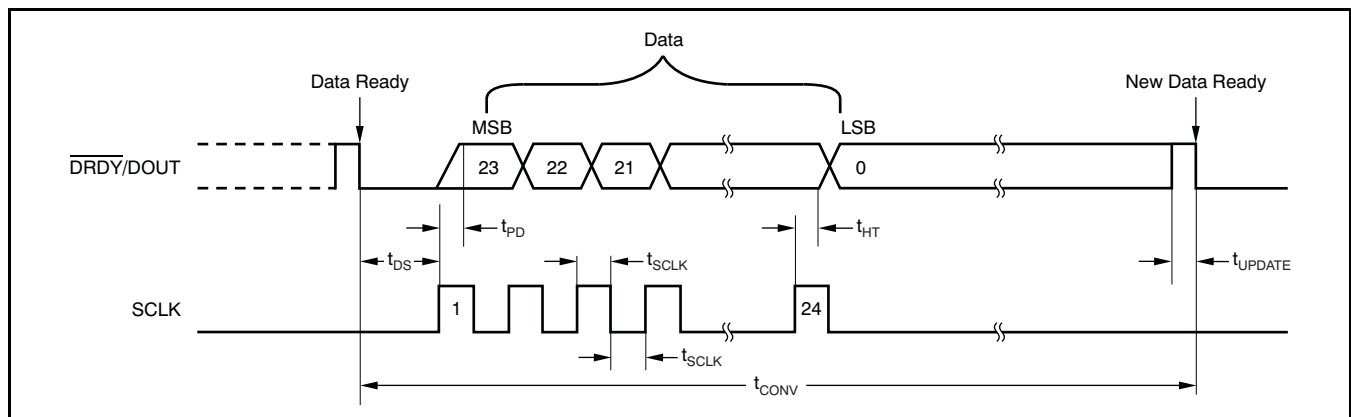


Figure 19. 24-Bit Data Retrieval Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DS}	$\overline{\text{DRDY}}/\text{DOUT}$ low to first SCLK rising edge	0			ns
t_{SCLK}	SCLK positive or negative pulse width	100			ns
$t_{\text{PD}}^{(1)}$	SCLK rising edge to new data bit valid: propagation delay			50	ns
$t_{\text{HT}}^{(1)}$	SCLK rising edge to old data bit valid: hold time	20			ns
t_{UPDATE}	Data updating: no readback allowed		90		μs
t_{CONV}	Conversion time (1/data rate)	SPEED = 1	12.5		ms
		SPEED = 0	100		ms

(1) Minimum required from simulation.

STANDBY MODE

Standby mode dramatically reduces power consumption by shutting down most of the circuitry. To enter Standby mode, simply hold SCLK high after $\overline{\text{DRDY}}/\text{DOUT}$ goes low; see Figure 21. Standby mode can be initiated at any time during readback; it is not necessary to retrieve all 24 bits of data beforehand.

When t_{STANDBY} has passed with SCLK held high, Standby mode activates. $\overline{\text{DRDY}}/\text{DOUT}$ stays high when Standby mode begins. SCLK must remain high to stay in Standby mode. To exit Standby mode (wakeup), set SCLK low. The first data after exiting Standby mode are valid.

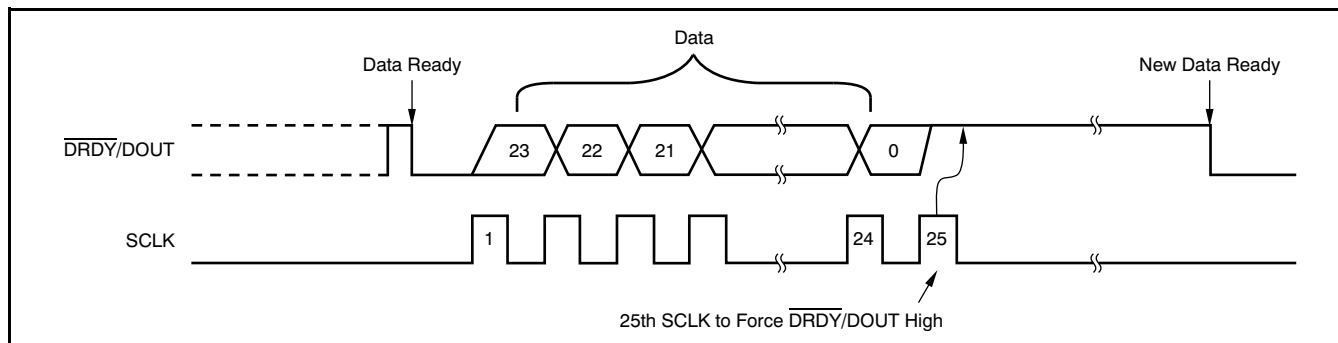


Figure 20. Data Retrieval with $\overline{\text{DRDY}}/\text{DOUT}$ Forced High Afterwards

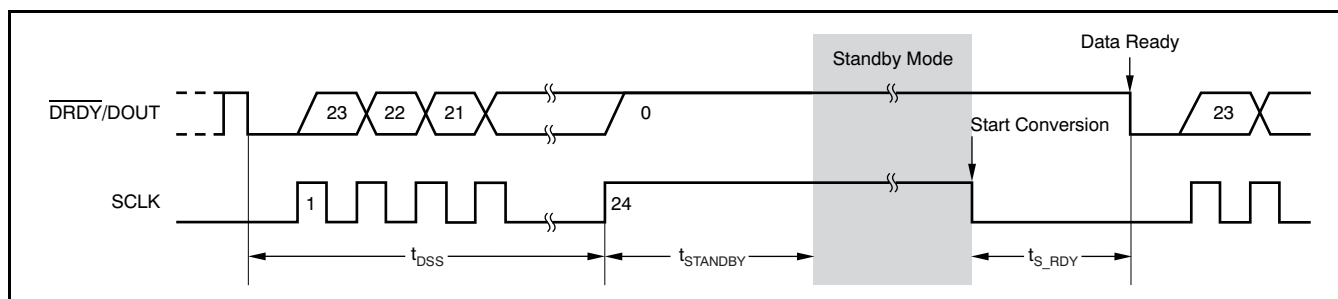


Figure 21. Standby Mode Timing (Can be used for single conversions)

SYMBOL	DESCRIPTION		MIN	TYP	MAX	UNITS
$t_{\text{DSS}}^{(1)}$	SCLK high after $\overline{\text{DRDY}}/\text{DOUT}$ goes low to activate Standby mode	SPEED = 1			12.44	ms
		SPEED = 0			99.94	ms
t_{STANDBY}	Standby mode activation time	SPEED = 1	12.5			ms
		SPEED = 0	100			ms
$t_{\text{S_RDY}}^{(1)}$	Data ready after exiting Standby mode	SPEED = 1		52.6		ms
		SPEED = 0		401.8		ms

(1) Based on an ideal internal oscillator.

POWER-DOWN MODE

Power-Down mode shuts down the entire ADC circuitry and reduces the total power consumption close to zero. To enter Power-Down mode, simply hold the $\overline{\text{PDWN}}$ pin low. Power-Down mode also resets the entire circuitry. Power-Down mode can be initiated at any time during readback; it is not necessary to retrieve all 24 bits of data beforehand. Figure 23 shows the wake-up timing from Power-Down mode.

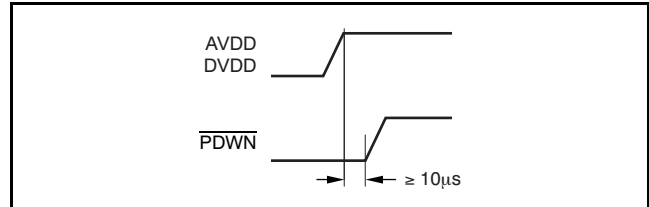


Figure 22. Power-Up Timing Sequence

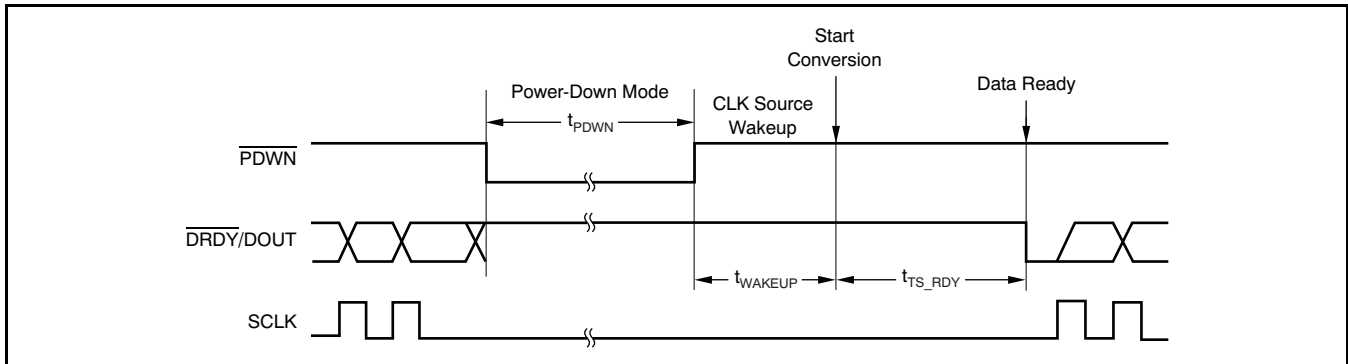


Figure 23. Wake-Up Timing from Power-Down Mode

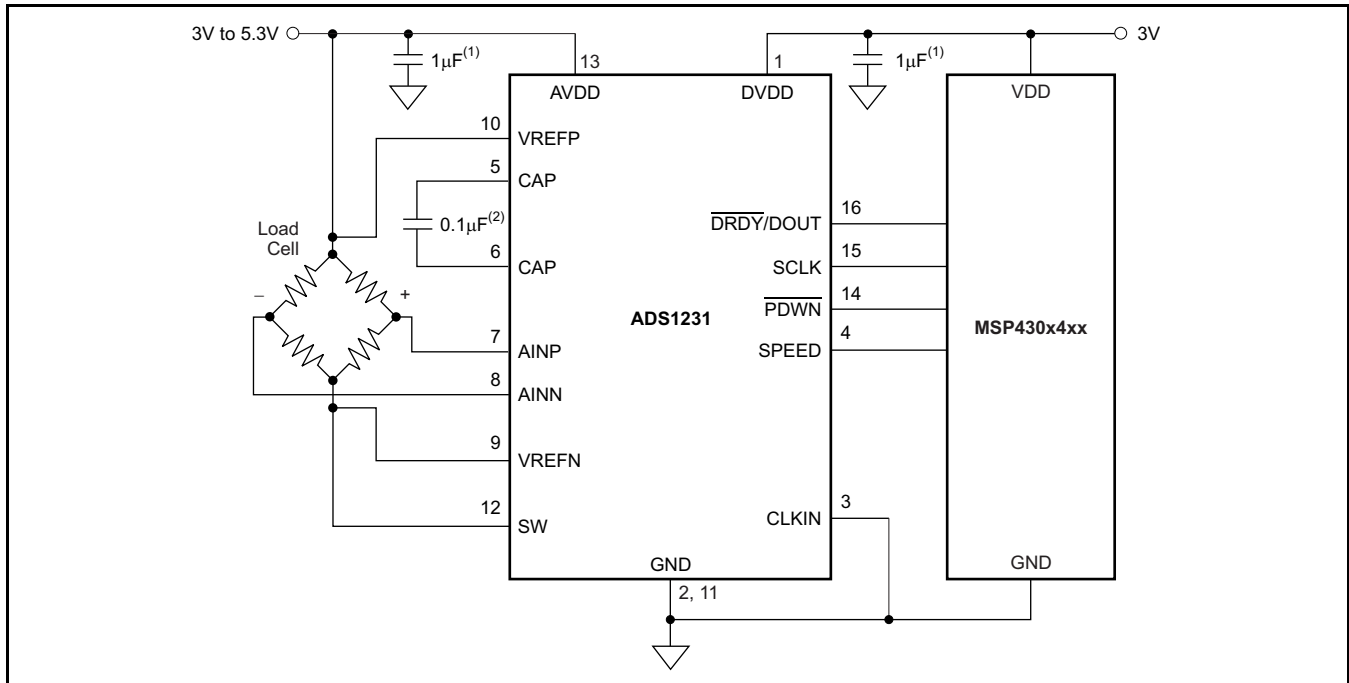
SYMBOL	DESCRIPTION	MIN	TYP	UNITS
$t_{\text{WAKEUP}}^{(1)(2)}$	Wake-up time after Power-Down mode		7.95	μs
$t_{\text{PDWN}}^{(1)}$	$\overline{\text{PDWN}}$ pulse width	26		μs

- (1) Based on an ideal internal oscillator.
 (2) Typical required from simulation.

APPLICATION EXAMPLE

Weigh Scale System

Figure 24 shows a typical ADS1231 application as part of a weigh scale system.



- (1) Place a 0.1µF or higher capacitor as close as possible on both AVDD and DVDD.
- (2) Place capacitor very close to the ADS1231 CAP pins for optimal performance.

Figure 24. Weigh Scale Example

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (December 2010) to Revision D	Page
• Changed "oscillator" to "clock in data rate parameter of electrical characteristics"	3
• Changed all "f _{CLK} " to "f _{CLKIN} " throughout data sheet	3
• Deleted extra space in data rate parameter typical value (typo)	3
• Changed "oscillator" to "clock in data rate parameter of electrical characteristics"	3
• Deleted extra space in data rate parameter typical value (typo)	3
• Changed location of noise parameter	3
• Changed "oscillator" to "clock in normal-mode rejection parameter of electrical characteristics"	3
• Changed "AGND" to "GND" in negative reference input parameter min value	3
• Added new external clock input frequency parameter	3
• Changed "oscillator" to "f _{CLKIN} " in note 2 of electrical characteristics	3
• Changed pin 12 name from PSW to SW in pinout drawing	5
• Changed pin 12 name from PSW to SW in Pin Descriptions table	5
• Changed title of Figure 5	7
• Changed title of Figure 6	7
• Changed plot title and X-axis label of Figure 9	8
• Changed plot title and Y-axis label of Figure 11	8
• Changed plot title and Y-axis label of Figure 12	8
• Changed <i>Clock Source</i> section	10
• Added text to first sentence of <i>Frequency Response</i> section	11
• Changed third paragraph of <i>Frequency Response</i> section	11
• Added new text to end of <i>Frequency Response</i> section	11
• Changed Table 2	12
• Changed pin numbers in Figure 24 to match the device pinout and added missing CLKIN pin	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1231ID	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1231	Samples
ADS1231IDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1231	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1231IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1231IDR	SOIC	D	16	2500	333.2	345.9	28.6

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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