Precision Analog Microcontroller
12-Bit ADCs and DACs, ARM7TDMI® Core

Silicon Anomaly

ADuC7019/ADuC702x

This anomaly list describes the known bugs, anomalies, and workarounds for the ADuC7019/ADuC702x MicroConverter®. The anomalies listed apply to all ADuC7019/ADuC702x packaged material branded as follows:

First Line ADuC7019 or ADuC702x (where: x = 0, 1, 2, 4, 5, 6, 7, 8, 9)

Third Line I31 (revision identifier)
or
Third Line I51 (revision identifier)

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADuC7019/ADuC702x FUNCTIONALITY ISSUES

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
		All silicon branded I31 or I51	Release	Rev. F	4

Rev. F

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ANOMALIES

ADuC7019/ADuC702x Functionality Issues

1. ADC Conversion Start Mode [er017]:

Background:	ADCCON[2:0] allow the user to select one of six ADC conversion start modes of operation, namely: • External pin (P2.0) triggered ADC conversion • Timer1 overflow • Timer0 overflow • Single software conversion • Continuous software conversion • PLA triggered ADC conversion
Issue:	The active-low, external pin (P2.0) triggered conversion is always active, even if it is not selected via ADCCON[2:0]. This is the case if the function of P2.0 is configured as a $\overline{\text{CONV}}_{\text{START}}$ input or if P2.0 is configured as any other function, for example, SOUT, PLAO[5], or GPIO. This means that if a falling edge is seen on P2.0, a single ADC conversion is triggered if ADCCON[7] is enabled. If an ADC conversion cycle is already in progress, this conversion stops, and a new ADC conversion cycle begins in response to a falling edge on P2.0.
Workaround:	Pending.
Related Issues:	ADCCON[7], the ADC enable conversion mode bit, is fully functional, allowing the user to disable any of the active ADC conversion modes except continuous conversion (see the ADuC7019/7020/7021/7022/7024/7025/7026/7027/7028/7029 data sheet).

2. I²C Slave not Releasing the Bus [er021]:

Background:	During a read from the master to the slave, if the slave's FIFO is empty, the slave should NACK the master's request. Then it should release the bus, allowing the master to generate a STOP condition.
Issue:	Following the generation of the NACK, the ADuC702x may not release the bus due to the generation of a FIFO transmit empty interrupt.
Workaround:	Following the generation of a transmit FIFO empty interrupt, the bus may be released by any of the following: Placing valid data in the transmit FIFO. Placing dummy data in the transmit FIFO followed by a transmit FIFO flush. Resetting the slave interface by disabling/enabling the slave.
Related Issues:	None.

3. Access to Flash Address 0x0008F7FF Causes a Data Abort [er022]:

Background:	The ADuC7019/702x devices contain either 32 kB or 62 kB of user accessible Flash memory.
Issue:	On the 62 kB variants of the ADuC7019/702x devices, user accesses to Address 0x0008F7FF causes a data abort exception error to occur.
Workaround:	The last user Flash address byte (0x0008F7FF) should never be accessed by the user code.
Related Issues:	None.

4. Timer3—WDT Secure Clear Bit Feature [er023]:

Background:	Timer3, configured in watchdog timer mode, is clocked from the internal 32 kHz oscillator. This clock is asynchronous to the core clock, which is used to update and read from timer registers. To ensure the value read back from T3VAL is correct, this register should be read twice and if the values differ, a third time. Similarly, to ensure the watchdog timeout period is reset, the user must perform two successive writes to T3CLRI.
Issue:	The secure clear bit feature requires a specific sequential value to be written to T3CLRI. This sequential write cannot be performed when following the recommended procedure to reset the watchdog timeout period (successive write to T3CLRI). Therefore, the secure clear bit feature should not be used.
Workaround:	None.
Related Issues:	None.

SECTION 1. ADuC7019/ADuC702x FUNCTIONALITY ISSUES

Reference Number	Description	Status
er001	External reference	Fixed
er002	ADC wrap around	Fixed
er003	Flash/EE controller	Fixed
er004	Code execution, 1 kB boundary issue	Fixed
er005	Clocking system	Fixed
er006	Wake-up timer operation	Fixed
er007	I^2C transmit FIFO flush operation	Fixed
er008	Use of I^2C in master mode	Fixed
er009	Block interconnection in PLA peripheral	Fixed
er010	Baud rate generation	Fixed
er011	Temperature sensor operation	Fixed
er012	PLA clock source pins	Fixed
er013	ADC power-up time	Feature
er014	PWM sync interrupt	Fixed
er015	Watchdog timer operation	Fixed
er016	External memory bus operation	Fixed
er017	ADC conversion start mode	Open
er018	MMR default values	Fixed
er019	On-chip loader's protection command	Fixed
er020	On-chip loader's write/verify commands	Fixed
er021	I^2C slave not releasing the bus	Open
er022	Access to Flash Address 0x0008F7FF causes a data abort	Open
er023	Timer3—WDT secure clear bit feature	Open

SECTION 2. ADuC7019/ADuC702x PERFORMANCE RELATED ISSUES

Reference Number	Description	Status
pr001	ADC linearity	Fixed
pr002	DAC gain error	Fixed
pr003	Execution speed	Fixed
pr004	Flash retention specification	Fixed

SECTION 3. ADuC7019/ADuC702x SILICON FUTURE ENHANCEMENTS

Reference Number	Description	Status
fe001	I^2C address matching	Fixed
fe002	I^2C start and stop condition identification	Fixed
fe003	External clock input pin	Fixed

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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