Low Power, Precision Analog Microcontroller, Dual Sigma-Delta ADCs

Silicon Anomaly

ADuC7060/ADuC7061

This anomaly list describes the known bugs, anomalies, and workarounds for the ADuC7060/ADuC7061 MicroConverter® Revision D silicon. The anomalies listed apply to all ADuC7060/ADuC7061 packaged material that is branded as follows:

First Line ADuC7060/ADuC7061
Third Line D30 or newer (revision identifier)

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADuC7060/ADuC7061 FUNCTIONALITY ISSUES

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
D	0	All silicon branded D30	Release	Rev. B	6

ADuC7060/ADuC7061 PERFORMANCE ISSUES

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
D	0	All silicon branded D30	Release	Rev. B	0

ADuC7060/ADuC7061 SILICON FUTURE ENHANCEMENTS

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
D	0	All silicon branded D30	Release	Rev. B	0

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FUNCTIONALITY ISSUES

Table 1. External IRQ When Configured as Level Sensitive [er002]

Background	There are four external interrupt sources on the ADuC7060/ADuC7061 parts. These can be configured as edge triggered (rising or falling) or level triggered (active high or active low).
Issue	When any of the external interrupt sources are configured as level triggered, either active high or active low, the external pin must remain at the active level until the program vectors to the interrupt vector handler for that external interrupt. If the external pin is activated, triggering an interrupt, but subsequently goes to an inactive level before the program vectors to the interrupt handler, the appropriate IRQSTA bit for the external interrupt may not be set. This results in the interrupt handler not knowing what interrupt source caused the part to vector to the interrupt vector.
Workaround	Edge triggered interrupts do not have this problem. A fix is pending for this issue.
Related Issues	None.

Table 2. DAC Output Limited to AVDD − 250 mV [er005]

Background	The DAC output range can be configured to four different settings: • 0 V to V_{REF} (1.2 V) range (internal reference source) • VREF− to VREF+ • ADC5/EXT_REF2IN− to ADC4/EXT_REF2IN+ • 0 V to AVDD
Issue	The DAC output buffer is limited in the maximum output voltage in that it can drive to AVDD − 250 mV. This is less than the data sheet specification of AVDD.
Workaround	A fix is pending for this issue.
Related Issues	None.

Table 3. Disabling I^2C Interface in Slave Mode When a Transfer Is in Progress [er006]

Background	Bit 0 (I2CSEN) of the I2CSCON register enables/disables the I^2C slave interface. Bit 6 (I2CBUSY) of the I2CSSTA register indicates if the I^2C slave interface is busy or not.
Issue	If I^2C slave mode is enabled (I2CSCON[0] = 1), and a transfer is in progress with the master, then I2CSCON[0] should not be cleared to 0 to disable the I^2C slave interface until Bit 6 of I2CSSTA (I2CBUSY, the I^2C slave busy status bit) is cleared. When I2CSCON[0] is cleared to 0 and the I^2C slave busy status bit is still set, the ADuC7060/ADuC7061 may drive the SDA pin low indefinitely. When this condition occurs, the ADuC7060/ADuC7061 does not release the SDA unless a hardware reset condition occurs.
Workaround	When disabling I^2C slave mode by writing to I2CSCON[0], first set Bit 0 (I2CMEN) of the I2CMCON register = 1 to enable master mode. Then disable the slave mode by clearing I2CSCON[0]. Finally, clear I2CMCON[0].
Related Issues	None.

Table 4. Operation of SPI in Slave Mode [er007]

Background	When in SPI slave mode, the ADuC7060/ADuC7061 expects the number of clock pulses from the master to be divisible by 8 when the slave chip select pin ($\overline{SS}$) is active. The internal bit shift counter does not reset when the chip select pin is deasserted.
Issue	If the number of clocks from the master is not divisible by 8 when the chip select ($\overline{SS}$) is active, this can result in incorrect data being received or transmitted by the ADuC7060/ADuC7061 because the internal bit shift counter will not be at 0 for subsequent transfers. The internal bit shift counter for the transmit or receive buffers can only be reset by a hardware, software, or watchdog reset condition.
Workaround	Always ensure that the number of SPI clocks are divisible by 8 when the ADuC7060/ADuC7061 chip select ($\overline{SS}$) is active.
Related Issues	None.

Table 5. I²C Slave Not Releasing the Bus [er008]

Background	When an I²C read request happens, if the slave's Tx FIFO is empty, the slave should NACK the masters' request. Then it should release the bus, allowing the master to generate a stop condition.
Issue	If the slave's Tx FIFO is loaded with a byte who's MSB is 0 just on the rising edge of SCL for the ACK/NACK, the slave will pull the SDA low and hold the line until the device is reset.
Workaround	Make sure the Tx FIFO is always loaded on time by preloading Tx FIFO in the preceding Rx interrupt.
Related Issues	None.

Table 6. I²C Clock Stretch Issue [er009]

Background	Clock stretching is a feature that allows a device to halt the I2C bus temporarily by holding SCL low. Bit 6 of the I2CxSCON register enables clock stretching in slave mode. Bit 3 of the I2CxMCON register enables clock stretching in master mode.
Issue	Writing to I2CxSCON Bit 6 or to I2CxMCON Bit 3 on the rising edge of SCL can cause a glitch that may be interpreted by other devices as a real clock edge and might hang the bus.
Workaround	Do not enable clock stretching.
Related Issues	None.

SECTION 1. ADuC7060/ADuC7061 FUNCTIONALITY ISSUES

Reference Number	Description	Status
er001	Power-down mode issue	Fixed on Revision C and later silicon
er002	External IRQ when configured as level sensitive	Open
er003	SPI issue in slave mode when the SPI serial clock phase mode bit (SPICH) is set	Fixed on Revision C and later silicon
er004	Primary ADC self-gain calibration mode	Fixed on Revision C and later silicon
er005	DAC output limited to AVDD – 250 mV	Open
er006	Disabling the I²C interface in slave mode when a transfer is in progress	Open
er007	Operation of SPI in slave mode	Open
er008	I²C slave not releasing the bus	Open
er009	I²C clock stretch issue	Open

SECTION 2. ADuC7060/ADuC7061 PERFORMANCE ISSUES

Reference Number	Description	Status
pr001	DAC relative accuracy when the output range is greater than 0 V to 1.2 V	Fixed on Revision C and later silicon

SECTION 3. ADuC7060/ADuC7061 SILICON FUTURE ENHANCEMENTS

Reference Number	Description	Status
fe001	Primary ADC input buffer bypass	Fixed on Revision C and later silicon

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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