Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management

Preliminary Technical Data

ADuCM4050

FEATURES

Ultra low power active and hibernate modes
- **Active < 40 µA/MHz**
- **Flexi™< 100 µA (typical)**
- **Hibernate < 680 nA (typical)**
- **Shutdown < 50 nA (typical)**
- **Shutdown (Fast wake-up) < 200 nA (typical)**

ARM® Cortex®-M4F processor @ 52 MHz with FPU, MPU, ITM with SWD interface

Power management
- **Single-supply operation (VBAT): 1.74 V to 3.6 V**
- **Optional buck converter for improved efficiency**

Memory options
- **512 KB of embedded flash memory with ECC**
- **4 KB of cache memory to reduce active power**
- **128 KB of configurable system SRAM with parity**

Safety
- **Watchdog with dedicated on-chip oscillator**
- **Hardware CRC with programmable polynomial**
- **Multiparity bit protected SRAM**
- **ECC protected embedded flash**

Security
- **Hardware cryptographic accelerator supporting AES-128, AES-256, and SHA-256**
- **Protected key storage in flash, SHA-256 based keyed HMAC and key wrap and unwrap**
- **User code protection**
- **True random number generator (TRNG)**

DIGITAL PERIPHERALS

3 SPI interfaces with hardware flow control to enable glue-less interface to sensors, radios, and converters
An I^2C and 2 UART peripheral interfaces
SPORT for natively interfacing with converters and radios
Programmable GPIOs (44 in LFCSP and 51 in WLCSP)
3 general-purpose timers with PWM support
RGB timer for driving RGB LED
RTC and FLEX_RTC with SensorStrobe™ and time stamping
Programmable beeper
27-channel DMA controller

CLOCKING FEATURES

26 MHz clock: On-chip oscillator, external crystal oscillator, SYS_CLKIN for external clock
32 kHz clock: On-chip oscillator, low power crystal oscillator
Integrated PLL with programmable divider
Clock fail detection for external crystals

ANALOG PERIPHERALS

12-bit SAR ADC, 1.8 MSPS, 8 channels, digital comparator

APPLICATIONS

Internet of Things (IoT)
- **Smart agriculture, smart building, smart metering, smart city, smart machine, sensor network**

Wearables
- **Fitness and Clinical**

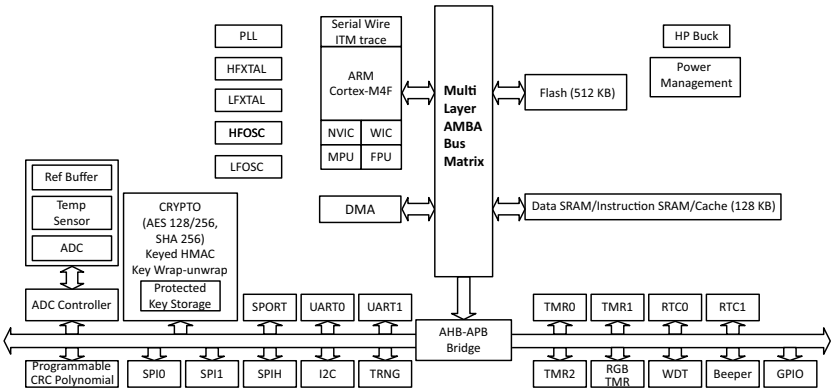

Figure 1. Functional Block Diagram

Rev. PrD **Document Feedback**

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- The ADuCM4050LF EZ-KIT®, Analog Devices, Inc. is an evaluation system for the ADuCM4050 processor.
- The ADuCM4050WL EZ-KIT®, Analog Devices, Inc. is an evaluation system for the ADuCM4050 processor

DOCUMENTATION

Data Sheet

- ADuCM4050: Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Preliminary Data Sheet

Processor Manuals

- ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference

TOOLS AND SIMULATIONS

- ADuCM4050 IBIS Models

REFERENCE MATERIALS

Press

- Analog Devices' Ultralow Power Accelerometer Enables Remote IoT Edge Nodes to Monitor Asset Health
- Ultra Low Power MCU Enables 10 Times System-Level Power Savings and Floating-Point Operation in IoT Applications

DESIGN RESOURCES

- ADuCM4050 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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GENERAL DESCRIPTION

The ADuCM4050 microcontroller unit (MCU) is an ultra low power integrated microcontroller system with integrated power management for processing, control, and connectivity. The MCU system is based on the ARM Cortex-M4F processor. The MCU also has a collection of digital peripherals, embedded SRAM and flash memory, and an analog subsystem which provides clocking, reset, and power management capability in addition to an analog-to-digital converter (ADC) subsystem.

The system features include the following:

- Up to 52 MHz ARM Cortex-M4F processor
- 512 KB of embedded flash memory with error correction code (ECC)
- Optional 4 KB cache for lower active power
- 128 KB system SRAM with parity
- Power management unit (PMU)
- Multilayer advanced microcontroller bus architecture (AMBA) bus matrix
- Central direct memory access (DMA) controller
- Beeper interface
- Crypto hardware supporting advanced encryption standard (AES) -128, AES-256 along with various modes (electronic code book (ECB), cipher block chaining (CBC), counter (CTR), cipher block chaining-message authentication code (CCM/CCM*) modes) and secure hash algorithm (SHA) -256

  Protected key storage with key wrap-unwrap

  Keyed HMAC with key unwrap
- Serial port (SPORT), serial peripheral interface (SPI), inter integrated (I^2C), and universal asynchronous receiver/transmitter (UART) peripheral interfaces
- Real-time clock (RTC)
- General-purpose and watchdog timers
- Programmable general-purpose input/output (GPIO) pins
- Hardware cyclic redundancy check (CRC) calculator with programmable generator polynomial
- Power on reset (POR) and power supply monitor (PSM)
- 12-bit successive approximation register (SAR) ADC
- RGB timer for driving RGB LED
- True random number generator (TRNG)

To support low dynamic and hibernate power management, the ADuCM4050 MCU provides a collection of power modes and features such as dynamic- and software-controlled clock gating and power gating.

For full details on the ADuCM4050 MCU, refer to the *ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference.*

HIGHLIGHTS

The following are the key features of the ADuCM4050 MCU**:**

- Industry leading ultralow power consumption.
- Robust operation.
  - Full voltage monitoring in deep sleep modes.
  - ECC support on flash.
  - Parity error detection on SRAM memory.
  - Leading edge security.
  - Fast encryption provides read protection to customer algorithms.
  - Write protection prevents device reprogramming by unauthorized code.
- Failure detection of 32 kHz LFXTAL via interrupt.
- SensorStrobe for precise time synchronized sampling of external sensors.
  - Works in hibernate mode, resulting in drastic current reduction in system solutions. Current consumption reduces by 10 times when using, for example, the ADXL363 accelerometer.
  - Software intervention is not required after setup.
  - No pulse drift due to software execution.

ARM CORTEX-M4F PROCESSOR

The ARM Cortex-M4F core is a 32-bit reduced instruction set computer (RISC). The length of the data can be 8, 16, or 32 bits. The length of the instruction word is 16 bits or 32 bits.

The processor has the following features:

- Cortex-M4F Architecture
  - Thumb-2 instruction set architecture (ISA) technology
  - 3-stage pipeline with branch speculation
  - Low-latency interrupt processing with tail chaining
  - Single-cycle multiply
  - Hardware divide instructions
  - Nested vectored interrupt controller (NVIC) (72 interrupts and 8 priorities)
  - Six hardware breakpoints and one watchpoint (unlimited software breakpoints using Segger JLink)
  - Bit banding support
  - Trace Support—instruction trace macrocell (ITM), trace port interface unit (TPIU), and data watchpoint and trace (DWT) triggers and counters

- Memory protection unit (MPU)
  - Eight-region MPU with subregions and background region
  - Programmable clock generator unit
- Configurable for ultralow power operation
  - Deep sleep modes, dynamic power management
  - Programmable clock generator unit
- Floating point unit (FPU)
  - Supports single-precision add, subtract, multiply, divide, multiply and accumulate, and square root operations.
  - Provides conversions between fixed point and floating point data formats, and floating point constant instructions.

ARM Cortex-M4F Subsystem

The memory map of the ADuCM4050 MCU is based on the Cortex-M4F model from ARM. By retaining the standardized memory mapping, it is easier to port applications across Cortex-M4F platforms. The ADuCM4050 application development is based on memory blocks across code/SRAM regions. Sufficient internal memory is available via internal SRAM and internal flash.

Code Region

Accesses in this region (0x0000 0000 to 0x0007 FFFF) are performed by the core and target the memory and cache resources.

SRAM Region

Accesses in this region (0x1000_0000 to 0x2005_7FFF) are performed by the ARM Cortex-M4F core. The SRAM region of the core can otherwise act as a data region for an application.

- **Internal SRAM Data Region.** This space can contain read/write data. Internal SRAM can be partitioned between code and data (SRAM region in M4F space) in 32 KB blocks. Access to this region occurs at core clock speed with no wait states. It also supports read/write access by the Cortex-M4F core and read/write DMA access by system devices.
- **System MMRs.** Various system memory mapped registers (MMR) reside in this region.

System Region

Accesses in this region (0xE000 0000 to 0xFFFF FFFF) are performed by the ARM Cortex-M4F core, and are handled within the Cortex-M4F platform.

- **CoreSight™ ROM:** The read only memory (ROM) table entries point to the debug components of the processor.
- **ARM APB Peripheral**. This space is defined by ARM and occupies the bottom 256 KB of the system (SYS) region (0xE000 0000 to 0xE004 0000). The space supports read/write access by the M4F core to the internal peripherals of the ARM core (NVIC, system control space (SCS), wake-up interrupt controller (WIC)) and CoreSight ROM. It is not accessible by system DMA.
- **Platform Control Register**. This space has registers within the Cortex-M4F platform component that control the ARM core, its memory, and the code cache. It is accessible by the Cortex-M4F core (but not accessible by system DMA).

MEMORY ARCHITECTURE

The internal memory of the ADuCM4050 MCU is shown in Figure 2. It incorporates 512 KB of embedded flash memory for program code and nonvolatile data storage, 96 KB of data SRAM, 32 KB of SRAM (configured as instruction space or data space).

SRAM Region

This memory space contains the application instructions and literal (constant) data which must be accessed in real-time. It supports read/write access by the ARM Cortex-M4F core and read/write DMA access by system peripherals. Byte, half-word and word accesses are supported.

SRAM is divided into data SRAM of 96 KB and instruction SRAM of 32 KB. If instruction SRAM is not enabled, then the associated 32 KB can be mapped as data SRAM, resulting in 128 KB of data SRAM.

When the cache controller is enabled, 4 KB of instruction SRAM are reserved as cache memory.

Parity bit error detection (optional) is available on all SRAM memories. Multiple parity bits are associated with each 32-bit word.

In hibernate mode, up to 124 KB of SRAM can be retained in the following ways:

- 124 KB of data SRAM.
- 96 KB of data SRAM and 28 KB of instruction SRAM.

Memory Mapped Registers (Peripheral Control/Status)

For the address space containing memory mapped registers (MMRs), refer to Figure 2. These registers provide control and status for on-chip peripherals of the ADuCM4050 MCU.

For more information about the MMRs, refer to the *ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference*.

Flash Memory

The ADuCM4050 MCU includes 512 KB of embedded flash memory, which is accessed using a flash controller. The flash controller is coupled with a cache controller. A prefetch mechanism is implemented in the flash controller to optimize code performance.

Flash writes are supported by a key hole mechanism via APB writes to MMRs. The flash controller provides support for DMA based key hole writes.

With respect to flash integrity, the device supports the following:

- A fixed user key required for running protected commands, including mass erase and page erase.
- An optional and user definable user failure analysis key (FAA key). Analog Devices personnel need this key while performing failure analysis.
- An optional and user definable write protection for user-accessible memory.
- An optional 8-bit ECC. It is disabled by default.

Cache Controller

The ADuCM4050 MCU has an optional 4 KB instruction cache. In certain applications, enabling the cache and executing the code can result in lower power consumption than operating directly from flash. When the cache controller is enabled, 4 KB of instruction SRAM is reserved as cache memory. In hibernate mode, the cache memory is not retained.

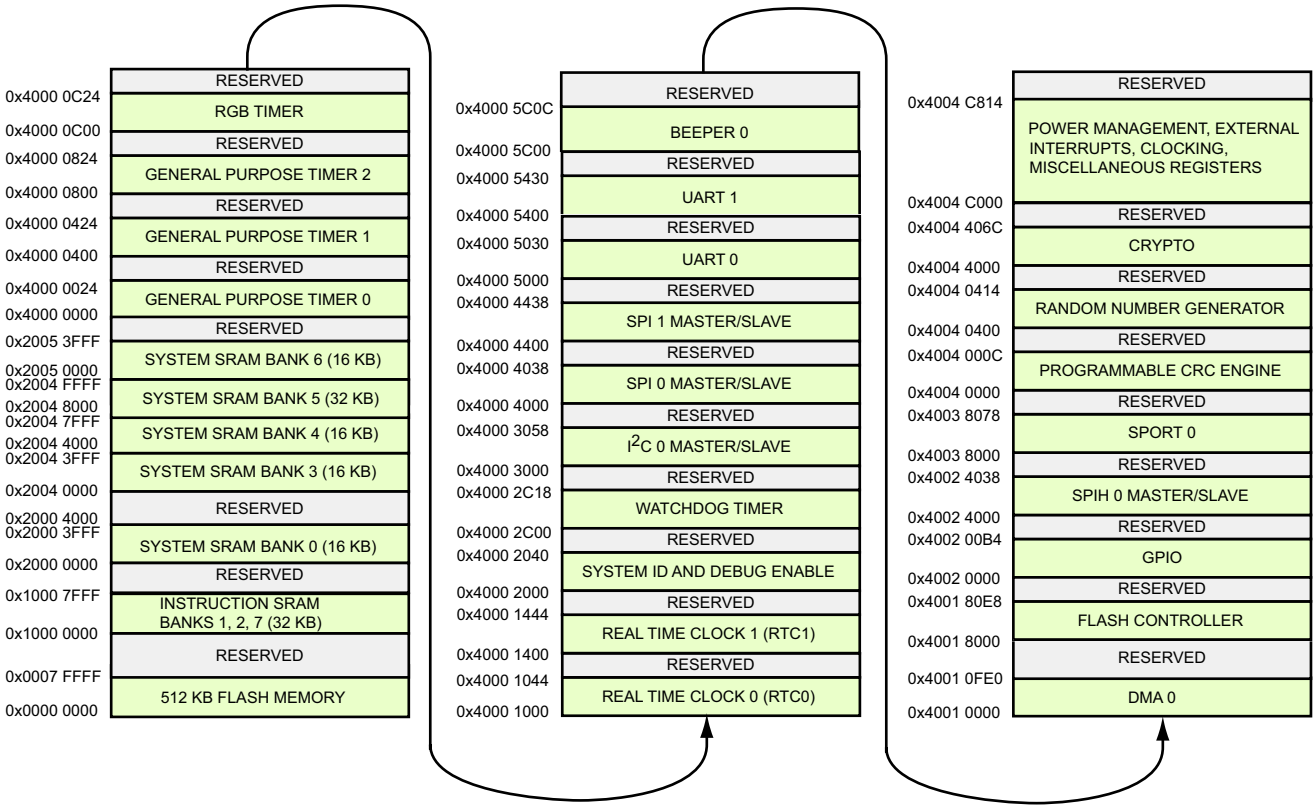


Figure 2. ADuCM4050 Memory Map - SRAM Mode 0

SYSTEM AND INTEGRATION FEATURES

The ADuCM4050 MCU provides several features that ease system integration.

Reset

There are four kinds of resets: external, power-on, watchdog timeout, and software system reset. The software system reset is provided as part of the Cortex-M4F core.

The $\overline{\text{SYS\_HWRST}}$ pin is toggled to perform a hardware reset.

Booting

The ADuCM4050 MCU supports two boot modes: booting from internal flash and upgrading software through UART download. If the SYS_BMODE0 pin (GPIO17) is pulled low during power-up or a hard reset, the MCU enters into serial download mode. In this mode, an on-chip loader routine is initiated in the kernel, which configures the UART port and communicates with the host to manage the firmware upgrade via a specific serial download protocol.

Table 1. Boot Modes

Boot Mode	Description
0	UART download mode.
1	Flash boot. Boot from integrated flash memory.

Power Management

The ADuCM4050 MCU has an integrated power management system that optimizes performance and extend battery life of the device.

The power management system consists of the following:

- Integrated 1.2 V low dropout regulator (LDO) and optional capacitive buck regulator
- Integrated power switches for low standby current in hibernate and shutdown modes

Additional power management features include the following:

- Customized clock gating for active modes
- Power gating to reduce leakage in hibernate/shutdown modes
- Flexible sleep modes
- Shutdown mode with no retention
- Optional high efficiency buck converter to reduce power
- Integrated low power oscillators

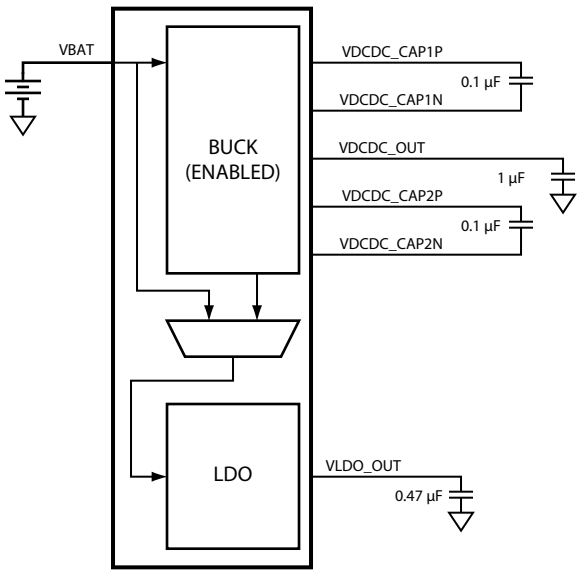
Power Modes

The PMU provides control of the ADuCM4050 MCU power modes and allows the ARM Cortex-M4F to control the clocks and power gating to reduce the power consumption.

Several power modes are available. Each mode provides an additional low power benefit with a corresponding reduction in functionality.

- Active mode. All peripherals can be enabled. Active power is managed by optimized clock management. See Table 3 for details on active mode current consumption.
- Flexi mode. The ARM Cortex-M4F core is clock gated, but the remainder of the system is active. No instructions can be executed in this mode, but DMA transfers can continue between peripherals as well as memory to memory. See Table 4 for details on Flexi mode current consumption.
- Hibernate mode. This mode provides state retention, configurable SRAM and port pin retention, a limited number of wake-up interrupts (SYS_WAKEn, UART0_RX, RTC0, and RTC1), and (optionally) two RTCs—RTC0 and RTC1 (FLEX_RTC).
- Shutdown mode. This mode is the deepest sleep mode, in which all the digital and analog circuits are powered down with an option to wake from four possible wake-up sources. The RTC0 can be (optionally) enabled in this mode, and the device can be periodically woken up by the RTC0 interrupt.
  Shutdown wake-up time is around 76 ms.
  Target power consumption < 50 nA (typical).
- Shutdown mode - Fast wake-up. This mode has a faster wake-up time than shutdown mode.
  Shutdown Fast wake-up time < 1.5 ms.
  Target power consumption < 200 nA.

  See Table 5 for deep sleep modes specifications.



Note: For designs in which the optional buck is not used, the following pins must be left unconnected—VDCDC_CAP1P, VDCDC_CAP1N, VDCDC_OUT, VDCDC_CAP2P, and VDCDC_CAP2N.

Figure 3. Buck Enabled Design

The following features are available for power management and control:

- Voltage range of 1.74 V to 3.6 V, using a single supply (such as the CR2032 coin cell battery).
- GPIOs are driven directly from the battery. The pin state is retained in hibernate and shutdown modes.The GPIO configuration is only retained in hibernate mode.
- Wake-up from external interrupts (via GPIOs), UART0_RX interrupt, and RTCs for hibernate mode.
- Wake-up from external interrupts (via GPIOs) and RTC0 for shutdown mode.
- Optional high power buck converter for 1.2 V full on support (MCU usage only). See Figure 3 for suggested external circuitry.

Security Features

The ADuCM4050 MCU provides a combination of hardware and software protection mechanisms that lock out access to the device in secure mode, but grant access in open mode. These mechanisms include password protected slave boot modes (UART), as well as password protected serial wire debug (SWD) interfaces.

- Mechanisms are provided to protect the device contents (flash, SRAM, CPU registers, and peripheral registers) from being read through an external interface by an unauthorized user. This is referred to as read protection.
- It is possible to protect the device from being reprogrammed in circuit with unauthorized code. This is referred to as in circuit write protection.

CAUTION
This product includes security features that can be used to protect embedded nonvolatile memory contents and prevent execution of unauthorized code. When security is enabled on this device (either by the ordering party or the subsequent receiving parties), the ability of Analog Devices to conduct failure analysis on returned devices is limited. Contact Analog Devices for details on the failure analysis limitations for this device.

The device can be configured with no protection, read protection, or read and in circuit write protection. It is not necessary to provide in circuit write protection without read protection.

Cryptographic Accelerator

The cryptographic accelerator is a 32-bit APB DMA capable peripheral. There are two 128-bit buffers provided for data I/O operations. These buffers read in or read out 128 bits in four data accesses. Big endian and little endian data formats are supported, as are the following modes:

- ECB mode—AES mode
- CTR mode
- CBC mode
- MAC mode
- CCM/CCM* mode
- SHA-256 modes
- Protected key storage with key wrap and unwrap—HMAC signature generation

True Random Number Generator (TRNG)

The TRNG is used during operations where nondeterministic values are required. This may include generating challenges for secure communication or keys used for an encrypted communication channel. The generator can run multiple times to generate a sufficient number of bits for the strength of the intended operation. The true random number generator can seed a deterministic random bit generator.

Reliability and Robustness Features

The ADuCM4050 MCU provides several features that can enhance or help achieve certain levels of system safety and reliability. While the level of safety is mainly dominated by system considerations, the following features are provided to enhance robustness:

- ECC enabled flash memory. The entire flash array can be protected to either correct single-bit errors or detect two-bit errors per 64-bit flash data (disabled by default).
- Multiparity bit protected SRAM. Each word of the SRAM and cache memory is protected by multiple parity bits to allow detection of random soft errors.
- Software watchdog. The on-chip watchdog timer can provide software-based supervision of the ADuCM4050 core.

Cyclic Redundancy Check (CRC) Accelerator

The CRC accelerator computes the CRC for a block of memory locations. The exact memory location can be in the SRAM, flash, or any combination of MMRs. The CRC accelerator generates a checksum that can be compared with an expected signature.

The main features of the CRC include the following:

- Generates a CRC signature for a block of data.
- Supports programmable polynomial length of up to 32 bits.
- Operates on 32 bits of data at a time, and generates CRC for any data length.
- Supports MSB first and LSB first CRC implementations.
- Various data mirroring capabilities.
- Initial seed to be programmed by user.
- DMA controller (memory to memory transfer) used for data transfer to offload the ADuCM4050 MCU.

Programmable GPIOs

The ADuCM4050 MCU has 44 and 51 GPIO pins in the LFCSP and WLCSP packages, respectively, with multiple, configurable functions defined by user code. They can be configured as I/O pins and have programmable pull-up resistors. All GPIO pins are functional over the full supply range.

In deep sleep modes, GPIO pins retain state. On reset, they tristate.

Timers

The ADuCM4050 MCU contains three general-purpose timers, a watchdog timer, and an RGB timer.

All timers support event capture feature, where they can take 40 different interrupts.

General-Purpose Timers

The ADuCM4050 MCU has three identical general-purpose timers, each with a 16-bit up/down counter. The up/down counter can be clocked from one of four user selectable clock sources. Any selected clock source can be scaled down using a prescaler of 1, 16, 64, or 256.

Watchdog Timer (WDT)

The WDT is a 16-bit count down timer with a programmable prescaler. The prescaler source is selectable and can be scaled by a factor of 1, 16, or 256. The watchdog timer is clocked by the 32 kHz on-chip oscillator (LFOSC) and used to recover from an illegal software state. The WDT requires periodic servicing to prevent it from forcing a reset or interrupt to the MCU.

RGB Timer

The ADuCM4050 MCU has an RGB Timer that supports a common anode RGB LED. It has a timer counter and three compare registers. It can generate three distinct PWM waveforms on three ports/pins simultaneously so that different colors can be realized on the common anode RGB LED.

When RGB timer is in operation, the other three timers are available for user software.

Analog-to-Digital Converter (ADC) Subsystem

The ADuCM4050 MCU integrates a 12-bit SAR ADC with up to eight external channels. Conversions can be performed in single or autocycle mode. In single mode, the ADC can be configured to convert on a particular channel by selecting one of the channels. Autocycle mode is provided to convert over multiple channels with reduced MCU overhead of sampling and reading individual channel registers. The ADC can also be used for temperature sensing and measuring battery voltage using dedicated channels. Temperature sensing and battery monitoring cannot be included in autocycle mode.

A digital comparator allows an interrupt to be triggered if ADC input is above or below a programmable threshold. The ADC0_VIN0, ADC0_VIN1, ADC0_VIN2, and ADC0_VIN3 can be used with the digital comparator.

The ADC can be used in DMA mode to reduce MCU overhead by moving ADC results directly into SRAM with a single interrupt asserted when the required number of ADC conversions has been completely logged to memory.

The main features of the ADC subsystem include the following:

- 12-bit resolution
- Programmable ADC update rate from 10 KSPS to 1.8 MSPS
- Integrated input mux that supports up to eight channels
- Temperature sensing support
- Battery monitoring support
- Software selectable on-chip reference voltage generation: 1.25 V, 2.5 V, and VBAT
- Software selectable internal or external reference
- Autocycle mode—ability to automatically select a sequence of input channels for conversion
- Multiple conversions over a single or multiple channels can be performed without core interruption
- Averaging function—converted data on single or multiple channels can be averaged up to 256 samples
- Alert function—internal digital comparator for AIN0, ADC0_VIN0, ADC0_VIN1, ADC0_VIN2, and ADC0_VIN3 channels. An interrupt is generated if the digital comparator detects an ADC result above or below a user defined threshold. In addition, up to eight cycles of hysteresis are built in
- Dedicated DMA channel support
- Each channel, including temperature sensor and battery monitoring, has a data register for conversion result

Clocking

The ADuCM4050 MCU has the following clocking options:

- High frequency clocks
  - Internal oscillator—HFOSC (26 MHz)
  - External crystal oscillator—HFXTAL (26 MHz or 16 MHz)
  - GPIO clock in—SYS_CLKIN
  - PLL
- Low frequency clocks
  - Internal oscillator—LFOSC
  - External crystal oscillator—LFXTAL

The clock options have software configurability with the following exceptions:

- HFOSC cannot be disabled when using an internal buck regulator is used.
- LFOSC cannot be disabled even using if LFXTAL.

Clock sources with a frequency greater than 26 MHz can be achieved by using a PLL. The maximum frequency that can be sourced from the PLL is 52 MHz.

When core frequency is greater than 26 MHz, flash wait states must be programmed to 1.

Hibernate mode can be entered and exited seamlessly (PLL is disabled and relock is transparent to user software) when the system frequency is sourced from PLL.

Clock Fail Detection

The LFOSC clock continuously monitors LFXTAL in hibernate, active, and Flexi power modes. If LFXTAL stops running, there is an option to detect and generate an interrupt and/or automatically switch to LFOSC without software intervention.

The HFOSC clock monitors HFXTAL, GPIO clock, and PLL clock. If any of these clocks is used as the system clock, and they fail to toggle, it can be detected through an interrupt. There is also an option to automatically switch to HFOSC.

Real-Time Clock (RTC)

The ADuCM4050 MCU has two RTC blocks, RTC0 and RTC1 (FLEX_RTC). The clock blocks share a low power crystal oscillation circuit that operates in conjunction with a 32,768 Hz external crystal.

The RTC has an alarm that interrupts the core when the programmed alarm value matches the RTC count. The software enables and configures the RTC.

The RTC also has a digital trim capability to allow a positive or negative adjustment to the RTC count at fixed intervals.

The FLEX_RTC supports four SensorStrobe outputs. Using this mechanism, the ADuCM4050 MCU can be used as a programmable clock generator in all power modes, except shutdown mode. In this way, the external sensors can have their timing domains mastered by the ADuC4050 MCU, as the SensorStrobe can output a programmable divider from the FLEX_RTC, which can operate up to a resolution of 30.7 µs. The sensors and microcontroller are in sync, which removes the need for additional resampling of data to time align it.

In the absence of this mechanism,

- The external sensor uses an RC oscillator (~±30% typical variation). The MCU must sample the data and re-sample it on the MCU's time domain before using it.

Or

- The MCU remains in a higher power state and drives each data conversion on the sensor side.

This mechanism allows the ADuCM4050 MCU to be in a lower power state for a long duration and avoids unnecessary data processing which extends the battery life of the end product. The key differences between RTC0 and RTC1 are shown in Table 2.

Table 2. RTC Features

Features	RTC0	RTC1 (FLEX_RTC)
Resolution of time base (prescaling)	Counts time at 1 Hz in units of seconds. Operationally, always prescales to 1 Hz (for example, divide by 32768) and always counts real time in units of seconds.	Can prescale the clock by any power of two from 0 to 15. It can count time in units of any of these 16 possible prescale settings. For example, the clock can be prescaled by 1, 2, 4, 8, …, 16384, or 32768.
Source clock	LFXTAL.	Depending on the low frequency multiplexer (LFMUX) configuration, the RTC is clocked by the LFXTAL or the LFOSC.
Wake-up timer	Wake-up time is specified in units of seconds.	Supports alarm times down to a resolution of 30.7 µs, i.e., where the time is specified down to a specific 32 kHz clock cycle.
Number of alarms	One alarm only. Uses an absolute, nonrepeating alarm time, specified in units of 1 sec.	Two alarms. One absolute alarm time and one periodic alarm, repeating every 60 prescaled time units.
SensorStrobe mechanism	Not available.	Four independent channels with fine control on duty cycle and frequency (0.5 Hz to 16 kHz). SensorStrobe is an alarm function in the RTC which causes an output pulse to be sent via GPIOs to an external device to instruct that device to take a measurement or perform some action at a specific time. SensorStrobe events are scheduled at a specific target time relative to the real-time count of the RTC. SensorStrobe can be enabled in hibernate mode.
Input capture	Not available.	Input capture takes a snapshot of the RTC real-time count when an external device signals an event via a transition on one of the GPIO inputs to the ADuCM4050 MCU. Typically, an input-capture event is triggered by an autonomous measurement or action on such a device, which then signals to the ADuCM4050 MCU that the RTC must take a snapshot of time corresponding to the event. The taking of this snapshot can wake up the ADuCM4050 MCU and cause an interrupt to the CPU. The CPU can subsequently obtain information from the RTC on the exact 32 kHz cycle on which the input capture event occurred.
Input sampling	Not available.	Each SensorStrobe channel has up to three separate GPIO inputs from an external device, which can be sampled based on the output pulse sent to the external device. Each channel can be configured to interrupt the ADuCM4050 MCU when any activity happens on these GPIO inputs from the external device. These inputs can broadcast sensor states such as FIFO full, switch open, and threshold crossed. This feature allows the ADuCM4050 MCU to remain in a low-power state and wakeup to process the data only when a specific programmed sequence from an external device is detected.

Beeper Driver

The ADuCM4050 MCU has an integrated audio driver for a beeper.

The beeper driver module in the ADuCM4050 MCU generates a differential square wave of programmable frequency. It drives an external piezoelectric sound component with two terminals that connect to the differential square wave output.

The beeper driver consists of a module that can deliver frequencies ranging from 8 kHz to ~0.25 kHz. It operates on a fixed independent 32 kHz clock source that is unaffected by changes in system clocks.

It allows programmable tone durations from 4 ms to 1.02 sec in 4 ms increments. Single-tone (pulse) and multitone (sequence) modes provide versatile playback options.

In sequence mode, the beeper can be programmed to play any number of tone pairs from 1 to 254 (2 to 508 tones) or be programmed to play forever (until stopped by the user). Interrupts are available to indicate the start or end of any beep, the end of a sequence, or when the sequence is nearing completion.

Debug Capability

The ADuCM4050 MCU supports 2-wire SWD interface and trace feature via a single-wire viewer port.

ON-CHIP PERIPHERAL FEATURES

The ADuCM4050 MCU contains a rich set of peripherals connected to the core via several concurrent high bandwidth buses, providing flexibility in system configuration as well as excellent overall system performance (see Figure 1).

The ADuCM4050 MCU contains high speed serial ports, an interrupt controller for flexible management of interrupts from the on-chip peripherals or external sources, and power management control functions to tailor the performance and power characteristics of the MCU and system to many application scenarios.

Serial Ports (SPORT)

The ADuCM4050 MCU provides two single direction half SPORTs or one bidirectional full SPORT. The synchronous serial ports provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices such as Analog Devices audio codecs, ADCs, and DACs. The serial ports contain of two data lines, a clock, and a frame sync. The data lines can be programmed to either transmit or receive, and each data line has a dedicated DMA channel.

Serial port data can be automatically transferred to and from on-chip memory/external memory via dedicated DMA channels. The frame sync and clock can be shared. Some of the ADCs/DACs require two control signals for their conversion process. To interface with such devices, SPT0_ACNV and SPT0_BCNV signals are provided. To use this signal, enable the timer enable mode. In this mode, a PWM timer inside the module generates the programmable SPT0_ACNV and SPT0_BCNV signals.

Serial ports operate in two modes:

- Standard DSP serial mode
- Timer enable mode

Serial Peripheral Interface (SPI) Ports

The ADuCM4050 MCU provides three SPIs. SPI is an industry standard, full-duplex, synchronous serial interface that allows eight bits of data to be synchronously transmitted and simultaneously received. Each SPI incorporates two DMA channels that interface with the DMA controller. One DMA channel transmits and the other receives. The SPI on the ADuCM4050 MCU eases interfacing to external serial flash devices.

The SPI features include the following:

- Serial clock phase mode and serial clock polarity mode
- Loopback mode
- Continuous transfer mode
- Wired OR output mode
- Read command mode for half-duplex operation (transmit followed by receive)
- Flow control support
- Multiple $\overline{CS}$ line support
- $\overline{CS}$ software override support
- Support for 3-pin SPI

UART Ports

The ADuCM4050 MCU provides two full-duplex UART ports, which are fully compatible with PC standard UARTs. The UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA supported, asynchronous transfers of serial data. The UART port includes support for five to eight data bits, and none, even, or odd parity. A frame is terminated by one, one and a half, or two stop bits.

I^2C

The ADuCM4050 MCU provides an I^2C bus peripheral that has two pins for data transfer. SCL is a serial clock pin and SDA is a serial data pin. The pins are configured in a wired AND format that allows arbitration in a multimaster system. A master device can be configured to generate the serial clock. The frequency is programmed by the user in the serial clock divisor register. The master channel can operate in fast mode (400 kHz) or standard mode (100 kHz).

DEVELOPMENT SUPPORT

Development support for the ADuCM4050 MCU includes documentation, evaluation hardware, and development software tools.

Documentation

The *ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference* details the functionality of each block on the ADuCM4050 MCU. It includes power management, clocking, memories, peripherals, and AFE.

Hardware

The ADZS-U4050LF-EZKIT® (for 64-lead LFCSP) and ADZS-U4050WL-EZKIT® (for 72-ball WLCSP) are available to prototype sensor configuration with the ADuCM4050 MCU.

Software

The ADZS-U4050LF-EZKIT and ADZS-U4050WL-EZKIT include a complete development and debug environment for the ADuCM4050 MCU. The board support package (BSP) for the ADuCM4050 MCU is provided for the IAR Embedded Workbench for ARM, Keil™, and CrossCore® embedded studio (CCES) environments.

The BSP also includes operating system (OS) aware drivers and example code for all the peripherals on the device.

ADDITIONAL INFORMATION

The following publications that describe the ADuCM4050 MCU can be ordered from any Analog Devices sales office or accessed electronically on the Analog Devices website:

- *ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Hardware Reference*
- *ADuCM4050 Ultra Low Power ARM Cortex-M4F MCU with Integrated Power Management Anomaly List*

This document describes the ARM Cortex-M4F core and memory architecture used on the ADuCM4050 MCU. It does not provide a detailed programming information about the ARM processor. For more information about programming the ARM processor, visit the ARM Infocenter web page.

The applicable documentation for programming the ARM Cortex-M4F processor include the following:

- *ARM Cortex-M4F Devices Generic User Guide*
- *ARM Cortex-M4F Technical Reference Manual*

REFERENCE DESIGNS

The Circuits from the Lab® web page provides the following:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

SECURITY FEATURES DISCLAIMER

To our knowledge, the Security Features, when used in accordance with the data sheet and hardware reference manual specifications, provide a secure method of implementing code and data safeguards. However, Analog Devices does not guarantee that this technology provides absolute security. ACCORDINGLY, ANALOG DEVICES HEREBY DISCLAIMS ANY AND ALL EXPRESS AND IMPLIED WARRANTIES THAT THE SECURITY FEATURES CANNOT BE BREACHED, COMPROMISED, OR OTHERWISE CIRCUMVENTED AND IN NO EVENT SHALL ANALOG DEVICES BE LIABLE FOR ANY LOSS, DAMAGE, DESTRUCTION, OR RELEASE OF DATA, INFORMATION, PHYSICAL PROPERTY, OR INTELLECTUAL PROPERTY.

SPECIFICATIONS

For information about product specifications, contact your Analog Devices, Inc. representative.

OPERATING CONDITIONS

Parameter		Condition	Min	Typ	Max	Unit
V_{BAT}[1,2]	External Battery Supply Voltage		TBD	TBD	TBD	V
V_{IH}	High Level Input Voltage	V_{BAT} = 3.6 V	TBD	TBD	TBD	V
V_{IL}	Low Level Input Voltage	V_{BAT} = 1.74 V	TBD	TBD	TBD	V
V_{BAT_ADC}	ADC Supply Voltage		TBD	TBD	TBD	V
T_J	Junction Temperature	$T_{AMBIENT}$ = −40°C to +85°C	TBD	TBD	TBD	°C

[1] Must remain powered (even if the associated function is not used).
[2] Value applies to VBAT_ANA1,VBAT_ANA2,VBAT_DIG1, and VBAT_DIG2 pins.

ELECTRICAL CHARACTERISTICS

Parameter		Condition	Min	Typ	Max	Unit
V_{OH}[1]	High Level Output Voltage	V_{BAT} = minimum V, I_{OH} = −1.0 mA	TBD	TBD	TBD	V
V_{OL}[1]	Low Level Output Voltage	V_{BAT} = minimum V, I_{OL} = 1.0 mA	TBD	TBD	TBD	V
I_{IHPU}[2]	High Level Input Current Pull-Up	V_{BAT} = maximum V, V_{IN} = maximum V_{BAT}	TBD	TBD	TBD	µA
I_{ILPU}[2]	Low Level Input Current Pull-Up	V_{BAT} = maximum V, V_{IN} = 0 V	TBD	TBD	TBD	µA
I_{OZH}[3]	Three-State Leakage Current	V_{BAT} = maximum V, V_{IN} = maximum V_{BAT}	TBD	TBD	TBD	µA
I_{OZL}[3]	Three-State Leakage Current	V_{BAT} = maximum V, V_{IN} = 0 V	TBD	TBD	TBD	µA
I_{OZLPU}[4]	Three-State Leakage Current Pull-Up	V_{BAT} = maximum V, V_{IN} = 0 V	TBD	TBD	TBD	µA
I_{OZHPU}[4]	Three-State Leakage Current Pull-Up	V_{BAT} = maximum V, V_{IN} = maximum V_{BAT}	TBD	TBD	TBD	µA
I_{OZLPD}[5]	Three-State Leakage Current Pull-Down	V_{BAT} = maximum V, V_{IN} = 0 V	TBD	TBD	TBD	µA
I_{OZHPD}[5]	Three-State Leakage Current Pull-Down	V_{BAT} = maximum V, V_{IN} = maximum V_{BAT}	TBD	TBD	TBD	µA
C_{IN}	Input Capacitance	T_J = 25°C	TBD	TBD	TBD	pF

[1] Applies to the output and bidirectional pins: P1_10, P0_10, P0_11, P1_02, P1_03, P1_04, P1_05, P2_01, P0_13, P0_15, P1_00, P1_01, P1_15, P2_00, P0_12, P2_11, P1_06, P1_07, P1_08, P1_09, P0_00, P0_01, P0_02, P0_03, P0_06, P0_07, P2_03, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P0_04, P0_05, P0_14, P2_02, P1_14, P1_13, P1_12, P1_11, P0_08, and P0_09
[2] Applies to the input pin with pull-up: $\overline{\text{SYS\_HWRST}}$.
[3] Applies to the three-statable pins: P1_10, P0_10, P0_11, P1_02, P1_03, P1_04, P1_05, P2_01, P0_13, P0_15, P1_00, P1_15, P2_00, P0_12, P2_11, P1_06, P1_07, P1_08, P1_09, P0_00, P0_01, P0_02, P0_03, P2_03, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P0_04, P0_05, P0_14, P2_02, P1_14, P1_13, P1_12, P1_11, P0_08, and P0_09.
[4] Applies to the three-statable pins with pull-ups: P1_10, P0_10, P0_11, P1_02, P1_03, P1_04, P1_05, P2_01, P0_13, P0_15, P1_00, P1_15, P2_00, P0_12, P2_11, P1_06, P1_07, P1_08, P1_09, P0_00, P0_01, P0_02, P0_03, P2_03, P2_04, P2_05, P2_06, P2_07, P2_08, P2_09, P2_10, P0_04, P0_05, P0_14, P2_02, P1_14, P1_13, P1_12, P1_11, P0_08, P0_09, P0_07, and P1_01.
[5] Applies to the three-statable pin with pull-down: P0_06.

Power Supply Current

Table 3. Active Mode—Current Consumption When VBAT = 3.0 V (T_J = 25°C)

Conditions	Buck	Typ	Unit
Code executing from flash, cache disabled, peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz[1]	Disabled	3.32	mA
Code executing from flash, cache disabled, peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz[1]	Disabled	3.58	mA
Code executing from flash, cache disabled, peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz[1]	Enabled	1.85	mA
Code executing from flash, cache disabled, peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz[1]	Enabled	1.98	mA
Code executing from flash, cache enabled, peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz[1]	Disabled	2.30	mA
Code executing from flash, cache enabled, peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz[1]	Disabled	2.55	mA
Code executing from flash, cache enabled, peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz[1]	Enabled	1.26	mA
Code executing from flash, cache enabled, peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz[1]	Enabled	1.43	mA
Code executing from flash, cache disabled, peripheral clocks off, PCLK = 26 MHz, HCLK = 52 MHz[2]	Disabled	5.40	mA
Code executing from flash, cache disabled, peripheral clocks on, PCLK = 26 MHz, HCLK = 52 MHz[2]	Disabled	5.90	mA
Code executing from flash, cache disabled, peripheral clocks off, PCLK = 26 MHz, HCLK = 52 MHz[2]	Enabled	2.89	mA
Code executing from flash, cache disabled, peripheral clocks on, PCLK = 26 MHz, HCLK = 52 MHz[2]	Enabled	3.14	mA
Code executing from flash, cache enabled, peripheral clocks off, PCLK = 26 MHz, HCLK = 52 MHz[2]	Disabled	4.36	mA
Code executing from flash, cache enabled, peripheral clocks on, PCLK = 26 MHz, HCLK = 52 MHz[2]	Disabled	4.85	mA
Code executing from flash, cache enabled, peripheral clocks off, PCLK = 26 MHz, HCLK = 52 MHz[2]	Enabled	2.34	mA
Code executing from flash, cache enabled, peripheral clocks on, PCLK = 26 MHz, HCLK = 52 MHz[2]	Enabled	2.58	mA
Code executing from SRAM, peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz[1]	Disabled	2.63	mA
Code executing from SRAM, peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz[1]	Disabled	2.88	mA
Code executing from SRAM, peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz[1]	Enabled	1.47	mA
Code executing from SRAM, peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz[1]	Enabled	1.60	mA
Code executing from SRAM, peripheral clocks off, PCLK = 26 MHz, HCLK = 52 MHz[2]	Disabled	5.01	mA
Code executing from SRAM, peripheral clocks on, PCLK = 26 MHz, HCLK = 52 MHz[2]	Disabled	5.50	mA
Code executing from SRAM, peripheral clocks off, PCLK = 26 MHz, HCLK = 52 MHz[2]	Enabled	2.66	mA
Code executing from SRAM, peripheral clocks on, PCLK = 26 MHz, HCLK = 52 MHz[2]	Enabled	2.91	mA
Code executing from flash, cache enabled, peripheral clocks off, PCLK = 26 MHz, HCLK = 6.5 MHz[1]	Enabled	0.465	mA

[1] Zero wait states and low HP Buck load.
[2] One wait state and high HP Buck load.

Table 4. Flexi™ Mode—Current Consumption When VBAT = 3.0 V (T_J = 25°C)

Conditions	Buck	Typ	Unit
Peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz	Disabled	593.39	µA
Peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz	Disabled	850.61	µA
Peripheral clocks off, PCLK = 26 MHz, HCLK = 26 MHz	Enabled	364.26	µA
Peripheral clocks on, PCLK = 26 MHz, HCLK = 26 MHz	Enabled	492.83	µA
Peripheral clocks off, PCLK = 26 MHz, HCLK = 52 MHz	Disabled	1114.90	µA
Peripheral clocks on, PCLK = 26 MHz, HCLK = 52 MHz	Disabled	1627.52	µA
Peripheral clocks off, PCLK = 26 MHz, HCLK = 52 MHz	Enabled	625.26	µA
Peripheral clocks on, PCLK = 26 MHz, HCLK = 52 MHz	Enabled	881.64	µA
Peripheral clocks on, PCLK = 26 MHz, HCLK = 812.5 kHz	Enabled	100	µA

Table 5. Deep Sleep Modes[1]—Current Consumption

Mode	Conditions	VBAT	−40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Hibernate	LFXTAL on, RTC0 disabled, RTC1 enabled, 16 KB SRAM retained	1.74 V		0.882			1.097			2.164		µA
	LFXTAL on, RTC0 enabled, RTC1 enabled, 16 KB SRAM retained			0.941			1.152			2.226		µA
	LFXTAL on, RTC0 enabled, RTC1 enabled, 124 KB SRAM retained			1.448			1.986			5.777		µA
Shutdown	LFXTAL on, RTC0 enabled			220			246			410		nA
Fast Shutdown	LFXTAL on, RTC0 enabled			338			379			557		nA
Hibernate	LFXTAL on, RTC0 disabled, RTC1 enabled, 16 KB SRAM retained	3 V		0.661			0.783			1.521		µA
	LFXTAL off, RTC0 disabled, RTC1 enabled, 16 KB SRAM retained						0.72					µA
	LFXTAL off, RTC0 disabled, RTC1 disabled, 16 KB SRAM retained						0.68					µA
	LFXTAL on, RTC0 enabled, RTC1 enabled, 124 KB SRAM retained			0.761			0.885			1.627		µA
	LFXTAL on, RTC0 enabled, RTC1 enabled, 124 KB SRAM retained			1.125			1.412			3.505		µA
Shutdown	LFXTAL on, RTC0 enabled			360			387			604		nA
Fast Shutdown	LFXTAL on, RTC0 enabled			490			532			761		nA
Hibernate	LFXTAL on, RTC0 disabled, RTC1 enabled, 16 KB SRAM retained	3.6 V		0.654			0.767			1.481		µA
	LFXTAL on, RTC0 enabled, RTC1 enabled, 16 KB SRAM retained			0.778			0.888			1.607		µA
	LFXTAL on, RTC0 enabled, RTC1 enabled, 124 KB SRAM retained			1.117			1.372			3.288		µA
Shutdown	LFXTAL on, RTC0 enabled			511			524			792		nA
Fast Shutdown	LFXTAL on, RTC0 enabled			641			673			954		nA

[1] Buck enable/disable selection does not affect power consumption.

SYSTEM CLOCKS/TIMERS

Table 6 and Table 7 show the system clock specifications for the ADuCM4050 MCU.

Platform External Crystal Oscillator

Table 6. Platform External Crystal Oscillator Specifications

Parameter	Min	Typ	Max	Unit	Conditions
LOW FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (LFXTAL)					
$C_{EXT1} = C_{EXT2}$	TBD	TBD	TBD	pF	External capacitor, $C_{EXT1} = C_{EXT2}$ (symmetrical load)
Frequency	TBD	TBD	TBD	Hz	
HIGH FREQUENCY EXTERNAL CRYSTAL OSCILLATOR (HFXTAL)					
$C_{EXT1} = C_{EXT2}$	TBD	TBD	TBD	pF	External capacitor, $C_{EXT1} = C_{EXT2}$ (symmetrical load)
Frequency	TBD	TBD	TBD	MHz	

On-Chip RC Oscillator

Table 7. On-Chip RC Oscillator Specifications

Parameter	Min	Typ	Max	Unit	Conditions
HIGH FREQUENCY RC OSCILLATOR (HFOSC)					
Frequency	TBD	TBD	TBD	MHz	
LOW FREQUENCY RC OSCILLATOR (LFOSC)					
Frequency	TBD	TBD	TBD	Hz	

ADC SPECIFICATIONS

Parameter	Typ	Unit	Conditions
OFFSET ERROR	TBD	LSB	
GAIN ERROR	TBD	LSB	
DIFFERNTIAL LINEARITY ERROR	TBD	LSB	
INTEGRAL LINEARITY ERROR	TBD	LSB	

FLASH SPECIFICATIONS

Parameter	Min	Typ	Max	Unit	Conditions
FLASH					
Endurance	TBD	TBD	TBD	Cycles	
Data Retention	TBD	TBD	TBD	Years	

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 8 may cause permanent damage to the product. This is a stress rating only. Functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 8. Absolute Maximum Ratings

Parameter	Rating
EXTERNAL BATTERY SUPPLY VOLTAGE (V_{BAT})	TBD
DIGITAL INPUT VOLTAGE[1, 2]	TBD
DIGITAL OUTPUT VOLTAGE SWING	TBD
ANALOG INPUT VOLTAGE	TBD
VOLTAGE REFERENCE INPUT VOLTAGE	TBD
STORAGE TEMPERATURE RANGE	TBD
JUNCTION TEMPERATURE (DURING BIAS)	TBD

[1] Applies to 100% transient duty cycle. For other duty cycles, see Table 9.
[2] Applies only when V_{BAT} is within specifications. When V_{BAT} is outside specifications, the range is V_{BAT} ± 0.2 V.

Table 9. Maximum Duty Cycle for Input Transient Voltage[1]

V_{in} Min (V)	V_{in} Max (V)	Maximum Duty Cycle
TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD
TBD	TBD	TBD

[1] Applies to all signal pins with the exception of SYS_CLKIN, SYS_XTAL.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PACKAGE INFORMATION

Table 10 and Figure 4 provides details about package branding. For a complete listing of product availability, see Future (Planned) Products section.

Figure 4. Product Information on Package[1]

[1] Exact brand may differ, depending on package type.

Table 10. Package Brand Information

Brand Key	Field Description
ADuCM4050	Product model
t	Temperature range
pp	Package type
Z	RoHS compliant designation
ccc	See Future (Planned) Products section
vvvvvv.x	Assembly lot code
n.n	Silicon revision
yyww	Date code

TIMING SPECIFICATIONS

Specifications are subject to change without notice.

Reset Timing

Table 11 and Figure 5 describe reset operation.

Table 11. Reset Timing

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{WRST}	$\overline{SYS\_HWRST}$ Asserted Pulse Width Low[1]	TBD	TBD	µs

[1] Applies after power-up sequence is complete.

Figure 5. Reset Timing

System Clock and PLL

Table 12 describes system clock and phase-locked loop (PLL) specifications.

Table 12. System Clock and PLL

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{CK}	PLL Input CLKIN Period[1]	TBD	TBD	ns
t_{CKL}	PLL Input CLKIN Width Low	TBD	TBD	ns
t_{CKH}	PLL Input CLKIN Width High	TBD	TBD	ns
f_{PLL}	PLL Output Frequency[2, 3]	TBD	TBD	MHz
f_{VCO}	VCO Output Frequency[3, 4]	TBD	TBD	MHz
t_{PCLK}	System Peripheral Clock Period	TBD	TBD	ns
t_{HCLK}	Advanced High Performance Bus (AHB) Subsystem Clock Period	TBD	TBD	ns

[1] The input to the PLL can come either from the high frequency external crystal or from the high frequency internal RC oscillator.

[2] For the min value, the recommended settings are PLL_MSEL = 13, PLL_NSEL = 16, PLL_DIV2 = 1 for PLL input clock = 26 MHz; and PLL_MSEL = 13, PLL_NSEL = 26, PLL_DIV2 = 1 for PLL input clock = 16 MHz.

[3] For the max value, the recommended settings are PLL_MSEL = 13, PLL_NSEL = 30, PLL_DIV2 = 0 for PLL input clock = 26 MHz; and PLL_MSEL = 8, PLL_NSEL = 30, PLL_DIV2 = 0 for 16 MHz.

[4] For the min value, the recommended settings are PLL_MSEL = 13, PLL_NSEL = 16 for PLL input clock = 26 MHz; and PLL_MSEL = 13, PLL_NSEL = 26 for PLL input clock = 16 MHz.

Serial Ports

To determine whether communication is possible between two devices at a particular clock speed, the following specifications must be confirmed:

- Frame sync delay and frame sync setup and hold
- Data delay and data setup and hold
- Serial clock (SPT_CLK) width

In Figure 6, the rising edge or falling edge of SPT_CLK (external or internal) can be used as the active sampling edge.

When externally generated, the SPORT clock is called $f_{SPTCLKEXT}$:

$$t_{SPTCLKEXT} = \frac{1}{f_{SPTCLKEXT}}$$

When internally generated, the programmed SPORT clock ($f_{SPTCLKPROG}$) frequency is set by the following equation:

$$f_{SPTCLKPROG} = \frac{f_{PCLK}}{2 \times (CLKDIV + 1)}$$

where CLKDIV is a field in the SPORT_DIV register that can be set from 0 to 65535.

$$t_{SPTCLKPROG} = \frac{1}{f_{SPTCLKPROG}}$$

Table 13. Serial Ports—External Clock

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{SFSE}	Frame Sync Setup Before SPT_CLK (Externally Generated Frame Sync in Transmit or Receive Mode)[1]	TBD	TBD	ns
t_{HFSE}	Frame Sync Hold After SPT_CLK (Externally Generated Frame Sync in Transmit or Receive Mode)[1]	TBD	TBD	ns
t_{SDRE}	Receive Data Setup Before Receive SPT_CLK[1]	TBD	TBD	ns
t_{HDRE}	Receive Data Hold After SPT_CLK[1]	TBD	TBD	ns
t_{SCLKW}	SPT_CLK Width[2]	TBD	TBD	ns
t_{SPTCLK}	SPT_CLK Period[2]	TBD	TBD	ns
SWITCHING CHARACTERISTICS				
t_{DFSE}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[3]	TBD	TBD	ns
t_{HOFSE}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[3]	TBD	TBD	ns
t_{DDTE}	Transmit Data Delay After Transmit SPT_CLK[3]	TBD	TBD	ns
t_{HDTE}	Transmit Data Hold After Transmit SPT_CLK[3]	TBD	TBD	ns

[1] These specifications are referenced to the sample edge.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPT_CLK.
[3] These specifications are referenced to the drive edge.

Table 14. Serial Ports—Internal Clock

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{SDRI}	Receive Data Setup Before SPT_CLK[1]	TBD	TBD	ns
t_{HDRI}	Receive Data Hold After SPT_CLK[1]	TBD	TBD	ns
SWITCHING CHARACTERISTICS				
t_{DFSI}	Frame Sync Delay After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]	TBD	TBD	ns
t_{HOFSI}	Frame Sync Hold After SPT_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[2]	TBD	TBD	ns
t_{DDTI}	Transmit Data Delay After SPT_CLK[2]	TBD	TBD	ns
t_{HDTI}	Transmit Data Hold After SPT_CLK[2]	TBD	TBD	ns
t_{SCLKIW}	SPT_CLK Width	TBD	TBD	ns
t_{SPTCLK}	SPT_CLK Period	TBD	TBD	ns

[1] These specifications are referenced to the sample edge.
[2] These specifications are referenced to the drive edge.

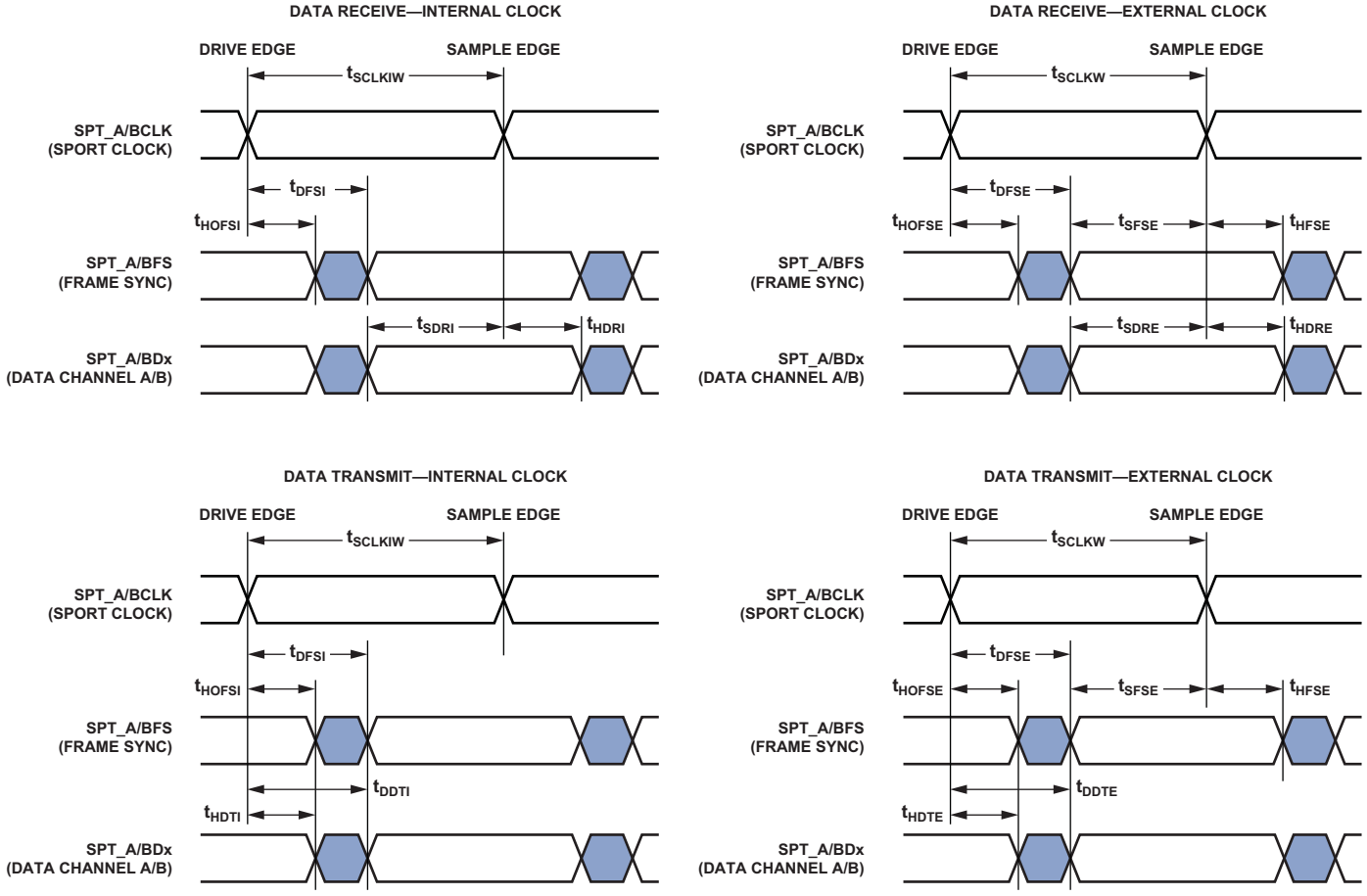


Figure 6. Serial Ports

Table 15. Serial Ports—Enable and Three-State

Parameter		Min	Max	Unit
SWITCHING CHARACTERISTICS				
t_{DDTIN}	Data Enable from Internal Transmit SPT_CLK[1]	TBD	TBD	ns
t_{DDTTI}	Data Disable from Internal Transmit SPT_CLK[1]	TBD	TBD	ns

[1] Referenced to the drive edge.

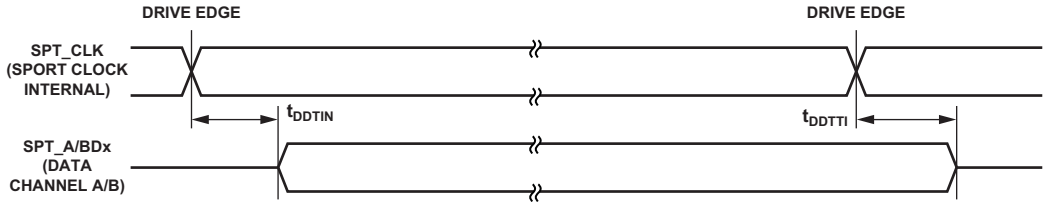


Figure 7. Serial Ports—Enable and Three-State

SPI Timing

Table 16, Figure 8, and Figure 9 (for master mode) and Table 17, Figure 10, and Figure 11 (for slave mode) describe SPI timing specifications. High speed SPI (SPIH) can be used for high data rate peripherals.

Table 16. SPI Master Mode Timing

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{CS}	$\overline{CS}$ to SCLK Edge	TBD	TBD	ns
t_{SL}	SCLK Low Pulse Width	TBD	TBD	ns
t_{SH}	SCLK High Pulse Width	TBD	TBD	ns
t_{DSU}	Data Input Setup Time Before SCLK Edge	TBD	TBD	ns
t_{DHD}	Data Input Hold Time After SCLK Edge	TBD	TBD	ns
SWITCHING CHARACTERISTICS				
t_{DAV}	Data Output Valid After SCLK Edge	TBD	TBD	ns
t_{DOSU}	Data Output Setup Before SCLK Edge	TBD	TBD	ns
t_{SFS}	$\overline{CS}$ High After SCLK Edge	TBD	TBD	ns

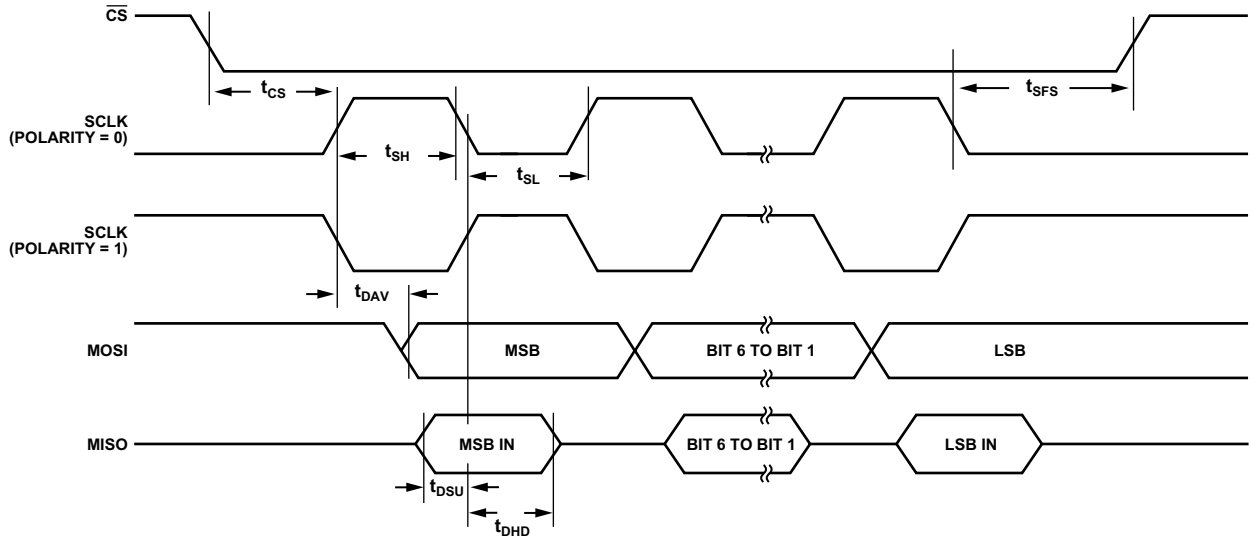


Figure 8. SPI Master Mode Timing (Phase Mode = 1)

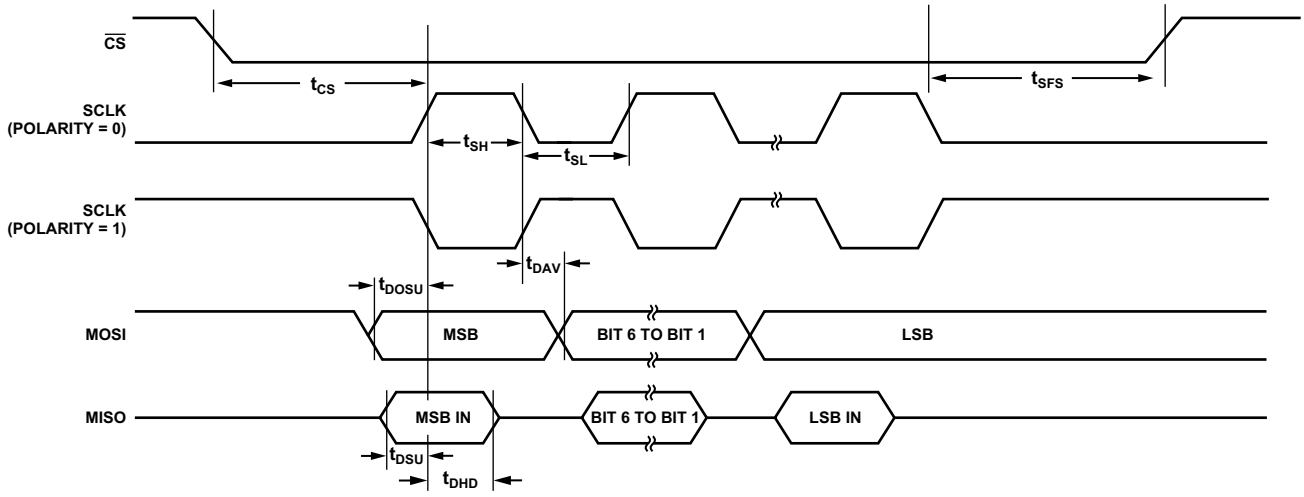


Figure 9. SPI Master Mode Timing (Phase Mode = 0)

Table 17. SPI Slave Mode Timing

Parameter	Description	Min	Max	Unit
TIMING REQUIREMENTS				
t_{CS}	$\overline{CS}$ to SCLK Edge	TBD	TBD	ns
t_{SL}	SCLK Low Pulse Width	TBD	TBD	ns
t_{SH}	SCLK High Pulse Width	TBD	TBD	ns
t_{DSU}	Data Input Setup Time Before SCLK Edge	TBD	TBD	ns
t_{DHD}	Data Input Hold Time After SCLK Edge	TBD	TBD	ns
SWITCHING CHARACTERISTICS				
t_{DAV}	Data Output Valid After SCLK Edge	TBD	TBD	ns
t_{DOCS}	Data Output Valid After $\overline{CS}$ Edge	TBD	TBD	ns
t_{SFS}	$\overline{CS}$ High After SCLK Edge	TBD	TBD	ns

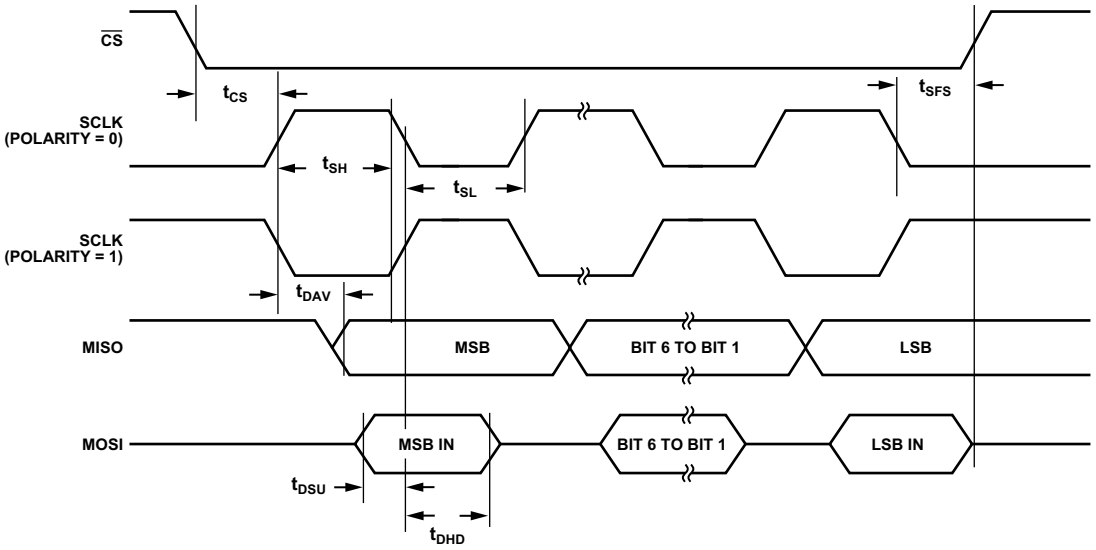


Figure 10. SPI Slave Mode Timing (Phase Mode = 1)

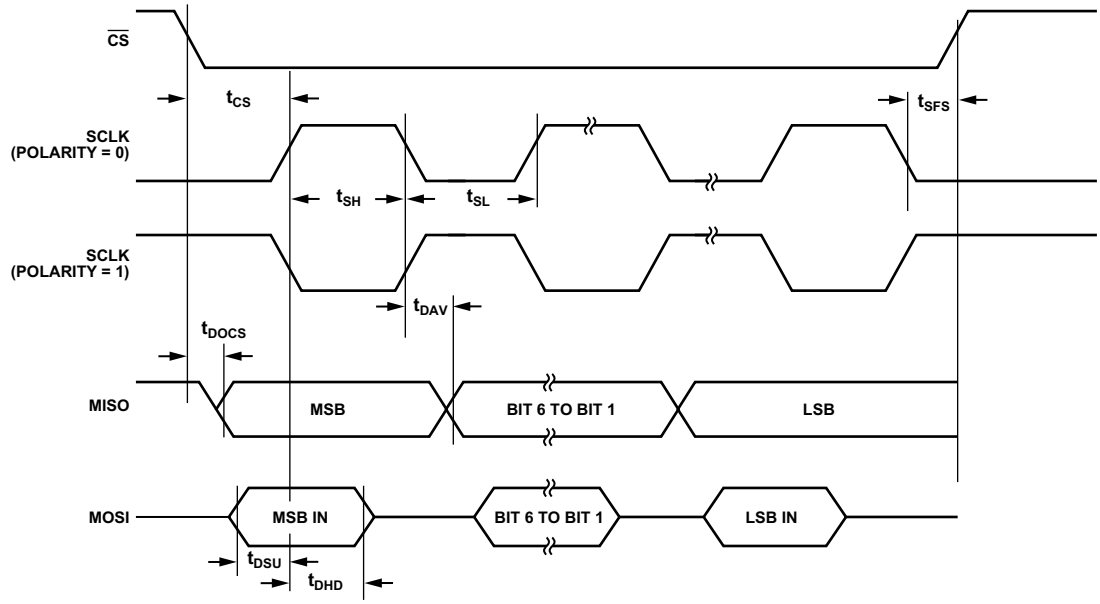


Figure 11. SPI Slave Mode Timing (Phase Mode = 0)

General-Purpose Port Timing

Table 18 and Figure 12 describe general-purpose port operations.

Table 18. General-Purpose Port Timing

Parameter		Min	Max	Unit
TIMING REQUIREMENTS				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	TBD	TBD	ns

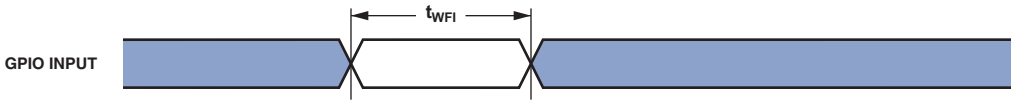


Figure 12. General-Purpose Port Timing

Timer PWM_OUT Cycle Timing

Table 19 and Figure 13 describe timing specifications for PWM_OUT operations.

Table 19. Timer Cycle Timing (Internal Mode)

Parameter		Min	Max	Unit
SWITCHING CHARACTERISTICS				
t_{PWMO}	Timer Pulse Width Output	TBD	TBD	ns

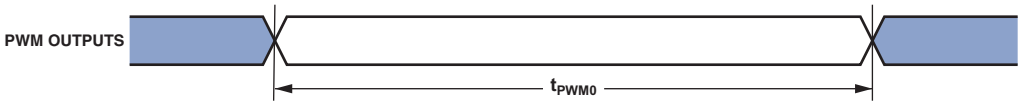


Figure 13. Timer Cycle Timing

MCU TEST CONDITIONS

The ac signal specifications (timing parameters) appearing in this data sheet include output disable time, output enable time, and others. Timing is measured on signals when they cross the V_{MEAS} level as described in Figure 14. All delays (in ns or µs) are measured between the point that the first signal reaches V_{MEAS} and the point that the second signal reaches V_{MEAS}. The value of V_{MEAS} is set to $V_{BAT}/2$.

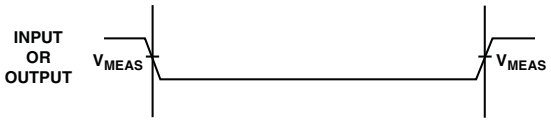
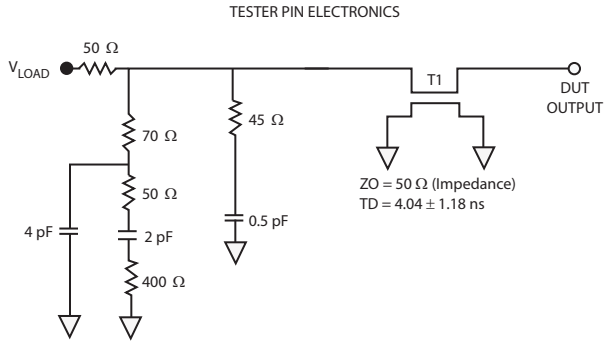


Figure 14. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)



NOTES:
THE WORST CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFELECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, A SYSTEM MAY INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 15. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

OUTPUT DRIVE CURRENTS

Table 20 shows driver types and Figure 16 and Figure 17 show typical current voltage characteristics for the output drivers of the MCU. The curves represent the current drive capability of the output drivers as a function of output voltage.

Table 20. Driver Types (TBD)

Driver Type	Associated Pins
TBD	TBD

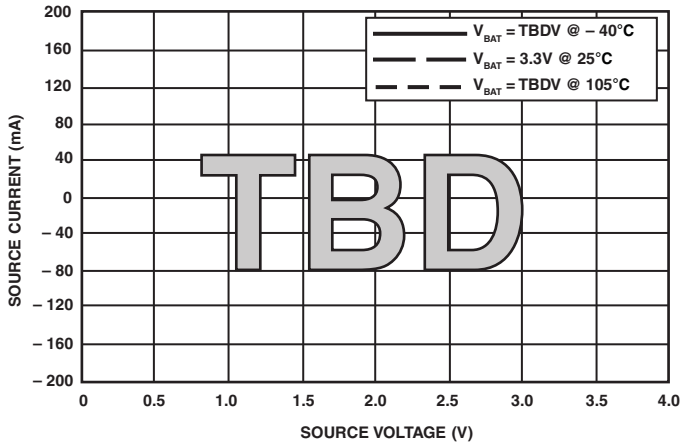


Figure 16. Driver Type A Current

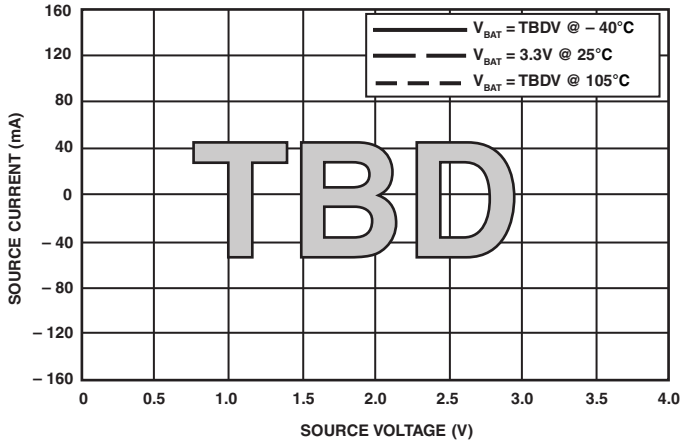


Figure 17. Driver Type B Current

ENVIRONMENTAL CONDITIONS

Table 21. Thermal Characteristics (64-Lead LFCSP)

Parameter	Typ	Unit	Conditions
θ_{JA}	TBD	°C/W	0 linear m/s airflow
θ_{JA}	TBD	°C/W	1 linear m/s airflow
θ_{JA}	TBD	°C/W	2 linear m/s airflow
θ_{JC}	TBD	°C/W	
Ψ_{JT}	TBD	°C/W	0 linear m/s airflow
Ψ_{JT}	TBD	°C/W	1 linear m/s airflow
Ψ_{JT}	TBD	°C/W	2 linear m/s airflow

Values of θ_{JA} are provided for package comparison and printed circuit board (PCB) design considerations.
θ_{JA} can be used for a first-order approximation of T_J by the equation:

$$T_J = T_A + (\theta_{JA} \times P_D)$$

where:
T_A is ambient temperature (°C).
T_J is junction temperature (°C).
P_D is power dissipation (To calculate P_D, see Power Supply Current on Page 14.

Values of θ_{JC} are provided for package comparison and PCB considerations when an external heat sink is required.

The following equation is used to determine the junction temperature on the application PCB:

$$T_J = T_{CASE} + (\Psi_{JT} \times P_D)$$

where:
T_J is junction temperature (°C).
T_{CASE} is case temperature (°C) measured by customer at top center of package.
Ψ_{JT} is obtained from Table 21.
P_D is power dissipation (To calculate P_D, see Power Supply Current on Page 14.

In Table 21, airflow measurements comply with JEDEC standards, JESD51-2 and JESD51-6. The junction to case measurement complies with MIL-STD-883 (Method 1012.1). All measurements use a 2S2P JEDEC test board.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

Figure 18 shows an overview of signal placement on the 72-Ball WLCSP.

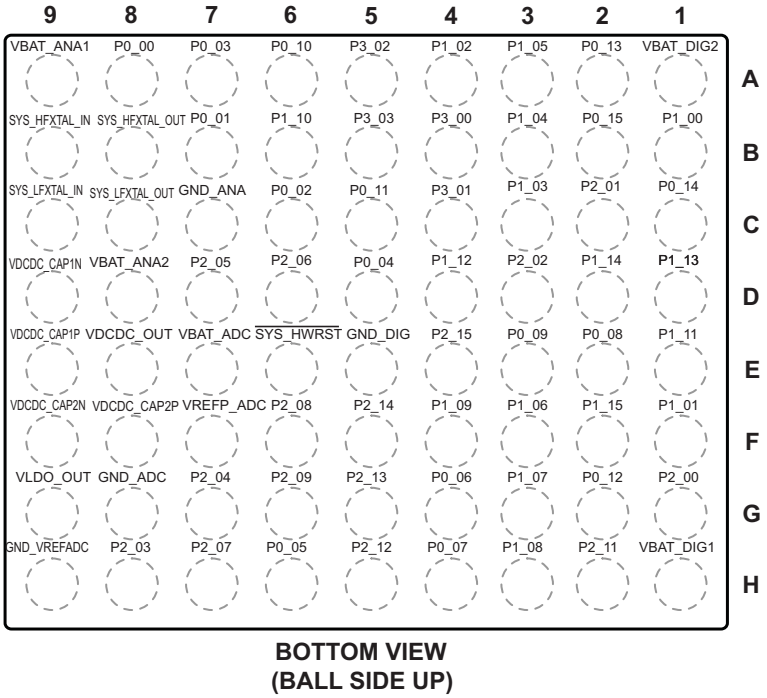


Figure 18. 72-Ball WLCSP Configuration

Table 22 lists the 72-Ball WLCSP package by ball number for the ADuCM4050 MCU.

Table 22. ADuCM4050 72-Ball WLCSP Assignment (Numerical by Ball Number)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
A1	VBAT_DIG2	C7	GND_ANA	F4	P1_09
A2	P0_13	C8	SYS_LFXTAL_OUT	F5	P2_14
A3	P1_05	C9	SYS_LFXTAL_IN	F6	P2_08
A4	P1_02	D1	P1_13	F7	VREFP_ADC
A5	P3_02	D2	P1_14	F8	VDCDC_CAP2P
A6	P0_10	D3	P2_02	F9	VDCDC_CAP2N
A7	P0_03	D4	P1_12	G1	P2_00
A8	P0_00	D5	P0_04	G2	P0_12
A9	VBAT_ANA1	D6	P2_06	G3	P1_07
B1	P1_00	D7	P2_05	G4	P0_06
B2	P0_15	D8	VBAT_ANA2	G5	P2_13
B3	P1_04	D9	VDCDC_CAP1N	G6	P2_09
B4	P3_00	E1	P1_11	G7	P2_04
B5	P3_03	E2	P0_08	G8	GND_ADC
B6	P1_10	E3	P0_09	G9	VLDO_OUT
B7	P0_01	E4	P2_15	H1	VBAT_DIG1
B8	SYS_HFXTAL_OUT	E5	GND_DIG	H2	P2_11
B9	SYS_HFXTAL_IN	E6	$\overline{\text{SYS\_HWRST}}$	H3	P1_08
C1	P0_14	E7	VBAT_ADC	H4	P0_07
C2	P2_01	E8	VDCDC_OUT	H5	P2_12
C3	P1_03	E9	VDCDC_CAP1P	H6	P0_05
C4	P3_01	F1	P1_01	H7	P2_07
C5	P0_11	F2	P1_15	H8	P2_03
C6	P0_02	F3	P1_06	H9	GND_VREFADC

Figure 19 shows an overview of signal placement on the 64-Lead LFCSP_WQ.

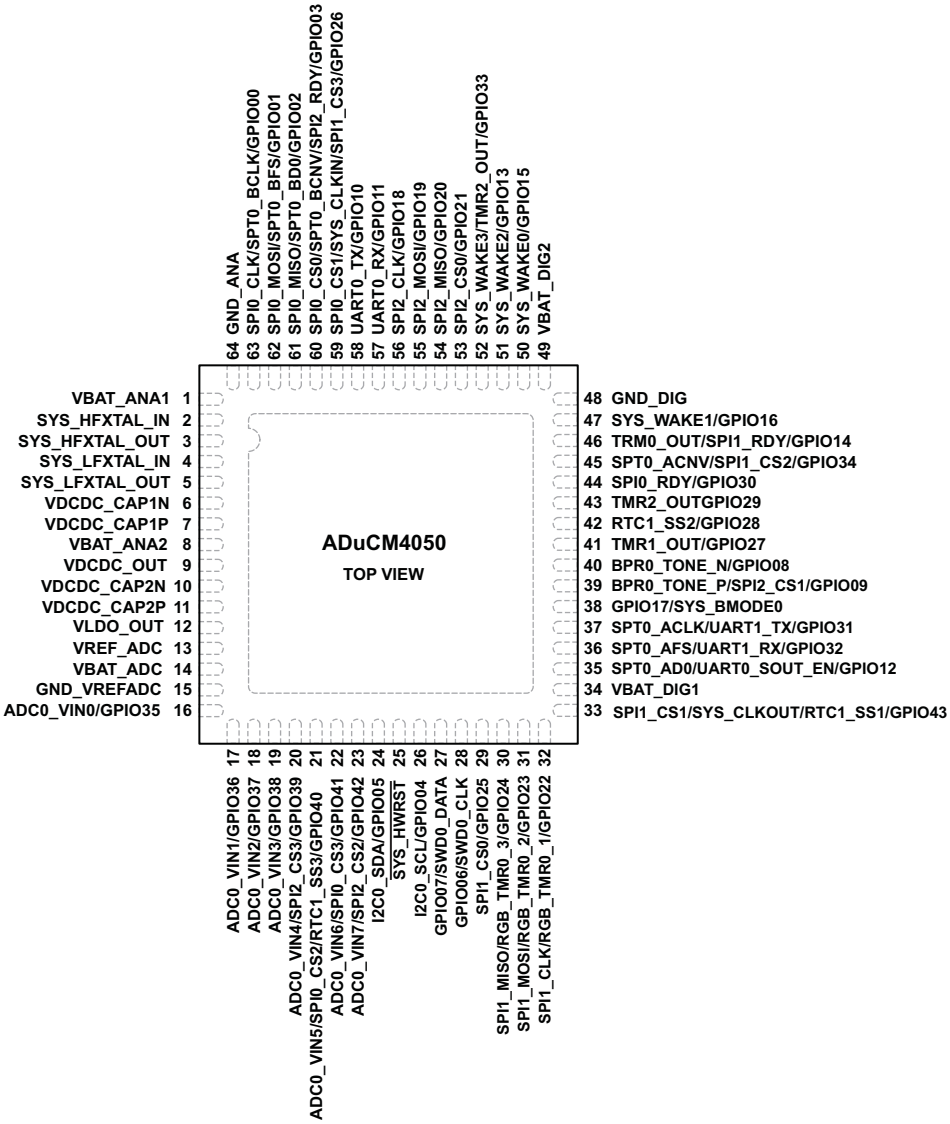


Figure 19. 64-Lead LFCSP Configuration

Table 23 lists the 64-Lead LFCSP package by lead number for the ADuCM4050 MCU.

Table 23. ADuCM4050 64-Lead LFCSP Assignment (Numerical by Lead Number)

Lead No.	Signal	Lead No.	Signal	Lead No.	Signal
1	VBAT_ANA1	23	P2_10	45	P2_02
2	SYS_HFXTAL_IN	24	P0_05	46	P0_14
3	SYS_HFXTAL_OUT	25	$\overline{\text{SYS\_HWRST}}$	47	P1_00
4	SYS_LFXTAL_IN	26	P0_04	48	GND_DIG
5	SYS_LFXTAL_OUT	27	P0_07	49	VBAT_DIG2
6	VDCDC_CAP1N	28	P0_06	50	P0_15
7	VDCDC_CAP1P	29	P1_09	51	P0_13
8	VBAT_ANA2	30	P1_08	52	P2_01
9	VDCDC_OUT	31	P1_07	53	P1_05
10	VDCDC_CAP2N	32	P1_06	54	P1_04
11	VDCDC_CAP2P	33	P2_11	55	P1_03
12	VLDO_OUT	34	VBAT_DIG1	56	P1_02
13	VREFP_ADC	35	P0_12	57	P0_11
14	VBAT_ADC	36	P2_00	58	P0_10
15	GND_VREFADC	37	P1_15	59	P1_10
16	P2_03	38	P1_01	60	P0_03
17	P2_04	39	P0_09	61	P0_02
18	P2_05	40	P0_08	62	P0_01
19	P2_06	41	P1_11	63	P0_00
20	P2_07	42	P1_12	64	GND_ANA
21	P2_08	43	P1_13	Exposed Pad	GND
22	P2_09	44	P1_14		

Table 24 lists the signal descriptions of the ADuCM4050 MCU.

Table 24. Signal Functional Descriptions

GPIO Signal Name	Description
SPIn_CLK	SPI Clock. n= 0, 1, 2.
SPIn_MOSI	SPI Master Out Slave In. n= 0, 1, 2.
SPIn_MISO	SPI Master In Slave Out. n= 0, 1, 2.
SPIn_RDY	SPI Ready Signal. n= 0, 1, 2.
SPIn_CSm	SPI Chip Select Signal. n= 0, 1, 2 and m= 0, 1, 2, 3.
SPT0_ACLK	SPORT A Clock Signal.
SPT0_AFS	SPORT A Frame Sync.
SPT0_AD0	SPORT A Data Pin 0.
SPT0_ACNV	SPORT A Converter Signal for Interface with ADC.
SPT0_BCLK	SPORT B Clock Signal.
SPT0_BFS	SPORT B Frame Sync.
SPT0_BD0	SPORT B Data Pin 0.
SPT0_BCNV	SPORT B Converter Signal for Interface with ADC.
I2C0_SCL	I^2C Clock.
I2C0_SDA	I^2C Data.
SWD0_CLK	Serial Wire Debug Clock.
SWD0_DATA	Serial Wire Debug Data.
BPR0_TONE_N	Beeper Tone Negative Pin.
BPR0_TONE_P	Beeper Tone Positive Pin.
UARTn_TX	UART Transmit Pin. n= 0, 1.
UARTn_RX	UART Receive Pin. n= 0, 1.
UART0_SOUT_EN	UART Serial Data Out Pin.
SYS_WAKEn	System Wake-Up Pin. Wake Up from Flexi/Hibernate/Shutdown Modes[1]. n= 0, 1, 2, 3.
TMRn_OUT	Timer Output Pin. n= 0, 1, 2.
RGB_TMR0_n	RGB Timer Pin. n= 1, 2, 3.
SYS_BMODE0	Boot Mode Pin.
SYS_CLKIN	External Clock In Pin.
SYS_CLKOUT	External Clock Out Pin.
SWV	Serial Wire Viewer
RTC1_SSn	RTC1 SensorStrobe Pin. n= 1, 2, 3, 4.
ADC0_VINn	ADC Voltage Input Pin. n= 0, 1, 2, 3, 4, 5, 6, 7.

[1] For shutdown, SYS_WAKE3 is not capable of waking the device from shutdown mode.

GPIO MULTIPLEXING FOR 72-BALL WLCSP

Table 25. Signal Multiplexing for PORT 0

Signal	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
P0_00	GPIO00	SPI0_CLK	SPT0_BCLK	
P0_01	GPIO01	SPI0_MOSI	SPT0_BFS	
P0_02	GPIO02	SPI0_MISO	SPT0_BD0	
P0_03	GPIO03	SPI0_CS0	SPT0_BCNV	SPI2_RDY
P0_04	GPIO04	I2C0_SCL		
P0_05	GPIO05	I2C0_SDA		
P0_06	SWD0_CLK	GPIO06		
P0_07	SWD0_DATA	GPIO07		
P0_08	GPIO08	BPR0_TONE_N		
P0_09	GPIO09	BPR0_TONE_P	SPI2_CS1	
P0_10	GPIO10	UART0_TX		
P0_11	GPIO11	UART0_RX		
P0_12	GPIO12	SPT0_AD0		UART0_SOUT_EN
P0_13	GPIO13	SYS_WAKE2		
P0_14	GPIO14	TMR0_OUT	SPI1_RDY	
P0_15	GPIO15	SYS_WAKE0		

Table 26. Signal Multiplexing for PORT 1

Signal	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
P1_00	GPIO16	SYS_WAKE1		
P1_01	SYS_BMODE0	GPIO17		
P1_02	GPIO18	SPI2_CLK		
P1_03	GPIO19	SPI2_MOSI		
P1_04	GPIO20	SPI2_MISO		
P1_05	GPIO21	SPI2_CS0		
P1_06	GPIO22	SPI1_CLK		RGB_TMR0_1
P1_07	GPIO23	SPI1_MOSI		RGB_TMR0_2
P1_08	GPIO24	SPI1_MISO		RGB_TMR0_3
P1_09	GPIO25	SPI1_CS0		SWV
P1_10	GPIO26	SPI0_CS1	SYS_CLKIN	SPI1_CS3
P1_11	GPIO27		TMR1_OUT	
P1_12	GPIO28		RTC1_SS2	
P1_13	GPIO29	TMR2_OUT		
P1_14	GPIO30		SPI0_RDY	
P1_15	GPIO31	SPT0_ACLK	UART1_TX	

Table 27. Signal Multiplexing for PORT 2

Signal	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
P2_00	GPIO32	SPT0_AFS	UART1_RX	
P2_01	GPIO33	SYS_WAKE3	TMR2_OUT	
P2_02	GPIO34	SPT0_ACNV	SPI1_CS2	
P2_03	GPIO35	ADC0_VIN0		
P2_04	GPIO36	ADC0_VIN1		
P2_05	GPIO37	ADC0_VIN2		
P2_06	GPIO38	ADC0_VIN3		
P2_07	GPIO39	ADC0_VIN4	SPI2_CS3	
P2_08	GPIO40	ADC0_VIN5	SPI0_CS2	RTC1_SS3
P2_09	GPIO41	ADC0_VIN6	SPI0_CS3	
P2_11	GPIO43	SPI1_CS1	SYS_CLKOUT	RTC1_SS1
P2_12	GPIO44	UART1_TX	SPI2_CS3	
P2_13	GPIO45	UART1_RX	SPI0_CS2	
P2_14	GPIO46	SPI0_CS3		
P2_15	GPIO47	SPI2_CS2	SPI1_CS3	SPI0_CS1

Table 28. Signal Multiplexing for PORT 3

Signal	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
P3_00	GPIO48	RGB_TMR0_1	SPT0_ACLK	
P3_01	GPIO49	RGB_TMR0_2	SPT0_AFS	
P3_02	GPIO50	RGB_TMR0_3	SPT0_AD0	
P3_03	GPIO51	RTC1_SS4	SPT0_ACNV	

GPIO MULTIPLEXING FOR 64-LEAD LFCSP

Table 29. Signal Multiplexing for PORT 0

Signal	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
P0_00	GPIO00	SPI0_CLK	SPT0_BCLK	
P0_01	GPIO01	SPI0_MOSI	SPT0_BFS	
P0_02	GPIO02	SPI0_MISO	SPT0_BD0	
P0_03	GPIO03	SPI0_CS0	SPT0_BCNV	SPI2_RDY
P0_04	GPIO04	I2C0_SCL		
P0_05	GPIO05	I2C0_SDA		
P0_06	SWD0_CLK	GPIO06		
P0_07	SWD0_DATA	GPIO07		
P0_08	GPIO08	BPR0_TONE_N		
P0_09	GPIO09	BPR0_TONE_P	SPI2_CS1	
P0_10	GPIO10	UART0_TX		
P0_11	GPIO11	UART0_RX		
P0_12	GPIO12	SPT0_AD0		UART0_SOUT_EN
P0_13	GPIO13	SYS_WAKE2		
P0_14	GPIO14	TMR0_OUT	SPI1_RDY	
P0_15	GPIO15	SYS_WAKE0		

Table 30. Signal Multiplexing for PORT 1

Signal	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
P1_00	GPIO16	SYS_WAKE1		
P1_01	SYS_BMODE0	GPIO17		
P1_02	GPIO18	SPI2_CLK		
P1_03	GPIO19	SPI2_MOSI		
P1_04	GPIO20	SPI2_MISO		
P1_05	GPIO21	SPI2_CS0		
P1_06	GPIO22	SPI1_CLK		RGB_TMR0_1
P1_07	GPIO23	SPI1_MOSI		RGB_TMR0_2
P1_08	GPIO24	SPI1_MISO		RGB_TMR0_3
P1_09	GPIO25	SPI1_CS0		SWV
P1_10	GPIO26	SPI0_CS1	SYS_CLKIN	SPI1_CS3
P1_11	GPIO27		TMR1_OUT	
P1_12	GPIO28		RTC1_SS2	
P1_13	GPIO29	TMR2_OUT		
P1_14	GPIO30		SPI0_RDY	
P1_15	GPIO31	SPT0_ACLK	UART1_TX	

Table 31. Signal Multiplexing for PORT 2

Signal	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function 3
P2_00	GPIO32	SPT0_AFS	UART1_RX	
P2_01	GPIO33	SYS_WAKE3	TMR2_OUT	
P2_02	GPIO34	SPT0_ACNV	SPI1_CS2	
P2_03	GPIO35	ADC0_VIN0		
P2_04	GPIO36	ADC0_VIN1		
P2_05	GPIO37	ADC0_VIN2		
P2_06	GPIO38	ADC0_VIN3		
P2_07	GPIO39	ADC0_VIN4	SPI2_CS3	
P2_08	GPIO40	ADC0_VIN5	SPI0_CS2	RTC1_SS3
P2_09	GPIO41	ADC0_VIN6	SPI0_CS3	
P2_10	GPIO42	ADC0_VIN7	SPI2_CS2	
P2_11	GPIO43	SPI1_CS1	SYS_CLKOUT	RTC1_SS1

OUTLINE DIMENSIONS

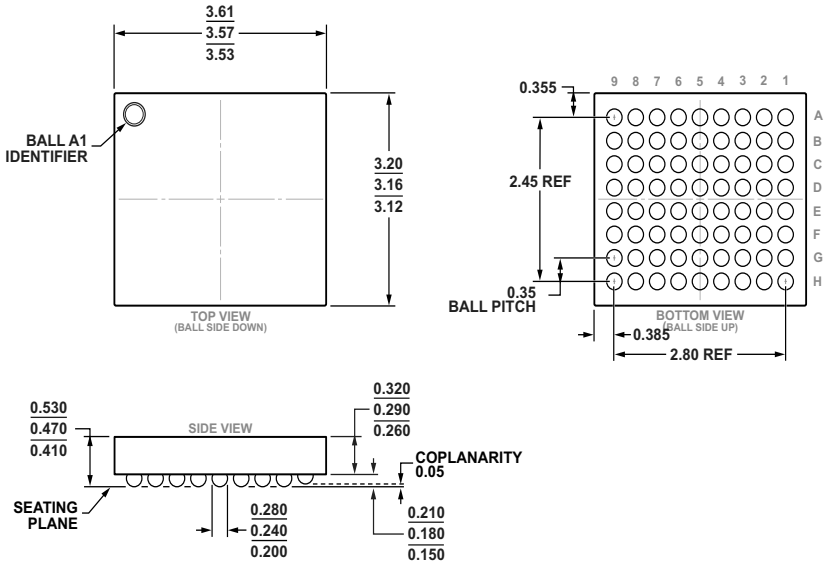


Figure 20. 72-Ball Wafer Level Chip Scale Package (WLCSP)
(CB-72-3)
Dimensions shown in mm

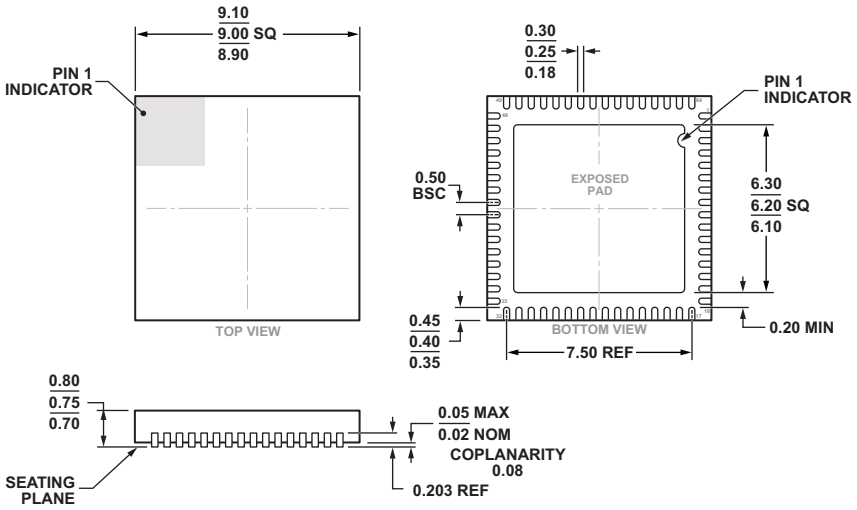


Figure 21. 64-Lead Frame Chip Scale Package (LFCSP_WQ)
9 x 9 mm Body, Very Thin Quad
(CP-64-17)
Dimensions shown in mm
Note: Exposed pad must be grounded.

FUTURE (PLANNED) PRODUCTS

Model[1]	Description	Temperature[2, 3]	Package Description	Package Option
ADuCM4050BCPZ-U1	ULP ARM Cortex-M4F with 512 KB Embedded Flash	−40°C to +85°C	64-Lead LFCSP	CP-64-17
ADuCM4050BCBZ-U1	ULP ARM Cortex-M4F with 512 KB Embedded Flash	−40°C to +85°C	72-Ball WLCSP	CB-72-3

[1] Z = RoHS Compliant Part.
[2] Referenced temperature is ambient temperature. The ambient temperature is not a specification. See the Absolute Maximum Ratings section for T_J (junction temperature) specification which is the only temperature specification.
[3] These are preproduction devices. See U1-Grade agreement for details.

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