Silicon SPDT Switch 100 MHz to 40 GHz

Preliminary Technical Data

ADRF5024

FEATURES

Ultrawideband frequency range: 100 MHz to 40 GHz
Reflective design
Low insertion loss: 1.5 dB at 40 GHz
High isolation: 37 dB at 40 GHz
High input linearity
1 dB compression (P1dB): 29.4 dBm typical
Third-order intercept (IP3): 50 dBm typical
High power handling: 27 dBm through path
ESD sensitivity: TBD
No low frequency spurious
RF settling time (0.1 dB final RF output): TBD
12-lead, 2.25 mm × 2.25 mm land grid array package

APPLICATIONS

Test instrumentation
Military radios, radars, electronic counter measures (ECMs)
Cellular infrastructure

FUNCTIONAL BLOCK DIAGRAM

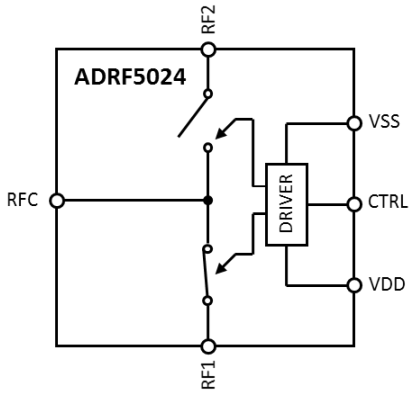

Figure 1.

GENERAL DESCRIPTION

The ADRF5024 is a general-purpose, single-pole, double-throw (SPDT) switch manufactured using a silicon process. It comes in a 2.25 mm × 2.25 mm, 12-lead land grid array (LGA) package and provides high isolation and low insertion loss from 100 MHz to 40 GHz.

This broadband switch requires dual supply voltages, +3.3 V and −3.3 V, and provides CMOS/LVTTL logic-compatible control.

Rev. PrA Document Feedback

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Technical Support www.analog.com

ADRF5024* PRODUCT PAGE QUICK LINKS

Last Content Update: 06/03/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- ADRF5024: Silicon SPDT Switch 100 MHz to 40 GHz Data Sheet

DESIGN RESOURCES

- ADRF5024 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADRF5024 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = −3.3 V, V_{CTL} = 0 V or 3.3 V, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			100		40,000	MHz
INSERTION LOSS						
Between RFC and RF1/RF2 (On)		100 MHz to 10 GHz		0.8		dB
		10 GHz to 30 GHz		1.3		dB
		30 GHz to 40 GHz		1.75		dB
ISOLATION						
Between RFC and RF1/RF2 (Off)		100 MHz to 10 GHz		45		dB
		10 GHz to 30 GHz		41		dB
		30 GHz to 40 GHz		37		dB
RETURN LOSS						
RFC and RF1/RF2 (On)		100 MHz to 10 GHz		27		dB
		10 GHz to 30 GHz		12		dB
		30 GHz to 40 GHz		10		dB
SWITCHING						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		2		ns
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		9		ns
Settling Time						
0.1 dB		50% V_{CTL} to 0.1 dB of final RF output		TBD		ns
0.05 dB		50% V_{CTL} to 0.05 dB of final RF output		TBD		ns
INPUT LINEARITY						
1 dB Power Compression	P1dB			29.4		dBm
Third-Order Intercept	IP3			50		dBm
SUPPLY CURRENT		VDD, VSS pins				
Positive Supply Current	I_{DD}			14		µA
Negative Supply Current	I_{SS}			120		µA
DIGITAL CONTROL INPUTS		CTRL pin				
Voltage						
Low	V_{INL}		0		TBD	V
High	V_{INH}		TBD		3.3	V
Current						
Low and High	I_{INL}, I_{INH}			<1		µA
RECOMMENDED OPERATING CONDITONS						
Supply Voltage						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Voltage	V_{CTL}		0		V_{DD}	V
RF Input Power	P_{IN}	f = 100 MHz to 40 GHz, T_{CASE} = 85°C				
Through Path		RF signal is applied to RFC or through connected RF1/RF2			27	dBm
Hot Switching		RF signal is present at RFC while switching between RF1 and RF2			27	dBm
Case Temperature	T_{CASE}		−40		+85	°C

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2.

Parameter	Rating
Positive Supply Voltage	−0.5 V to +3.6 V
Negative Supply Voltage	−3.6 V to +0.5 V
Digital Control Input Voltage	−0.5 V to V_{DD} + 0.5 V
RF Input Power (f = 100 MHz to 40 GHz, T_{CASE} = 85°C)	
Through Path	28 dBm
Hot Switching	28 dBm
Temperature	
Junction, T_J	135°C
Storage	−65°C to +150°C
Reflow (MSL3 Rating)	260°C
Junction to Case Thermal Resistance, θ_{JC}	
Through Path	TBD °C/W
ESD Sensitivity	
Human Body Model (HBM)	TBD

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

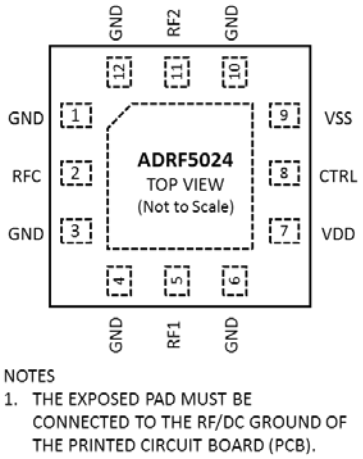


Figure 2. Pin Configuration (Top View)

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 4, 6, 10, 12	GND	Ground. These pins must be connected to the RF/dc ground of the printed circuit board (PCB).
2	RFC	RF Common Port. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc.
5	RF1	RF Throw Port 1. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc.
7	VDD	Positive Supply Voltage Pin.
8	CTRL	Control Input.
9	VSS	Negative Supply Voltage Pin.
11	RF2	RF Throw Port 2. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the printed circuit board (PCB).

INTERFACE SCHEMATICS

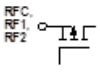


Figure 3. RF Pin Interface Schematic

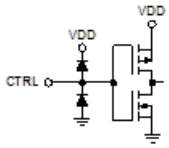


Figure 4. Digital Pin Interface Schematic

TYPICAL PERFORMANCE CHARCTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

TBD

TBD

TBD

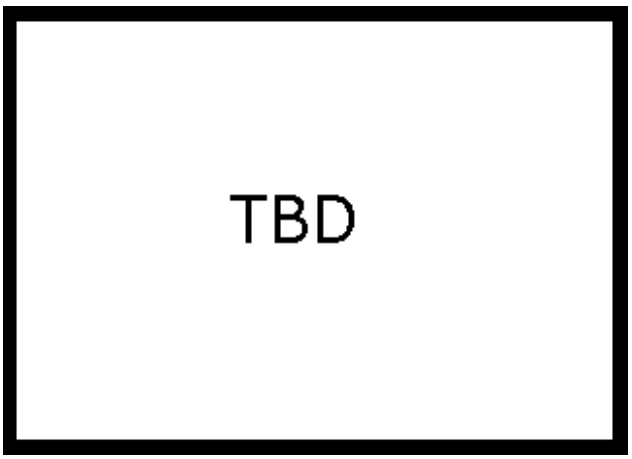
TBD

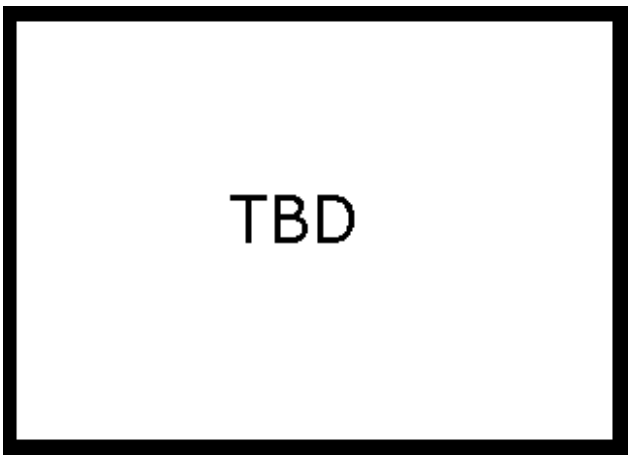
TBD

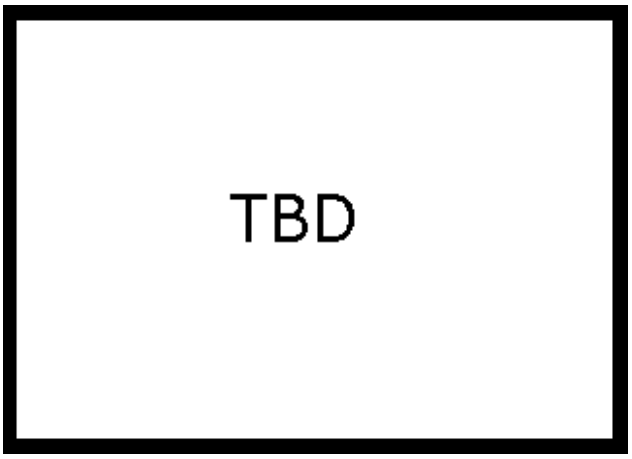
TBD

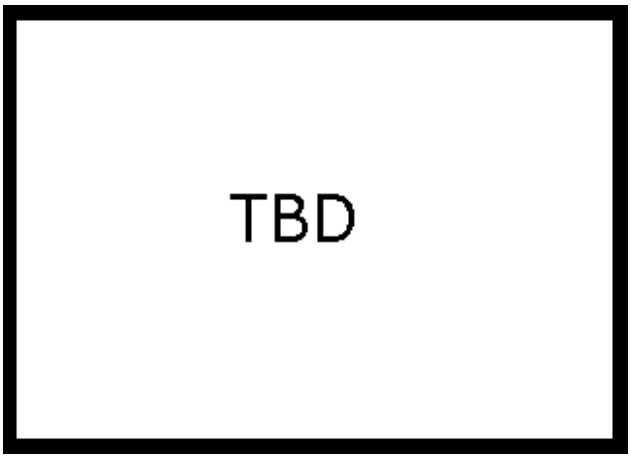
TYPICAL PERFORMANCE CHARCTERISTICS

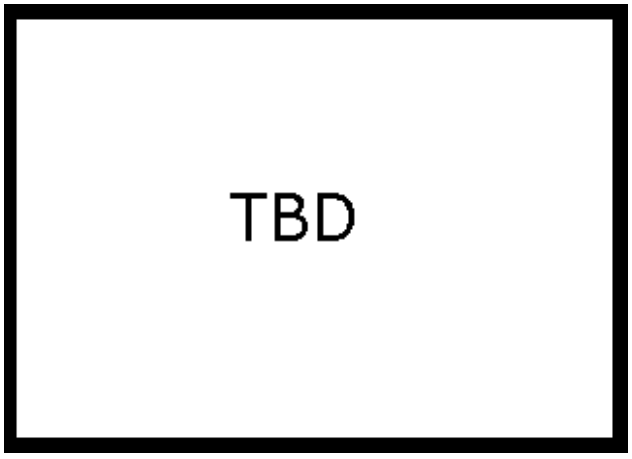
INPUT POWER COMPRESSION AND THIRD ORDER INTERCEPT

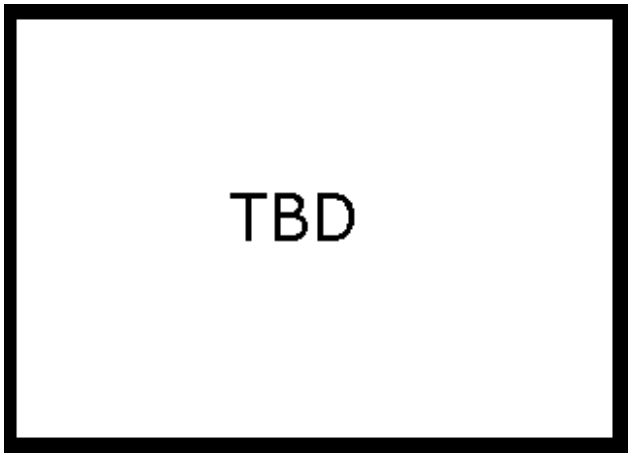












THEORY OF OPERATION

The ADRF5024 requires a positive supply voltage applied to the VDD pin and a negative supply voltage applied to the VSS pin. A driver is incorporated on die to perform logic functions internally and to provide the user with the advantage of a simplified control interface. The driver features a single digital control input pin, CTRL that controls the state of RF paths. Depending on the logic level applied to the CTRL pin, one RF path is in insertion loss state while the other path is in isolation state (see Table 4). The insertion loss path conducts the RF signal equally well in both directions between RF throw port and RF common port while the isolation path provides high loss between RF throw port and the insertion loss path. RF throw port becomes open reflective in off state.

Table 4. Control Voltage Truth Table

Digital Control Input	RF Paths	
V1	**RF1 to RFC**	**RF2 to RFC**
Low	Isolation (off)	Insertion loss (on)
High	Insertion loss (on)	Isolation (off)

The ideal power-up sequence is as follows:

1. Connect ground.
2. Power up VDD and VSS. The relative order is not important.
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. However, powering the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures.
4. Apply an RF input signal. The design is bidirectional; the RF input signal can be applied to the RFC port while the RF throw ports are outputs or vice versa. All of the RF ports are dc-coupled to 0 V, and no dc blocking is required at the RF ports when the RF line potential is equal to 0 V.

OUTLINE DIMENSIONS

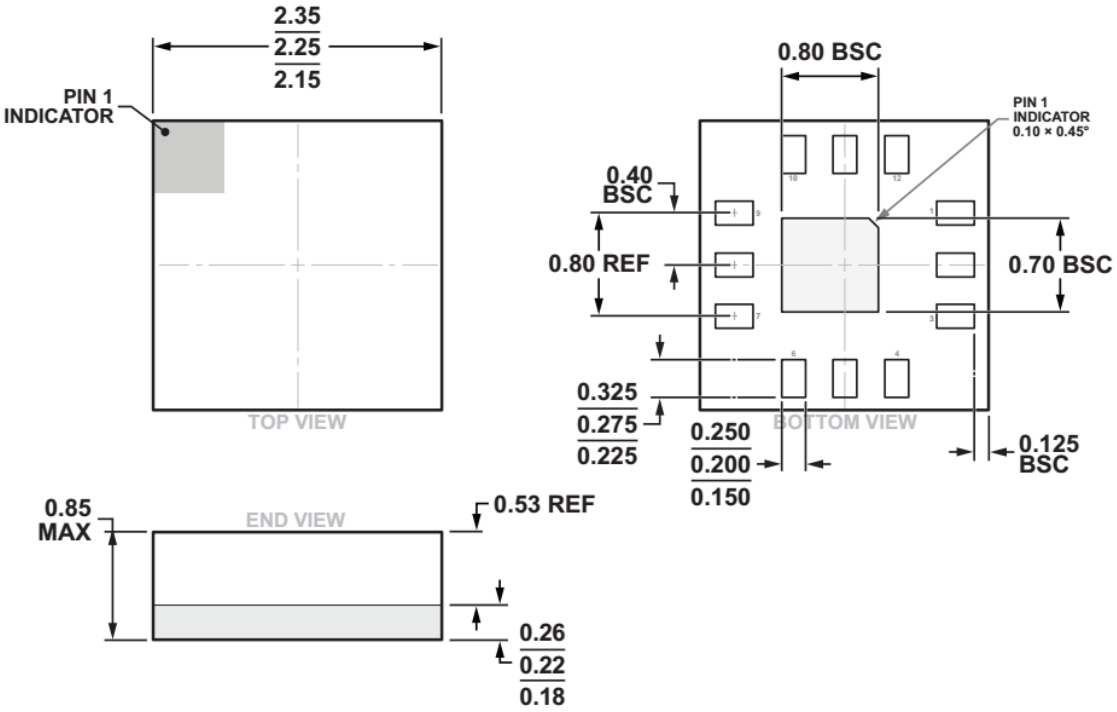


Figure 12-Terminal Land Grid Array [LGA]
2.25 mm × 2.25 mm Body and 0.75 mm Package Height
(CC-12-3)
Dimensions shown in millimeters

PR16011-0-5/17(PrA)