0.5 dB LSB, 6-Bit, Silicon Digital Attenuator, 9 kHz to 40 GHz

Preliminary Technical Data

ADRF5720

FEATURES

- Attenuation range: 0.5 dB steps to 31.5 dB
- Low insertion loss
  - 2.1 dB at 20 GHz
  - 3.0 dB at 30 GHz
  - TBD at 40 GHz
- Excellent attenuation accuracy
  - 0.2 ± 1% at 35 GHz
  - TBD at 40 GHz
- Typical step error: less than ±0.35 dB
- Low phase shift error: 35° phase shift at 20 GHz
- High input linearity
  - 0.1 dB power compression (P0.1dB)
    - 30 dBm for insertion loss state
    - 27 dBm for other states
  - Third-order intercept (IP3): 50 dBm
- High power handling: 27 dBm
- RF settling time (0.1 dB of final RF output): 6.8 µs
- TTL-/CMOS-compatible serial and parallel controls
- Dual supply, no low frequency switching spurs
- ESD rating: Class 1B (1000 V HBM)
- 4 mm × 4 mm, 24-lead land grid array package
- Pin compatible with ADRF5730, fast switching version

APPLICATIONS

- Test instrumentation
- Military radios, radars, electronic counter measures (ECMs)
- Cellular infrastructure

FUNCTIONAL BLOCK DIAGRAM

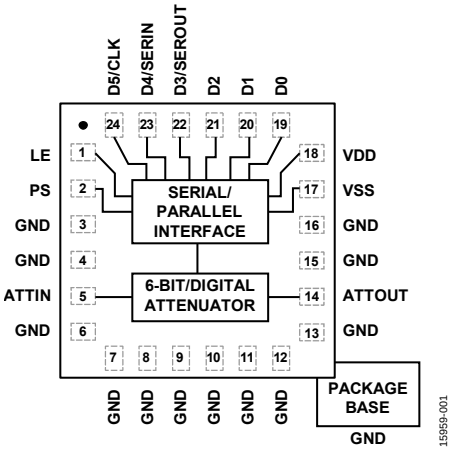

Figure 1.

GENERAL DESCRIPTION

The ADRF5720 is an ultrawideband, high accuracy 6-bit silicon digital attenuator, operating from 9 kHz to 40 GHz with 31.5 dB attenuation control range in 0.5 dB steps.

The ADRF5720 offers excellent attenuation accuracy and high linearity with maximum input power handling of 27 dBm for all states.

The ADRF5720 requires dual supply voltages, 3.3 V and −3.3 V. The device incorporates a driver that supports TTL-/CMOS-compatible serial and parallel controls.

The ADRF5720 is unidirectional, with an radio frequency (RF) input and output internally matched to 50 Ω. It comes in a RoHS compliant, 4 mm × 4 mm, 24-lead land grid array (LGA) package.

Rev. PrB Document Feedback

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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

V_{DD} = 3.3 V, V_{SS} = −3.3 V, control input voltage (V_{CTL}) = 0 V or 3.3 V, T_A = 25°C, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE			0.009		40,000	MHz
INSERTION LOSS	IL	9 kHz to 10 GHz		1.7		dB
		10 GHz to 20 GHz		2.1		dB
		20 GHz to 30 GHz		3.0		dB
		30 GHz to 35 GHz		3.7		dB
		35 GHz to 40 GHz		TBD		dB
ATTENUATION		9 kHz to 40 GHz				
Range		Between minimum and maximum attenuation states		31.5		dB
Step Size		Between any successive attenuation states		0.5		dB
Accuracy		All attenuation states referenced to insertion loss				
		9 kHz to 35 GHz		0.2 ± 1% of attenuation state		dB
		35 GHz to 40 GHz		TBD		dB
Step Error		Between any successive attenuation states				
		9 kHz to 35 GHz		±0.35		dB
		35 GHz to 40 GHz		TBD		dB
Overshoot/Undershoot		Between all attenuation states		+1.5/−2.5		dB
RETURN LOSS (ATTIN and ATTOUT)		All attenuation states				
		9 kHz to 30 GHz		13		dB
		30 GHz to 35 GHz		9		dB
		35 GHz to 40 GHz		TBD		dB
RELATIVE PHASE		10 GHz		18		Degrees
		20 GHz		35		Degrees
		35 GHz		75		Degrees
		40 GHz		TBD		Degrees
SWITCHING CHARACTERISTICS		All attenuation states				
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		1.6		µs
On and Off Time	t_{ON}, t_{OFF}	50% V_{CTL} to 90% of RF output		4.1		µs
Settling Time		50% V_{CTL} to 0.1 dB of final RF output		6.8		µs
		50% V_{CTL} to 0.05 dB of final RF output		8		µs
INPUT LINEARITY[1]		1 MHz to 40 GHz				
0.1 dB Compression	P0.1dB	Insertion loss state		30		dBm
		Other attenuation states		27		dBm
Third-Order Intercept	IP3			50		dBm
SUPPLY CURRENT		VDD, VSS pins				
Positive	I_{DD}	V_{DD} = 3.3 V		110		µA
Negative	I_{SS}	V_{SS} = −3.3 V		−110		µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL CONTROL INPUTS		LE, PS, D0, D1, D2, D3/SEROUT,[2] D4/SERIN, D5/CLK pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			1		µA
High	I_{INH}	D0, D1, D2		40		µA
		LE, PS, D3/SEROUT,[2] D4/SERIN, D5/CLK pins		1		µA
DIGITAL CONTROL OUTPUT		D3/SEROUT pin[2]				
Voltage						
Low	V_{OUTL}			0 ± 0.3		V
High	V_{OUTH}			V_{DD} ± 0.3		V
Current	I_{OUTL},I_{OUTH}				0.5	mA
RECOMMENDED OPERATING CONDITIONS						
Supply Voltage Range						
Positive	V_{DD}		3.15		3.45	V
Negative	V_{SS}		−3.45		−3.15	V
Digital Control Voltage	V_{CTL}		0		V_{DD}	V
RF Input Power						
ATTIN	P_{IN}	All attenuation states, T_{CASE} = 85°C			27	dBm
ATTOUT		For bidirectional use			TBD	dBm
Case Temperature	T_{CASE}		−40		+85	°C

[1] Input linearity performance degrades at frequencies less than 1 MHz.
[2] D3/SEROUT pin is an input in parallel control mode and an output in serial control mode. See Table 5 for pin function descriptions.

Timing Specifications

See Figure 17 and Figure 18 for the timing diagrams.

Table 2.

Parameter	Description	Min	Typ	Max	Unit
t_{SCK}	Minimum serial period, see Figure 17.	70			ns
t_{CS}	Control setup time, see Figure 17.	15			ns
t_{CH}	Control hold time, see Figure 17.		20		ns
t_{LN}	LE setup time, see Figure 17.	15			ns
t_{LEW}	Minimum LE pulse width, see Figure 17 and Figure 18.		1000 (TBD)		ns
t_{LES}	Minimum LE pulse spacing, see Figure 17.		630		ns
t_{CKN}	Serial clock hold time from LE, see Figure 17.		0		ns
t_{PH}	Hold time, see Figure 18.		10		ns
t_{PS}	Setup time, see Figure 18.		2		ns

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	
Positive	−0.5 V to +3.45 V
Negative	−3.45 V to +0.5 V
Digital Control Input Voltage	−0.3 V to V_{DD} + 0.3 V
RF Input Power[1] (f = 1 MHz to 30 GHz, T_{CASE} = 85°C)	
Average	28 dBm
Peak	31 dBm
Hot Switch	
Average	25 dBm
Peak	28 dBm
Temperature	
Junction (T_J)	135°C
Storage	−65°C to +150°C
Reflow (MSL3 Rating)	260°C
Continuous Power Dissipation (P_{DISS})	TBD
ESD Sensitivity	
Human Body Model (HBM)	1000 V (Class 1B)
Charge Device Model (CDM)	TBD

[1] Power handling degrades at frequencies less than 1 MHz.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
CC-24-4[1]	TBD	°C/W

[1] TBD.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

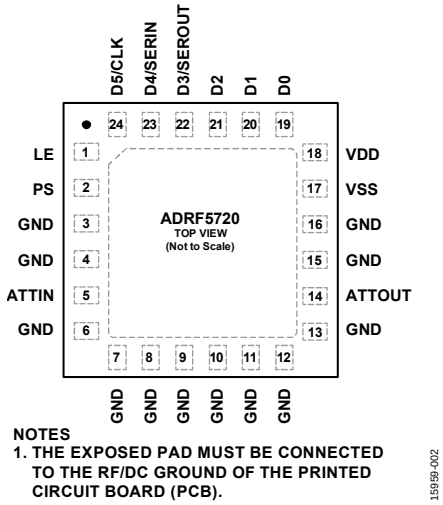


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	LE	Latch Enable Input. See the Theory of Operation section for more information.
2	PS	Parallel or Serial Control Interface Selection Input. See the Theory of Operation section for more information.
3, 4, 6 to 13, 15, 16	GND	Ground. These pins must be connected to the RF/dc ground of the PCB.
5	ATTIN	Attenuator Input. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc.
14	ATTOUT	Attenuator Output. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc.
17	VSS	Negative Supply Input.
18	VDD	Positive Supply Input.
19	D0	Parallel Control Input for 0.5 dB Attenuator Bit. See the Theory of Operation section for more information.
20	D1	Parallel Control Input for 1 dB Attenuator Bit. See the Theory of Operation section for more information.
21	D2	Parallel Control Input for 2 dB Attenuator Bit. See the Theory of Operation section for more information.
22	D3/SEROUT	Parallel Control Input for 4 dB Attenuator Bit (D3). Serial Data Output (SEROUT). See the Theory of Operation section for more information.
23	D4/SERIN	Parallel Control Input for 8 dB Attenuator Bit (D4). Serial Data Input (SERIN). See the Theory of Operation section for more information.
24	D5/CLK	Parallel Control Input for 16 dB Attenuator Bit (D5). Serial Clock Input (CLK). See Theory of Operation section for more information.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB.

INTERFACE SCHEMATICS

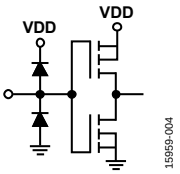


Figure 3. Digital Input Interface (LE, PS, D3/SEROUT, D4/SERIN, D5/CLK)

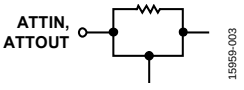


Figure 4. ATTIN and ATTOUT Interface

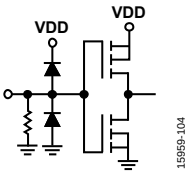


Figure 5. Digital Input Interface (D0, D1, D2)

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, STATE ERROR, STEP ERROR, AND RELATIVE PHASE

Measured on probe matrix board using ground/signal/ground (GSG) probes close to the RF pins. Refer to the Applications Information section for details on evaluation and probe matrix boards.

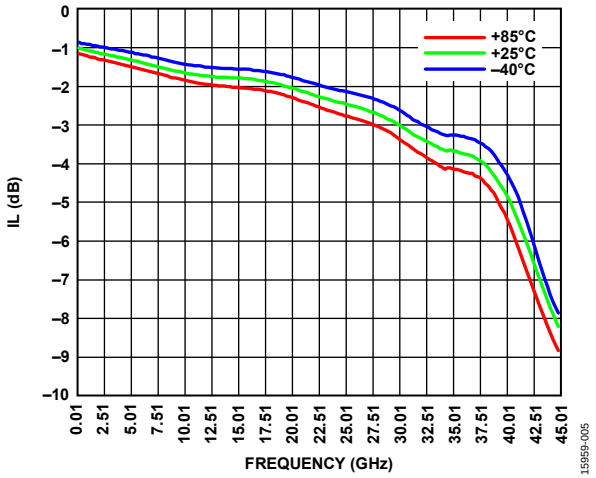


Figure 6. Insertion Loss (IL) vs. Frequency over Temperature

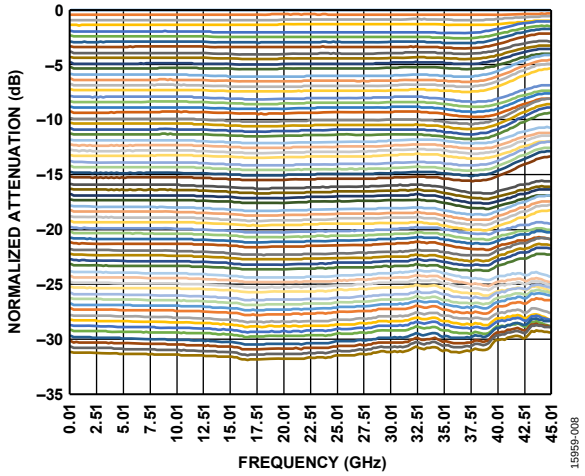


Figure 9. Normalized Attenuation for All States at Room Temperature

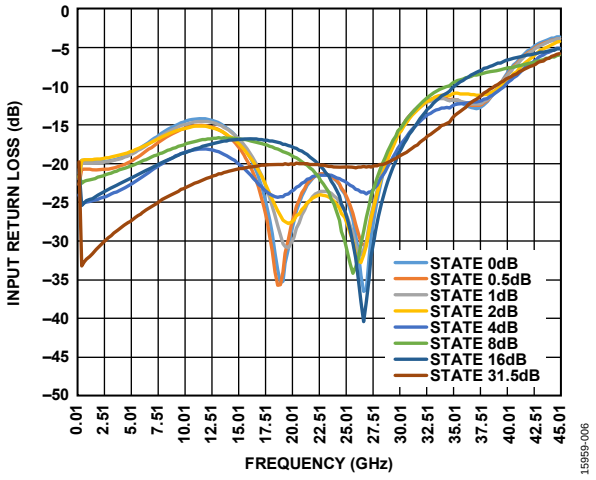


Figure 7. Input Return Loss (Major States Only)

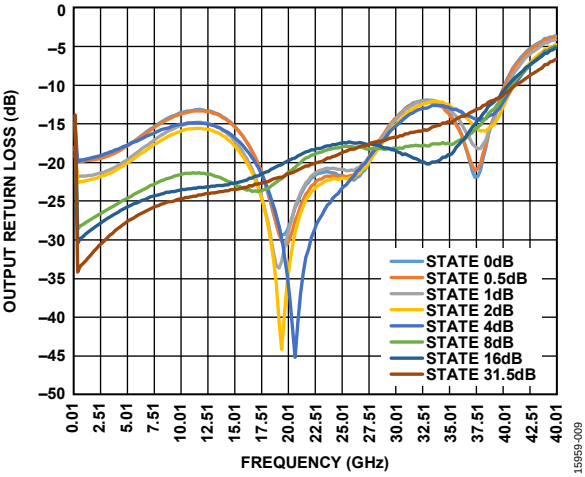


Figure 10. Output Return Loss (Major States Only)

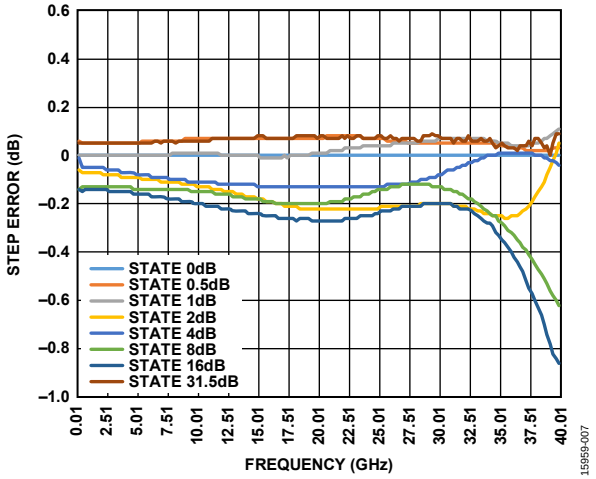


Figure 8. Step Error vs. Frequency (Major States Only)

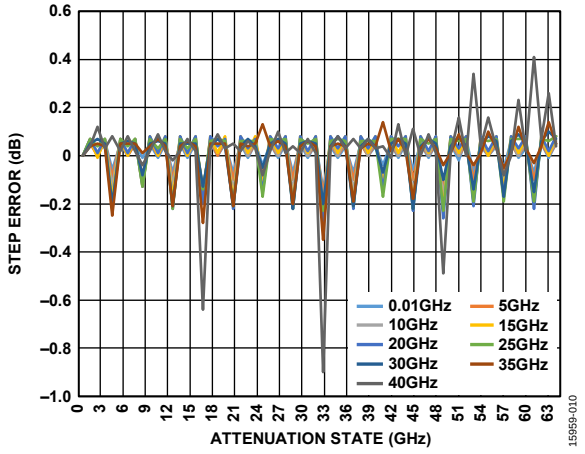


Figure 11. Step Error vs. Attenuation State over Frequency

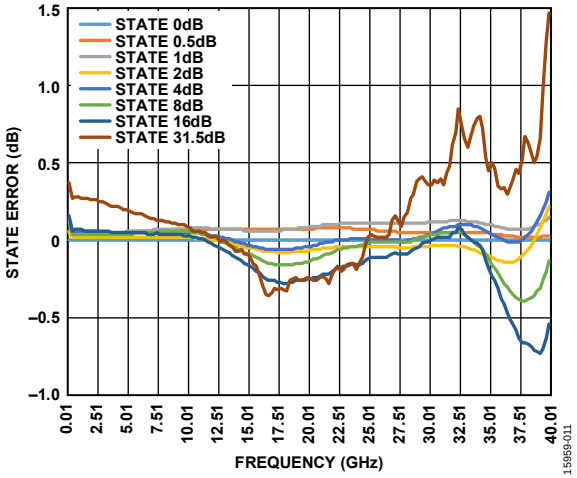


Figure 12. State Error vs. Frequency (Major States Only)

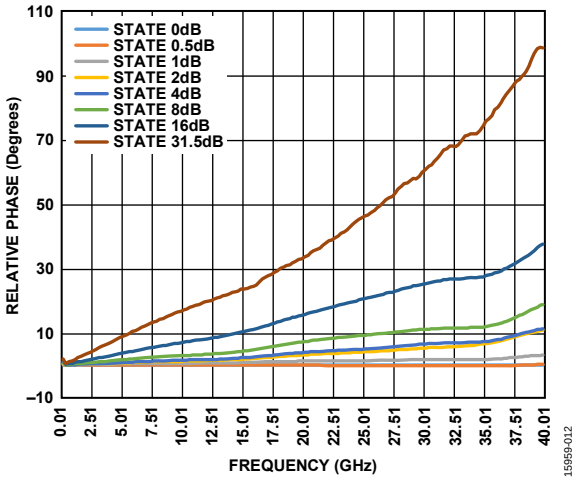


Figure 13. Relative Phase vs. Frequency (Major States Only)

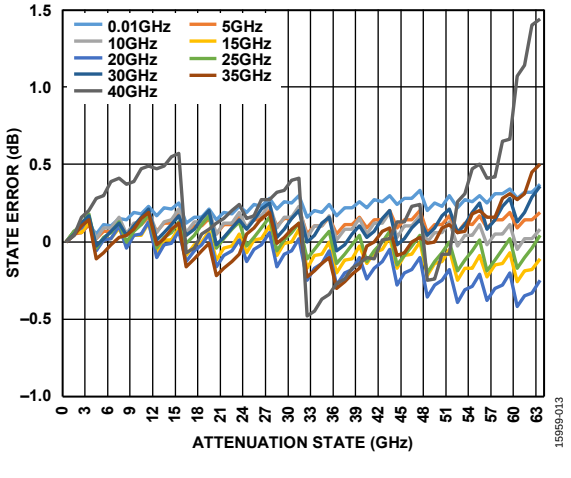


Figure 14. State Error vs. Attenuation State over Frequency

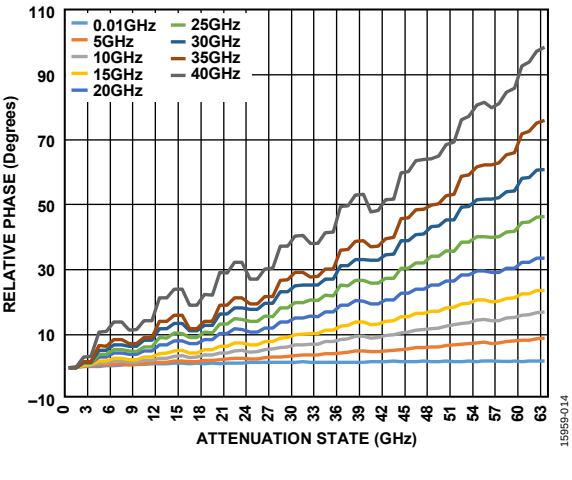
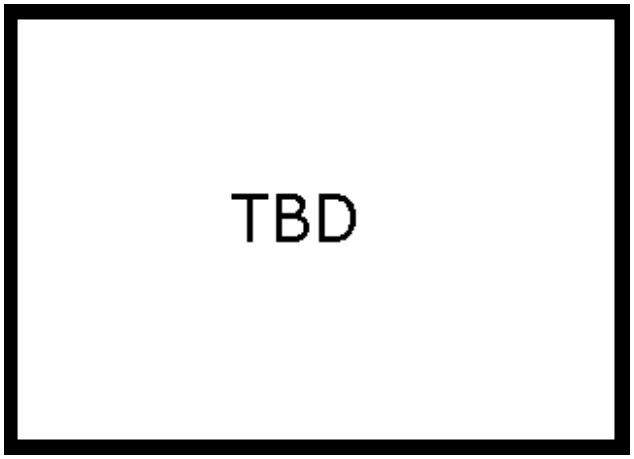
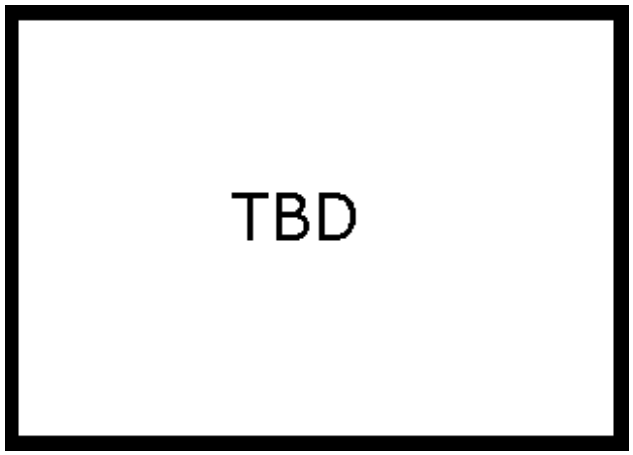
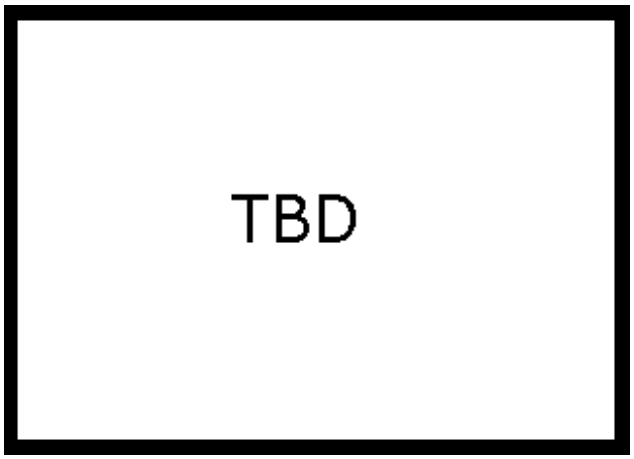


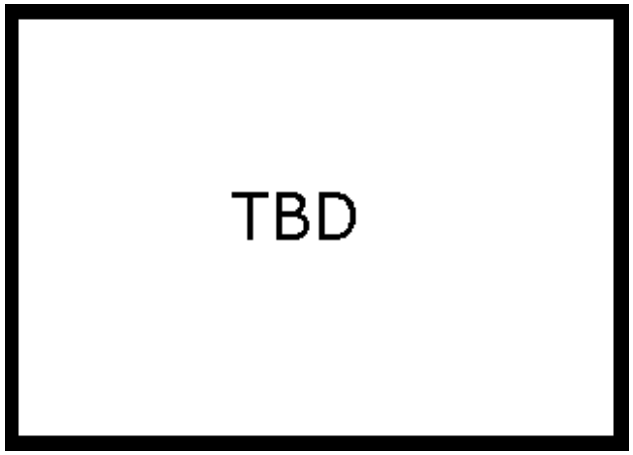
Figure 15. Relative Phase vs. Attenuation State over Frequency

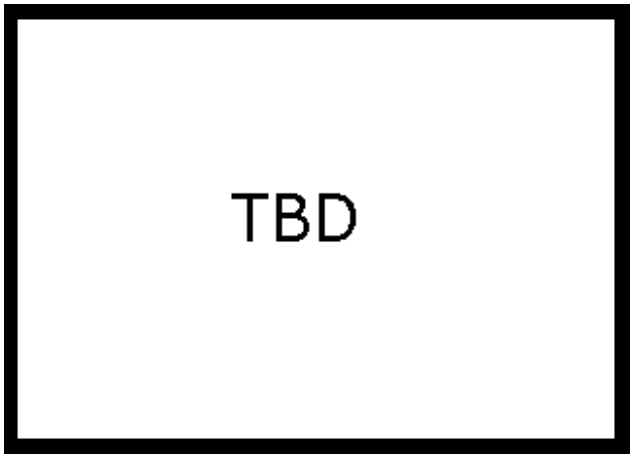
INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

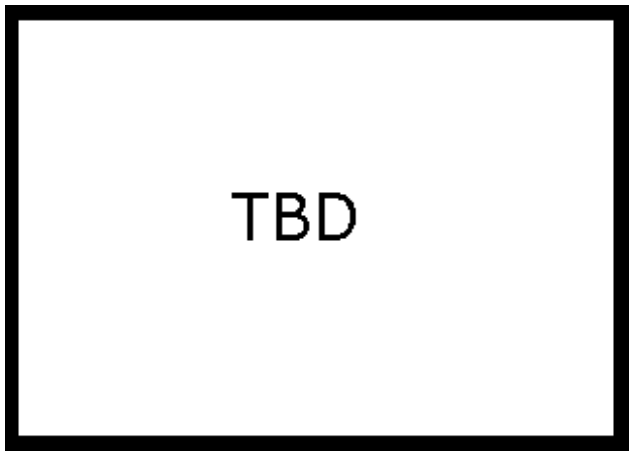












THEORY OF OPERATION

The ADRF5720 incorporates a 6-bit fixed attenuator array that offers an attenuation range of 31.5 dB in 0.5 dB steps. An integrated driver provides both serial and parallel mode control of the attenuator array (see Figure 16).

POWER SUPPLY

The ADRF5720 requires a dc voltage applied to the VDD and the VSS pins. The ideal power-up sequence is as follows:

1. Connect to ground.
1. Power up VDD and VSS. The relative order is not important.
2. Apply the digital control inputs. The relative order of the digital control inputs is not important. However, powering the digital control inputs before the VDD supply can inadvertently forward bias and damage the internal ESD protection structures.
3. Apply an RF input signal to ATTIN or ATTOUT.

The power-down sequence is the reverse of the power-up sequence.

RF INPUT AND OUTPUT

The ADRF5720 attenuator is unidirectional. It can be used bidirectionally at lower power levels. Refer to the RF input power limitations specified in Table 1. The ATTIN and ATTOUT pins are both internally matched to 50 Ω; therefore, no external matching components are required. RF pins are dc-coupled to 0 V; therefore, dc blocking capacitors are not required when the RF line potential is equal to 0 V.

SERIAL OR PARALLEL MODE SELECTION

The ADRF5720 can be controlled in either serial or parallel mode by setting the PS pin to high or low, respectively (see Table 6).

Table 6. Mode Selection

PS	Control Mode
Low	Parallel
High	Serial

SERIAL MODE INTERFACE

The ADRF5720 supports a 3-wire serial peripheral interface (SPI): serial data input (SERIN), clock (CLK), and latch enable (LE). The serial control interface is activated when PS is set to high.

In serial mode, the 6-bit SERIN data is clocked MSB first on the rising CLK edges into the shift register and then LE must be toggled high to latch the new attenuation state into the device. LE must be set to low to clock new 6-bit data into the shift register as CLK is masked to prevent the attenuator value from changing if LE is kept high. See Figure 17 in conjunction with Table 2 and Table 7.

The ADRF5720 also features a serial data output pin, SEROUT, that outputs serial input data delayed by six clock cycles to control the cascaded attenuator using a single SPI bus.

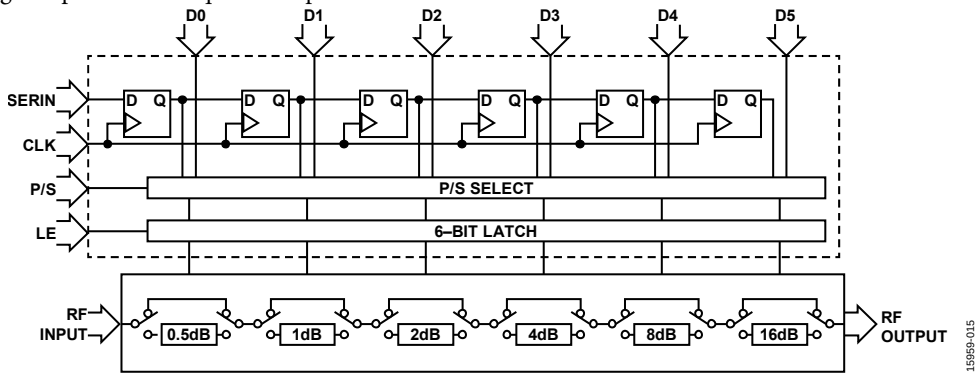


Figure 16. Simplified Circuit Diagram

Table 7. Truth Table

Digital Control Input[1]						
D5	D4	D3	D2	D1	D0	Attenuation State (dB)
Low	Low	Low	Low	Low	Low	0 (reference)
Low	Low	Low	Low	Low	High	0.5
Low	Low	Low	Low	High	Low	1.0
Low	Low	Low	High	Low	Low	2.0
Low	Low	High	Low	Low	Low	4.0
Low	High	Low	Low	Low	Low	8.0
High	Low	Low	Low	Low	Low	16.0
High	High	High	High	High	High	31.5

[1] Any combination of the control voltage input states shown in Table 7 provides an attenuation equal to the sum of the bits selected.

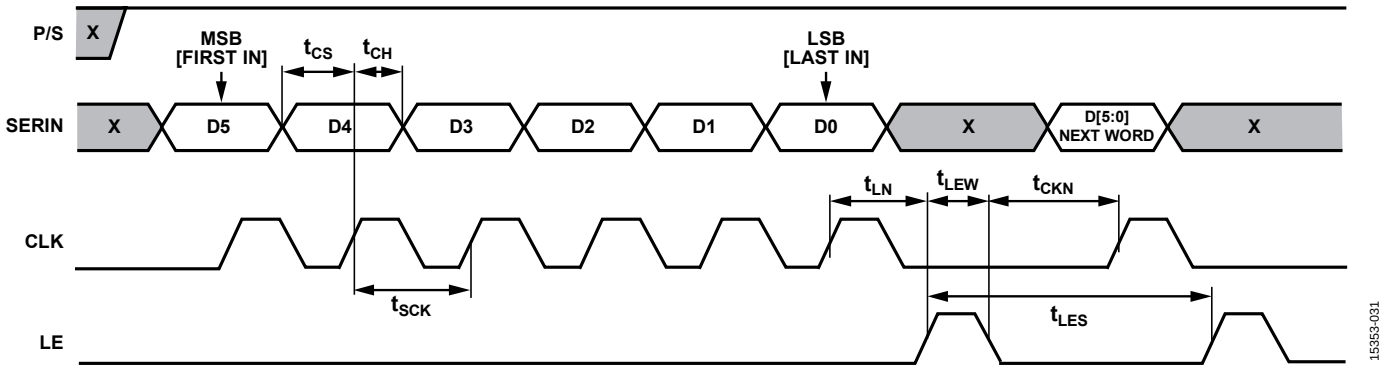


Figure 17. Serial Control Timing Diagram

PARALLEL MODE INTERFACE

The ADRF5720 has six digital control inputs, D0 (LSB) to D5 (MSB), to select the desired attenuation state in parallel mode, as shown in Table 7. The parallel control interface is activated when PS is set to low.

There are two modes of parallel operation: direct parallel and latched parallel.

Direct Parallel Mode

The LE pin must be kept high. The attenuation state is changed by the control voltage inputs (D0 to D5) directly. This mode is ideal for manual control of the attenuator.

Latched Parallel Mode

The LE pin must be kept low when changing the control voltage inputs (D0 to D5) to set the attenuation state. When the desired state is set, LE must be toggled high to transfer the 6-bit data to the bypass switches of the attenuator array, and then toggled low to latch the change into the device until the next desired attenuation change (see Figure 18 in conjunction with Table 2).

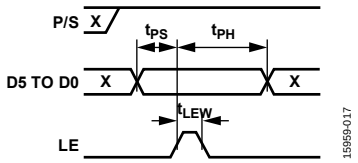


Figure 18. Latched Parallel Mode Timing Diagram

APPLICATIONS INFORMATION

EVALUATION BOARD

The ADRF5720-EVALZ is a 4-layer evaluation board. Each copper layer is 0.7 mil (0.5 oz) and separated by dielectric materials. Shown in Figure 19 is the stackup for this evaluation board.

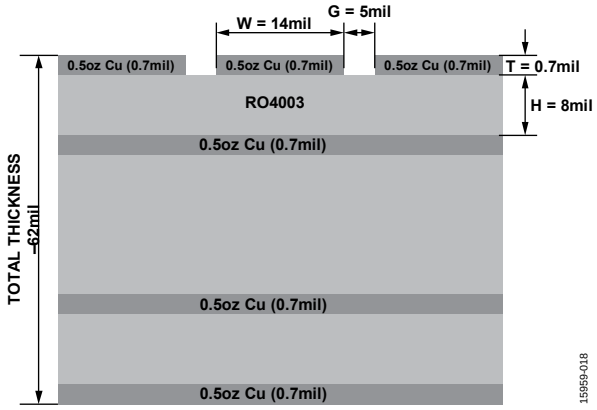


Figure 19. Evaluation Board (Cross Sectional View)

All RF and dc traces are routed on the top copper layer whereas the inner and bottom layers are grounded planes that provide a solid ground for the RF transmission lines. Top dielectric material is 8 mil Rogers RO4003, offering optimal high frequency performance. The middle and bottom dielectric materials provide mechanical strength. The overall board thickness is 62 mil, which allows 2.4 mm RF launchers to be connected at the board edges.

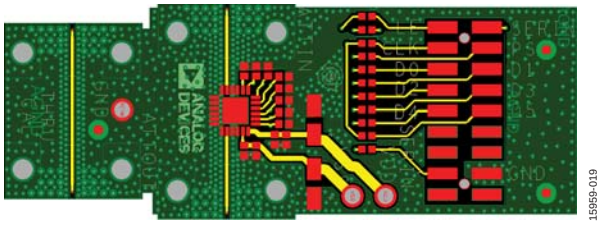


Figure 20. Evaluation Board Layout, Top View

The RF transmission lines were designed using a coplanar waveguide (CPWG) model, with trace width of 14 mil and ground clearance of 5 mil to have a characteristic impedance of 50 Ω. For optimal RF and thermal grounding, as many plated through vias as possible are arranged around transmission lines and under the exposed pad of the package.

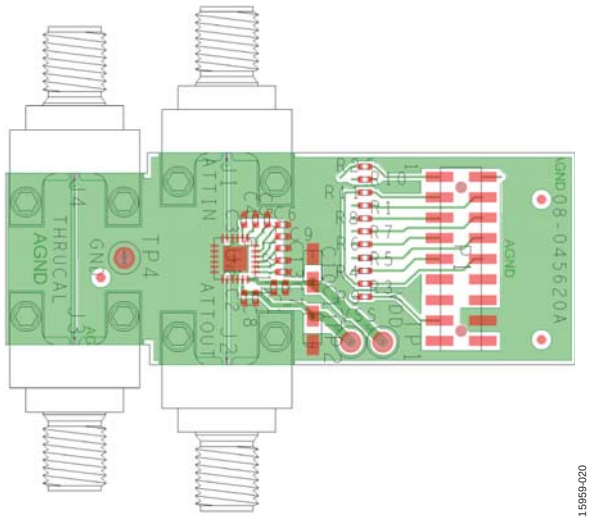


Figure 21. Evaluation Board Component Placement

Figure 21 shows the actual ADRF5720 evaluation board with component placement. Two power supply ports are connected to the VDD and VSS test points, TP1 and TP2, and the ground reference is connected to the GND test point, TP4. On the supply traces, VDD and VSS, a 100 pF bypass capacitor is used to filter high frequency noise. Additionally, unpopulated components positions are available for applying extra bypass capacitors.

The RF input and output ports (ATTIN and ATTOUT) are connected through 50 Ω transmission lines to the 2.4 mm RF launchers, J1 and J2, respectively. These high frequency RF launchers are by contact and not soldered onto the board. A thru calibration line connects the unpopulated J3 and J4 launchers; this transmission line is used to estimate the loss of the PCB over the environmental conditions being evaluated.

All the digital control pins are connected through digital signal traces to the 2 × 9-pin header, P1. There are provisions for an RC filter to help eliminate dc-coupled noise if needed by applications. The ADRF5720 was evaluated without an external RC filter, the series resistors are 0 Ω, and shunt capacitors are open on the evaluation board. The schematic of the ADRF5720 evaluation board is shown in Figure 22.

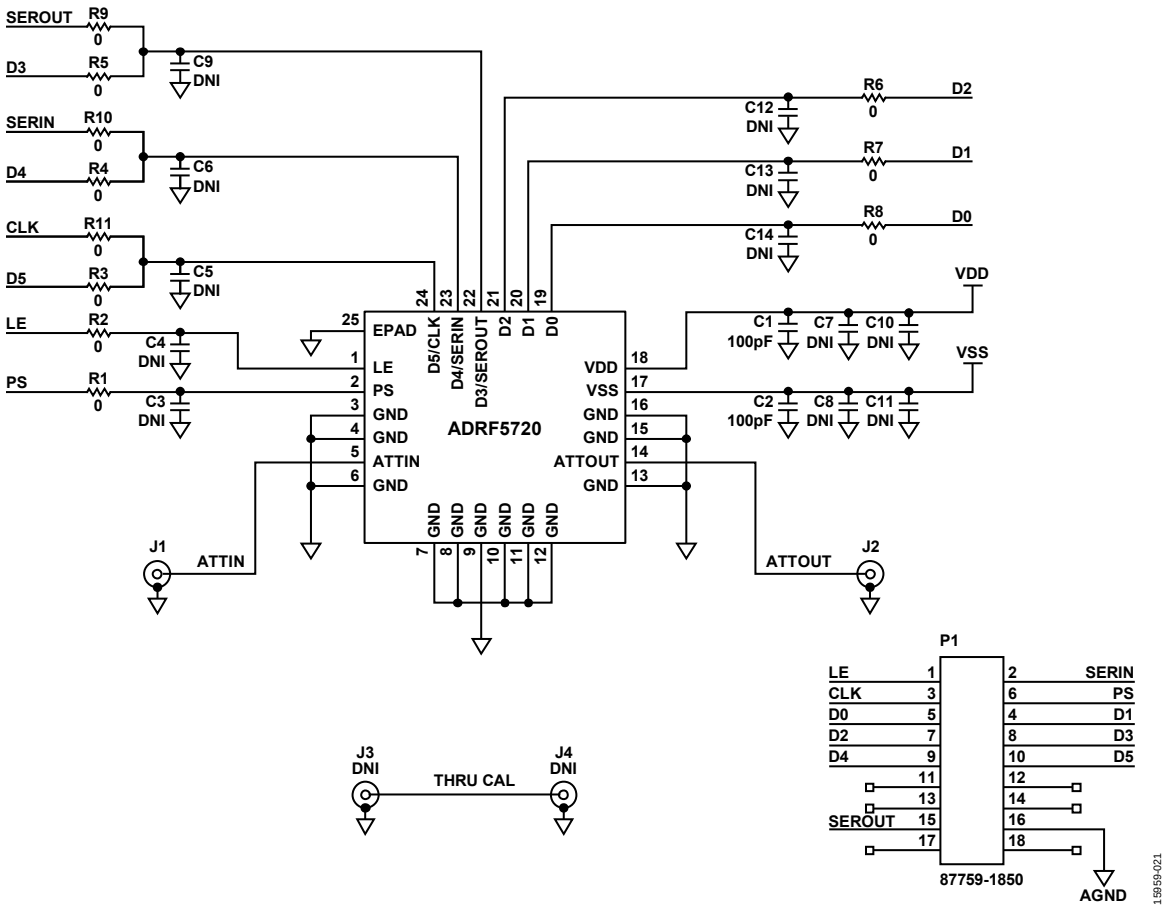


Figure 22. Evaluation Board Schematic

Table 8. Evaluation Board Components

Component	Default Value	Description
C1, C2	100 pF	Capacitor, C0402 package
C10, C11	10 µF	Capacitor, C3216 package
C7,C8	0.01 µF	Capacitor, C0402 package
J1, J2, J3, J4	Not applicable	2.4 mm end launch connector (Southwest Microwave: 1492-04A-5)
P1	Not applicable	2 × 9-pin header
R1 to R11	0 Ω	Resistor, 0402 package
TP1, TP2, TP4	Not applicable	Through hole mount test point
U1	ADRF5720	ADRF5720 digital attenuator, Analog Devices, Inc.
C3 to C6, C9, C12 to C14	100 pF	Capacitor, C0402 package

PROBE MATRIX BOARD

The probe matrix board is a 2-layer board. Similar to the evaluation board, this board also uses an 8 mil Rogers RO4003 dielectric inserted between two 0.7 mil copper layers. The RF transmission lines were designed using a CPWG model with a width of 14 mil and ground spacing of 5 mil to have a characteristic impedance of 50 Ω.

Figure 23 and Figure 24 show the cross sectional and top view of the board. Measurements are made using 535 µm GSG probes at close proximity to the RF pins. Unlike the evaluation board, probing reduces reflections caused by mismatch arising from connectors, cables, and board layout, resulting in a more accurate measurement of the part performance.

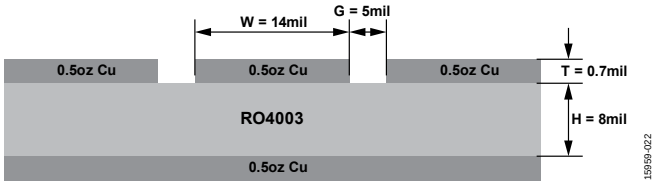


Figure 23. Probe Matrix Board (Cross Sectional View)

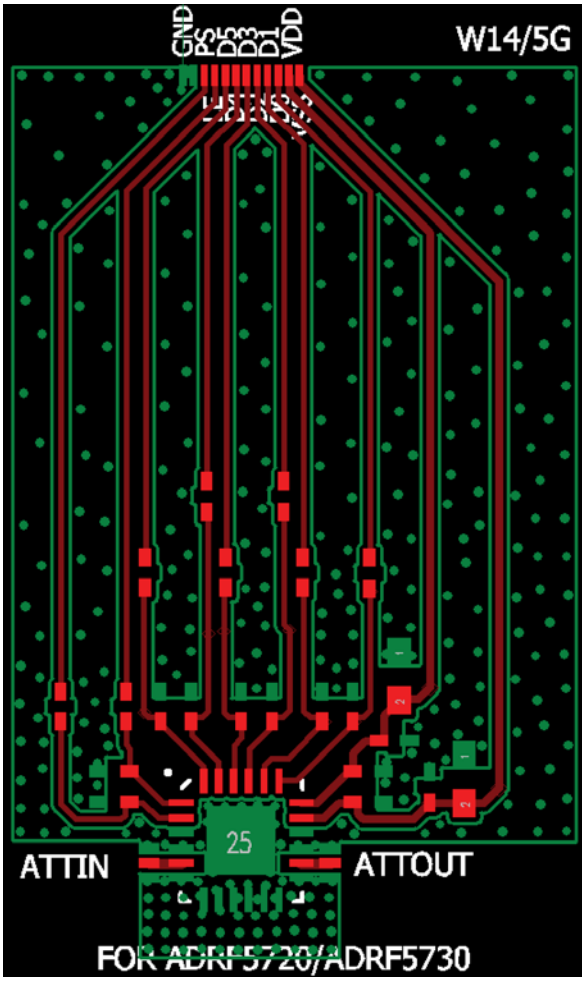


Figure 24. Probe Board Layout (Top View)

RF traces for a through reflect line (TRL) calibration are designed on the board itself. Board loss is compensated for at calibration by using a nonzero line length. The actual board duplicates the same layout in matrix form to assemble multiple devices at once. All S parameters were measured on this board.

HIGH IMPEDANCE CIRCUIT

Instead of using 50 Ω transmission lines at the RF pins, small signal measurement can further be improved by using high impedance transmission lines. Figure 25 and Figure 26 highlight the difference in the transmission line at the RF pins.

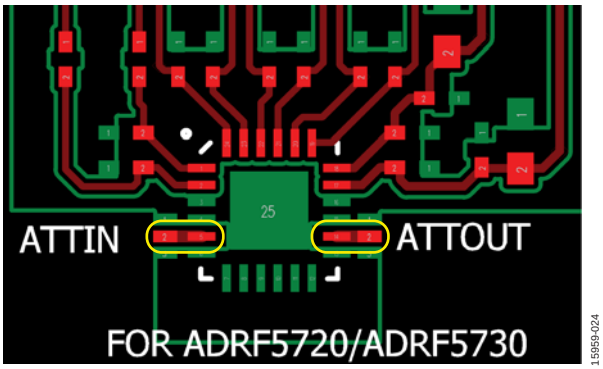


Figure 25. 50 Ω Impedance Lines

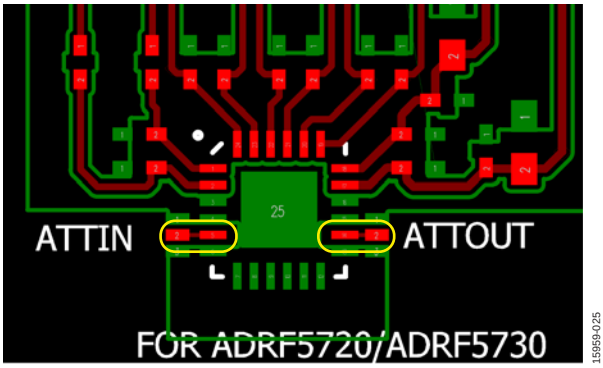


Figure 26. High Impedance Circuit.

The dimensions of the 50 Ω lines are with 14 mil trace width and 5 mil gap. To achieve a high impedance, use 10 mil length transmission lines of 5 mil trace width and 9.5 mil gap. Figure 27 to Figure 32 show the small signal performance of using this application circuit.

Table 9. Comparison of 50 Ω Parameters with High Impedance Circuit

Parameter	Comments	50 Ω Circuit (dB)	High Impedance Circuit (dB)
Insertion Loss	9 kHz to 10 GHz	1.7	1.5
	10 GHz to 20 GHz	2.1	2.3
	20 GHz to 30 GHz	3.0	2.8
	30 GHz to 35 GHz	3.7	3.4
	35 GHz to 40 GHz	TBD	TBD
Return Loss	9 kHz to 30 GHz	13	14
	30 GHz to 35 GHz	9	15
	35 GHz to 40 GHz	TBD	TBD

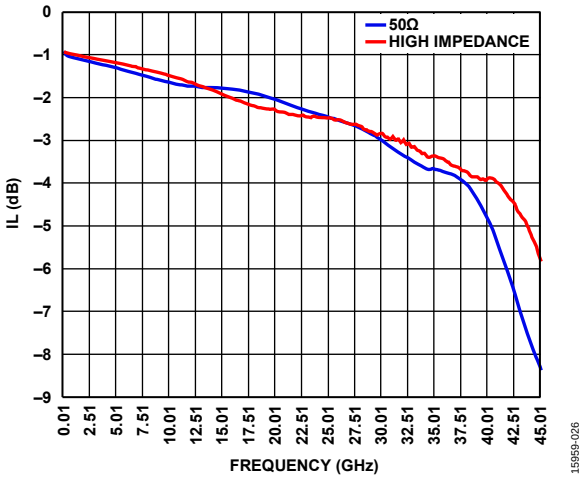


Figure 27. IL vs. Frequency, High Impedance and 50 Ω Circuit

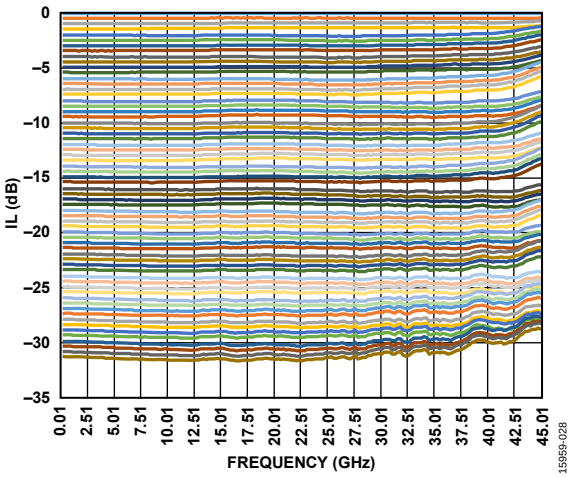


Figure 30. Normalized Attenuation for All States at Room Temperature, High Impedance

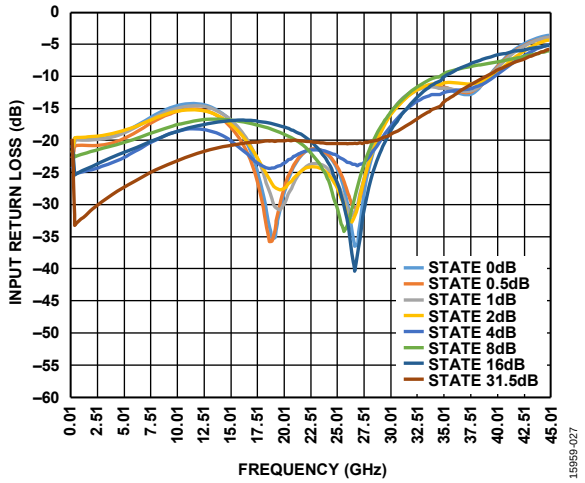


Figure 28. Input Return Loss (Major States Only), 50 Ω Circuit

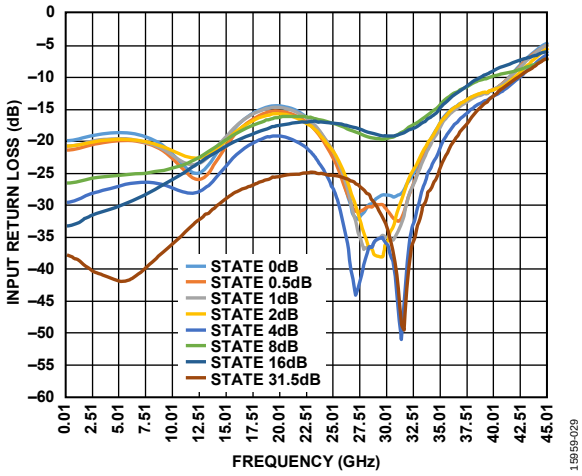


Figure 31. Input Return Loss (Major States Only), High Impedance Circuit

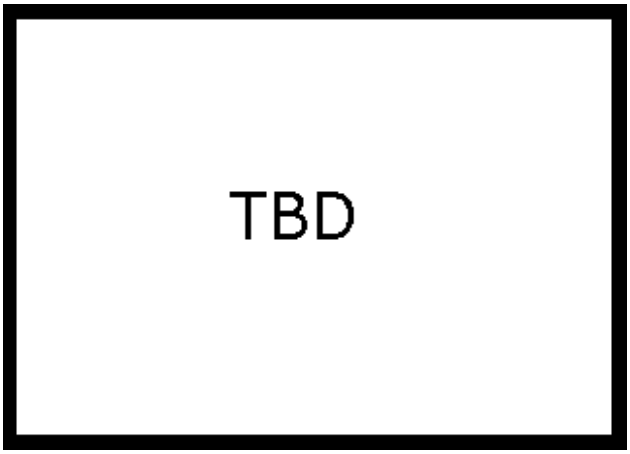


Figure 29. Step Error

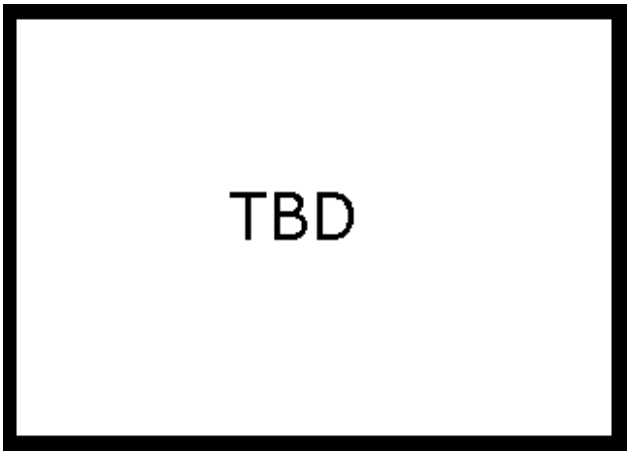


Figure 32. State Error

PACKAGING AND ORDERING INFORMATION

OUTLINE DIMENSIONS

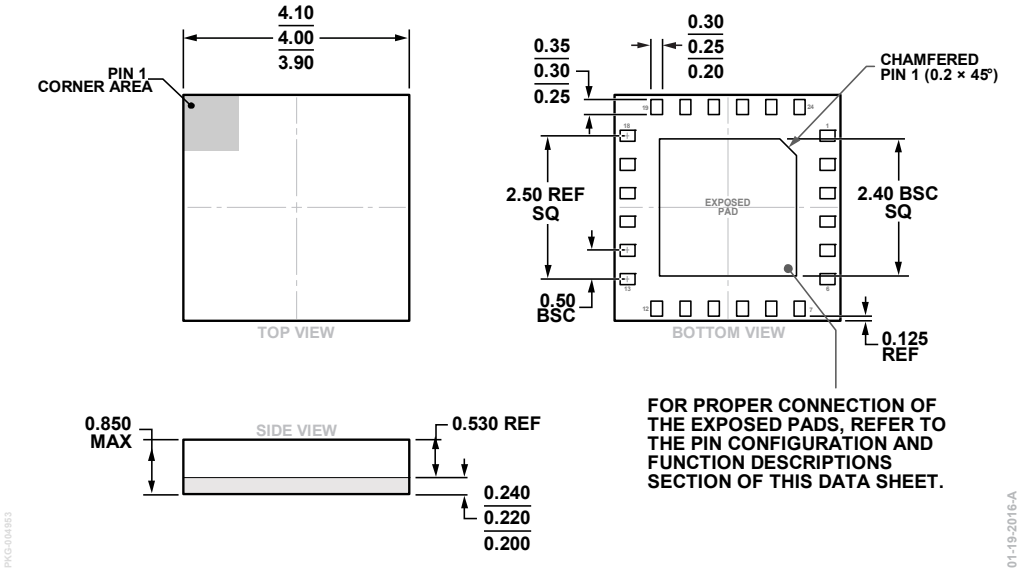


Figure 33. 24-Terminal Land Grid Array [LGA]
4 mm × 4 mm Body and 0.85 mm Package Height
(CC-24-5)
Dimensions shown in millimeters

PR15959-0-8/17(PrB)