Low Noise µPMU
3 A Buck Regulator with 3 A LDO

Preliminary Technical Data

ADP5003

FEATURES

Highly efficient low noise DC power supply system
- **High efficiency buck for first stage conversion**
- **High PSRR, low noise LDO to remove switching ripple**
- **Adaptive LDO headroom control option for optimal efficiency and PSRR across full load range**

3 A Low-Noise Buck Regulator
- **Wide Input Voltage Range: 4.2 V to 15 V**
- **Programmable Output Voltage Range: 0.6 V to 5 V**
- **< 40 uVrms Output Noise (Independent of output voltage)**
- **300 kHz to 2.5 MHz Internal clock with external sync up to 26 MHz (factory programmable divider)**

3 A Low-Noise NFET LDO (Active Filter)
- **Wide Input Voltage Range: 0.65 V to 5 V**
- **Fixed/Programmable Output Voltage Range: 0.6 V to 3.3 V**
- **Differential Point of Load Remote-Sensing**
- **< 10 uVrms Output Noise (independent of output voltage)**
- **PSRR > 50 dB (to 100 kHz) with 300 mV headroom at 3 A**
- **Ultra-Fast Transient Response**
- **Power Good Output**

Precision Enable Inputs for both the Buck Regulator and LDO

–40 °C to +125 °C junction temperature

32-lead 5 mm x 5 mm LFCSP Package

APPLICATIONS

Low noise power for High Speed ADC and DAC designs

Powering RF Agile Transceiver and Clocking ICs

FUNCTIONAL BLOCK DIAGRAM

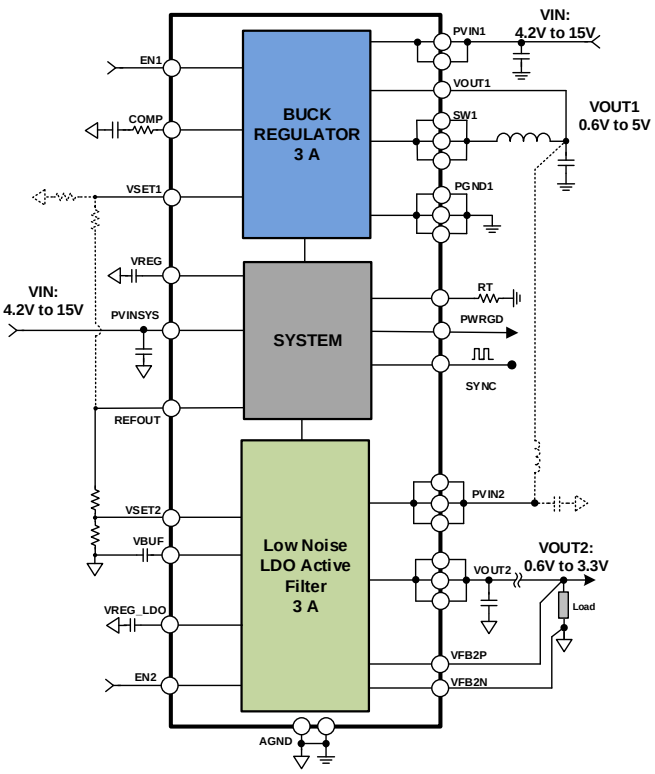

Figure 1.

GENERAL DESCRIPTION

ADP5003 integrates a high voltage buck regulator and an ultra-low noise low dropout (LDO) regulator in a small 5mm x 5mm LFCSP 32 lead package to provide highly efficient and quiet regulated supplies.

The buck regulator is optimized to operate at high output currents up to 3 A. The LDO is capable of a maximum output current of 3 A and is designed to operate efficiently with low headroom voltage while maintaining high power supply rejection for frequencies as high as 1MHz.

ADP5003 can be configured to operate in one of two modes. The adaptive mode allows the LDO to operate with a set headroom by adjusting the buck output voltage internally Alternatively ADP5003 can operate in an independent mode where both regulators operate separately from each other and where the output voltages are programmed using resistor dividers.

The LDO output voltage can be accurately controlled at the point of load (POL) using the remote sense which compensates for PCB trace impedance while delivering high output currents.

Each regulator is activated via a dedicated precision enable input. The buck switching frequency can be synchronized to an external signal, or programmed with an external resistor.

Safety features in the ADP5003 include thermal shutdown (TSD) and input undervoltage lockout (UVLO). The ADP5003 is rated for a –40°C to +125°C junction temperature range.

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COMPARABLE PARTS

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DOCUMENTATION

Data Sheet

- ADP5003: Low Noise µPMU 3 A Buck Regulator with 3 A LDO Preliminary Data Sheet

DESIGN RESOURCES

- ADP5003 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADP5003 EngineerZone Discussions.

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SPECIFICATIONS

GENERAL SPECIFICATIONS

V_{PVIN1} = $V_{PVINSYS}$ = 4.2 V to 15 V; V_{PVIN2} = 0.9 V to 5 V; V_{VREG} = V_{VREG_LDO} = 4.2 V to 5 V; T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT VOLTAGE RANGE	V_{PVIN1}, $V_{PVINSYS}$	4.2		15	V	
	V_{PVIN2}	0.65		5	V	
THERMAL SHUTDOWN						
Threshold	T_{SD}		150		°C	T_J rising
Hysteresis	T_{SD-HYS}		15		°C	
SYNC_IN INPUT						
Input Logic High	V_{IH}	1.1			V	
Input Logic Low	V_{IL}			0.4	V	
Input Leakage Current	$V_{I-LEAKAGE}$			TBD	µA	
ADAPTIVE MODE INPUT (VSET1)						
Input Rising Threshold	V_{ADPR}		2.5		V	
Input Hysteresis	V_{ADPH}		TBD		mV	
PWRGD OPEN DRAIN OUTPUT						
Output Voltage Level	V_{OL}		50	TBD	mV	I_{SINK} = 1 mA
PRECISION ENABLING						
High Level Threshold	V_{TH_H}	TBD	1.15	TBD	V	
Low Level Threshold	V_{TH_L}	TBD	1.05	TBD	V	
Shutdown Mode	V_{TH_S}			0.4	V	
EN1, EN2 Pull-down	R_{ENPD}		1.5		MΩ	
INPUT CURRENT						
Both Channels Enabled	$I_{STBY-NOSW}$		TBD	TBD	µA	No load
Both Channels Disabled	$I_{SHUTDOWN}$		5	TBD	µA	T_J = −40°C to +85°C
REFOUT CHARACTERISTICS						
Output Voltage	V_{REF}		2.0		V	
Accuracy		TBD		TBD	%	
VREG, VREG_LDO CHARACTERISTICS						
Output Voltage			5		V	
Accuracy		-2		2	%	
Current Limit[1]		10			mA	
POWER-GOOD PIN						
Power-good lower limit	$PWRGD_F$	80	85	90	%	FBx Low threshold
Power-good lower hysteresis	$PWRGD_{FH}$		2.5		%	FBx Low hysteresis
Power-good maximum drain current	$I_{PWRGD(MAX)}$	TBD				
Power-good Deglitch Time	t_{PWRGDD}		50		µs	
PVINSYS UNDERVOLTAGE LOCKOUT						
UVLO Input Voltage Rising	$UVLO_{PVINSYSRISE}$			4.2	V	
UVLO Input Voltage Falling	$UVLO_{PVINSYSFALL}$	3.9			V	

[1] VREG and VREG_LDO should not be used to supply external loads. This current limit is to protect against pin short to ground.

BUCK SPECIFICATIONS

$V_{PVIN1} = V_{PVINSYS}$ = 4.2 V to 15 V; V_{PVIN2} = 0.65 V to 5 V; $V_{VREG} = V_{VREG\_LDO}$ = 4.2 V to 5.25 V; T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS						
Programmable Output Voltage Range[1]	V_{PVOUT1}	0.6		5.0	V	
Buck Gain	A_{BUCK}		2.5			
Output Voltage Accuracy	V_{PVOUT1}	-1		1	%	I_{LOAD1} = 10 mA
Line Regulation	$(\Delta V_{PVOUT1}/V_{PVOUT1})/\Delta V_{PVIN1}$		TBD		%/V	I_{LOAD1} = 10 mA
Load Regulation	$(\Delta V_{PVOUT1}/V_{PVOUT1})/\Delta I_{PVOUT1}$		TBD		%/A	0 mA ≤ I_{LOAD1} ≤ 3 A V_{PVIN1} = 15 V
Total Output Voltage Accuracy			+/- 1.5		%	4.2 V ≤ V_{PVIN1} ≤ 15 V, 1 mA ≤ I_{LOAD1} ≤ 3 A
OPERATING SUPPLY CURRENT	I_{IN}		TBD		µA	I_{LOAD1} = 0 mA, LDO disabled
SW CHARACTERISTICS						
SW On Resistance	R_{PFET}		TBD	TBD	mΩ	V_{PVIN1} = 15 V (PVIN1 to SW1)
	R_{NFET}		TBD	TBD	mΩ	V_{PVIN1} = 15 V (SW1 to PGND1)
Current Limit	I_{LIMIT1}	TBD			A	NFET switch valley current limit
		-1			A	Negative current limit
Slew Rate	$SLEW_{SW}$		TBD		V/ns	I_{PVOUT1} = 1 A
Minimum on-time				TBD	ns	
Minimum off-time		TBD			ns	
ACTIVE PULL-DOWN	R_{PDWN-B}		75		Ω	Channel disabled
SOFT-START	t_{SSBUCK}		2		ms	See factory options
ADJ INPUT BIAS CURRENT	$I_{VSET1,2}$		10	150	nA	4.2 V ≤ $V_{PVINSYS}$ ≤ 15 V
OUTPUT NOISE	N_{PVOUT1}		40		µV r ms	10 Hz to 100 kHz
POWER SUPPLY REJECTION RATIO	$PSRR_{BUCK}$					V_{PVIN1} = 12 V, I_{VOUT1} = 1 A
			TBD		dB	1 kHz, V_{VOUT1} = 0.6 V
			TBD		dB	1 kHz, V_{VOUT1} = 3.3 V
			TBD		dB	10 kHz, V_{VOUT1} = 0.6 V
			TBD		dB	10 kHz, V_{VOUT1} = 3.3 V
			TBD		dB	100 kHz, V_{VOUT1} = 0.6V
			TBD		dB	100 kHz, V_{VOUT1} = 3.3 V
OSCILLATOR						
Internal Switching Freq.	f_{SW1}	2.25	2.5	2.75	MHz	R_T = x kΩ
	f_{SW2}	0.27	0.3	0.33	MHz	R_T = y kΩ
SYNC Frequency Range	f_{SYNC}	0.3		26	MHz	Maximum measured at 16x divider
SYNC Minimum Pulse		TBD			ns	
SYNC Min Off Time		TBD			ns	

[1] The minimum output voltage is dictated by the switching frequency and minimum on-time.

LDO SPECIFICATIONS

V_{PVIN1} = $V_{PVINSYS}$ = 4.2 V to 15 V; V_{PVIN2} = 0.65 V to 5 V; V_{VREG} = V_{VREG_LDO} = 4.2 V to 5.25 V; V_{HR} = 300 mV headroom[1]; T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT CHARACTERISTICS						
Programmable Output Voltage Range[2]	V_{PVOUT2}	0.6		3.3	V	
LDO Gain	A_{LDO}		1.65			
Output Voltage Accuracy	V_{PVOUT2}	-1		1	%	I_{LOAD2} = 100 mA @ 25°C
Line Regulation	$(\Delta V_{PVOUT2}/V_{PVOUT2})/\Delta V_{PVIN2}$		0.05		%/V	$(V_{PVOUT2} + V_{HR}) \le V_{PVIN2} \le 6$ V I_{LOAD2} = 100 mA
Load Regulation	$(\Delta V_{PVOUT2}/V_{PVOUT2})/\Delta I_{PVOUT2}$		0.2		%/A	10 mA ≤ $I_{LOAD2} \le 3$ A
Total Output Voltage Accuracy			+/- 1.5		%	$(V_{PVOUT2} + V_{HR}) \le V_{PVIN2} \le 6$ V, 10 mA ≤ $I_{LOAD2} \le 3$A
OPERATING SUPPLY CURRENT	I_{GND}		1	TBD	mA	I_{LOAD2} = 0 µA
			13	TBD	mA	I_{LOAD2} = 3 A
VREG_LDO to VOUT Minimum Voltage	V_{LDO-HR}	1.7			V	Required to drive NFET
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$		100	TBD	mV	I_{LOAD2} = 3 A
CURRENT-LIMIT THRESHOLD[4]	I_{LIMIT}	3.6			A	
SOFT START TIME	t_{SSLDO}		500		µs	SS = HiZ
ACTIVE PULL-DOWN	$R_{PDWNLDO}$		300		Ω	Channel disabled
OUTPUT NOISE	N_{PVOUT2}			10	µV rms	10 Hz to 100 kHz
POWER SUPPLY REJECTION RATIO	$PSRR_{LDO}$					VPVIN2 = VPVOUT2 + 0.2 V, IOUT = 1 A
			70		dB	1 kHz, VPVOUT2 = 0.6 V
			70		dB	1 kHz, VPVOUT2 = 3.3 V
			70		dB	10 kHz, VPVOUT2 = 0.6 V
			70		dB	10 kHz, VPVOUT2 = 3.3 V
			50		dB	100 kHz, VPVOUT2 = 0.6V
			50		dB	100 kHz, VPVOUT2 = 3.3 V
			30		dB	1000 kHz, VPVOUT2 = 0.6 V
			30		dB	1000 kHz, VPVOUT2 = 3.3 V
Combined PSRR Buck + LDO	$PSRR_{COMB}$		TBC		dB	
REMOTE SENSE FEEDBACK						
Maximum Voltage Drop PVOUT2 to VFB2P				TBD	V	
Maximum Voltage Drop AGND2 to VFB2N		TBD		TBD	V	
Maximum Filter Impedance[5]			TBD		Ω	

[1] V_{HR} is the LDO headroom voltage
[2] Limited by minimum VREG_LDO to PVOUT2 voltage.
[3] Dropout voltage is defined as the input to output voltage differential when the input voltage is set to the nominal output voltage.
[4] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 1.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 1.0 V, or 0.9 V.
[5] Maximum complex impedance from PVOUT2 to VFB2P in series with the load that is allowable for both stability and voltage drop at maximum load current

ADAPTIVE HEADROOM CONTROLLER SPECIFICATIONS

V_{PVIN1} = $V_{PVINSYS}$ = 4.2 V to 15 V; V_{PVIN2} = 0.65 V to 5 V; V_{VREG} = V_{VREG_LDO} = 4.2 V to 5.25 V; T_J = −40°C to +125°C for minimum/maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
HEADROOM ACCURACY						
Headroom Voltage Accuracy	V_{HR}	-1		1	%	I_{LOAD2} = 100 mA @ 25°C
HEADROOM VOLTAGE	V_{HR}					
			TBC		V	I_{LOAD2} = 0 A to 0.5 A
			TBC			I_{LOAD2} = 0.5 A to 2.5 A
			TBC			I_{LOAD2} = 2.5 A to 3 A

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
PVIN1, PVINSYS to AGND1	−0.3 V to +16 V
PVIN2 to AGND2	−0.3 V to +6.0 V
AGND1 to AGND2	−0.3 V to +0.3 V
PGND1to AGND1, AGND2	−0.3 V to +0.3 V
PVOUT2 to AGND	−0.3 V to (PVIN2 + 0.3 V)
VFB2N to AGND2	−0.3 V to +0.3 V
VOUT1, VFB2P, EN1, EN2, SYNC, RT, REFOUT, VBUF, VSET1, VSET2, COMP1 to AGND1, AGND2	−0.3 V to the lower of (VREG + 0.3 V) or + 6.0 V
SW1 to PGND1	−0.3 V to (PVIN1 + 0.3 V)
VREG, VREG_LDO to AGND1	−0.3 V to the lower of (PVINSYS + 0.3V) or +6.0 V
VREG to VREG_LDO	−0.3 V to +0.3 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} and θ_{JT} are based on a 4-layer printed circuit board (PCB) (two signal and two power planes) with nine thermal vias connecting the exposed pad to the ground plane as recommended in the layout considerations. $\boldsymbol{\theta_{JT}}$ is measured at the top of the package and is independent of the PCB. The $\boldsymbol{\Psi_{JT}}$ value is most appropriate for calculating junction to case temperature in the application.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JT}	Ψ_{JT}	Unit
32 Lead LFCSP	41.56	20.95	0.22	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

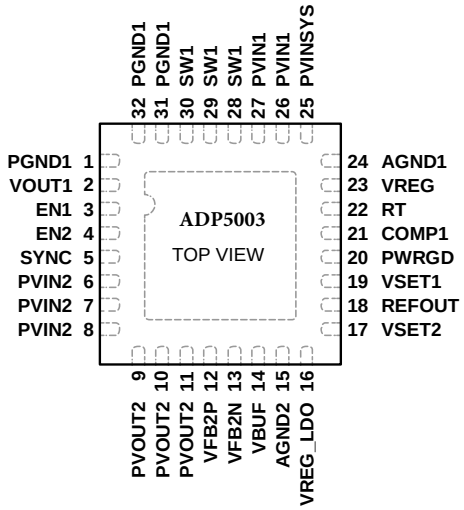


Figure 2. Pin Configuration – Top View (Preliminary data subject to change)

Table 4. Preliminary Pin Function Descriptions (Subject to change)

Pin No.	Mnemonic	Description
1, 31, 32	PGND1	Buck regulator dedicated power ground.
2	VFB1	Buck regulator sense feedback input. Connect short sense trace to output capacitor.
3	EN1	Buck regulator precision enable.
4	EN2	LDO precision enable.
5	SYNC	External clock input / Clock synchronization output (Factory programmable).
6, 7, 8	PVIN2	LDO regulator power input.
9, 10, 11	PVOUT2	LDO regulator power output.
12	VFB2P	LDO regulator positive sense feedback input. Connect sense trace to LDO output at load. Route with VFB2N on PCB
13	VFB2N	LDO regulator ground sense feedback input. Connect sense trace to ground at load. Route with VFB2P on PCB.
14	VBUF	Bypass capacitor terminal for LDO reference.
15	AGND2	LDO dedicated analogue ground.
16	VREG_LDO	Internal regulator output for LDO. Connect a ceramic decoupling capacitor between this pin and AGND2. Do not use to power external devices.
17	VSET2	LDO regulator output voltage configuration input.
18	REFOUT	Internal reference output required for driving external resistor dividers for VSET1 and VSET2.
19	VSET1	Buck regulator output voltage configuration input. Connect to VREG to enable adaptive regulation mode.
20	PWRGD	Power Good digital output (open-drain NFET pull down driver).
21	COMP1	Buck regulator external compensation.
22	RT	Resistor adjustable frequency programming input (Factory programmable).
23	VREG	Internal regulator output. Connect a ceramic decoupling capacitor between this pin and AGND1. Do not use to power external devices.
24	AGND1	Analog ground.
25	PVINSYS	System power supply for the ADP5003.
26,27	PVIN1	Buck regulator power input.
28, 29, 30	SW1	Buck regulator switching output.
EPAD	EPAD	Exposed Thermal pad. Connect to AGND1

THEORY OF OPERATION

POWER MANAGEMENT UNIT

The ADP5003 is a micro power management unit (uPMU) combing a step-down (buck) dc-to-dc converter and an ultra low noise low dropout linear regulator (LDO). The high switching frequency and 5mm x 5mm 32-lead LFCSP package allow for a compact power management solution.

Adaptive Headroom Control

The ADP5003 features a scheme to control the LDO headroom voltage. This ensures an optimal operating efficiency whilst maintaining ultra low noise performance across the full range of load current . When in adaptive mode, the buck regulator output voltage is managed by the ADP5003. Alternatively the buck and LDO may be operated independently with a fixed intermediate voltage.

Precision Enables / Shutdown

The ADP5003 has individual enable pins (EN1 and EN2) to control the regulators.

Each enable input has a coarse enable threshold associated with it which is used to turn on the ADP5003 internal logic and exit shutdown. When either EN1 or EN2 exceed the coarse enable rising threshold, the internal logic will turn on. When both EN1 and EN2 fall below the coarse enable falling threshold, the chip will enter shutdown mode.

A precision enable function allows for a precise turn on point for the regulators to allow the possibility of external sequencing. A voltage level higher than V_{ENRP} applied to the EN1 or EN2 pin activates a regulator whereas a level below V_{ENRP}, minus V_{ENHP} hysteresis, turns off a regulator. The buck is controlled by EN1, and the LDO is controlled by EN2 pin.

Undervoltage Lockout (UVLO)

To protect against input voltage being too low, under voltage lockout (UVLO) circuitry is integrated in the system. If the input voltage on PVINSYS drops below a predefined UVLO threshold, all channels shut down.

The part is enabled again when the voltage on PVINSYS rises above the UVLO threshold if the enable pins remain active.

Thermal Shutdown (TSD)

In the event that the junction temperature rises above 150°C, the thermal shutdown circuit turns off all of the regulators. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 15°C hysteresis is included so that when thermal shutdown occurs, the regulators do not return to operation until the on-chip temperature drops below 135°C. When emerging from thermal shutdown, all regulators restart with soft start control.

Active Pulldown

Both regulators have optional, factory programmable, active pull-down resistors discharging the respective output capacitors when the regulators are disabled. The pull-down resistors are connected between VOUTx and AGND. Active pull-downs are disabled when the regulators are turned on.

In case of a TSD or UVLO event, the active pull-downs are enabled to discharge the output capacitors quickly. The pull-down resistors remain engaged until the fault event is no longer present or the input supply voltage falls below a min voltage level, typically 1V, that guarantees pull-down to remain enabled.

Soft Start

Both regulators have an internal soft start function that ramps the output voltage in a controlled manner upon startup, thereby limiting the inrush current. This reduces the risk of noise spikes and voltage drops on upstream supplies.

The ADP5003 may be factory programmed to allow control of either the SS time.

Power-Good

The ADP5003 has a dedicated power good, open-drain, output PWRGD. This indicates whether one or more regulators are outside the voltage limits specified by $PWRGD_L$ (Lower limit) and $PWRGD_R$ (Upper limit). When either one or both of the regulator outputs are outside the power good limits, the PWRGD output is pulled low.

When in adaptive mode the power-good will only monitor the LDO output.

When in standalone mode the power-good will only monitor the regulator / regulators which are enabled.

During startup the PWRGD will be held low until the soft start ramp is complete.

BUCK REGULATOR

Control Scheme

The buck operate with a fixed frequency, current mode PWM control architecture where the duty cycle of the integrated switches is adjusted and regulates the output voltage.
At the start of each oscillator cycle, the PFET switch is turned on, sending a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current threshold, which turns off the PFET switch and turns on the NFET synchronous rectifier. This sends a negative voltage across the inductor, causing the inductor current to decrease. The synchronous rectifier stays on for the remainder of the cycle. The buck regulates the output voltage by adjusting the peak inductor current threshold. The peak current sense signal is generated by means of an emulated inductor current scheme which senses the actual current in the inductor during the 'off' phase of cycle when the NFET is conducting. This information is used to set the emulated signal into a capacitor which then mimics the ramp during the 'on' phase of the cycle which is what is the used to compare against the control signal.

Startup

The buck will turn on with a controlled ramp set according to the internal factory programmed soft start setting.

Oscillator Frequency Control

The ADP5003 may be factory programmed to allow control of either the SS time or the buck regulator oscillator frequency using the RT/SS pin. If configured, the RT/SS pin can be connected via a resistor to AGND in order to define the buck regulator internal switching frequency.

When there is no resistor present on the pin, the internal oscillator will operate at the lowest frequency. An upper limit will prevent out of range frequencies when the RT/SS pin is shorted to ground or connected with an incorrect resistor value.

External Oscillator Synchronisation

The SYNC_IN/SYNC_OUT pin is dedicated to oscillator synchronisation and allows the ADP5003 to lock to an external clock or to output a synchronisation signal for low noise applications. The pin may be factory programmed to either mode.

In SYNC_IN mode, an applied external clock signal will act as a synchronization and the buck regulator will operate in sync with this signal. By default the ratio of SYNC_IN frequency to internal frequency is 1:1, however this can be factory programmed to 2:1, 4:1, 8:1 or 16:1 in order to divide down from faster system clocks.

When alternating between external clocks and the internal oscillator, the presence of an external frequency will cause a multiplexer to switch between the internal oscillator and the external SYNC frequency. The output of this multiplexer will act as the frequency reference to an internal PLL. This will ensure that changing between the two modes of operation will result in a smooth transition between the different frequencies.

In SYNC_OUT mode, the pin will output the internal buck switching frequency allowing other regulators or devices to synchronize with this signal.

Current Limit

The buck has protection circuitry to limit the amount of current flowing through the switches.

Short Circuit Protection

The buck has protection circuitry to limit the amount of current in the event of a short circuit on the output.

LDO REGULATOR

The ADP5003 contains a single low-noise, low dropout linear regulator that uses an NFET pass device to provide high power supply rejection ratio (PSRR) with low headroom voltage and output current up to 3 A.

APPLICATIONS

POWER MANAGEMENT UNIT

Soft Start

The ADP5003 may be factory programmed to allow control of the SS time.

Power-Good

An external pull-up is necessary to drive PWRGD output high. Whilst the value of the pull-up resistor is not critical, it is recommended to use a 10kΩ to 300kΩ resistor. The resistor must be pulled to a voltage level within 1.2V to 5V. The PWRGD pin can sink a maximum current of $I_{PWRGD(MAX)}$.

BUCK REGULATOR

Output Voltage

The output voltage on the buck regulator is adjustable through an external resistor divider or can be factory programmed to default values. When using adaptive control, the buck output voltage is controlled by the ADP5003.

Adjustable output voltage operation is shown in Figure 3 and fixed voltage operation in Figure 4.

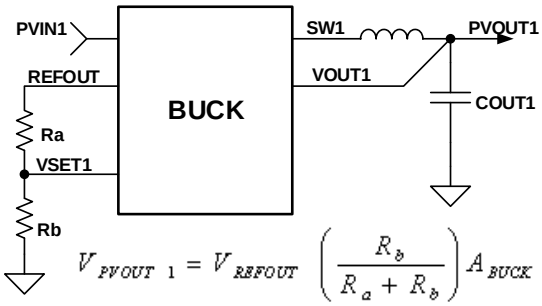


Figure 3. Buck Adjustable Output VoltageSetting

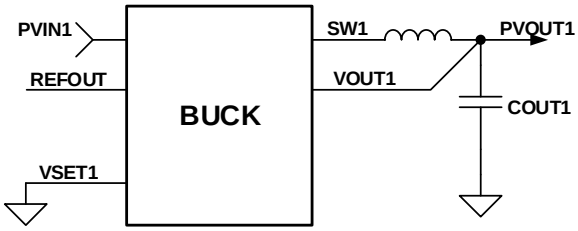


Figure 4 Buck Fixed Output Voltage Configuration

LDO REGULATOR

Output Voltage

The output voltage on the LDO regulator is adjustable through an external resistor divider or can be factory programmed to default values. Adjustable output voltage operation is shown in Figure 5 and fixed voltage operation in Figure 6.

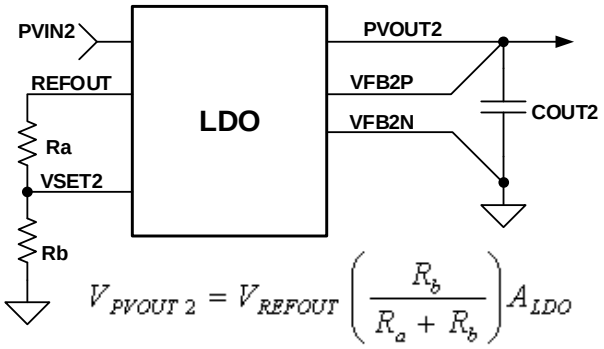


Figure 5. LDO Adjustable Output VoltageSetting

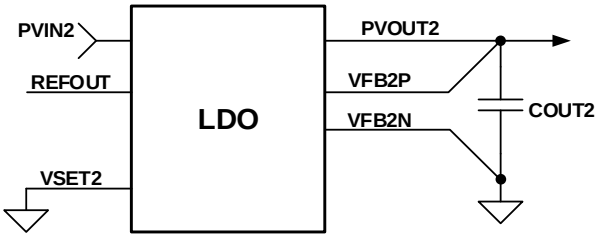


Figure 6. LDO Fixed Output Voltage Configuration

ADAPTIVE OPERATION

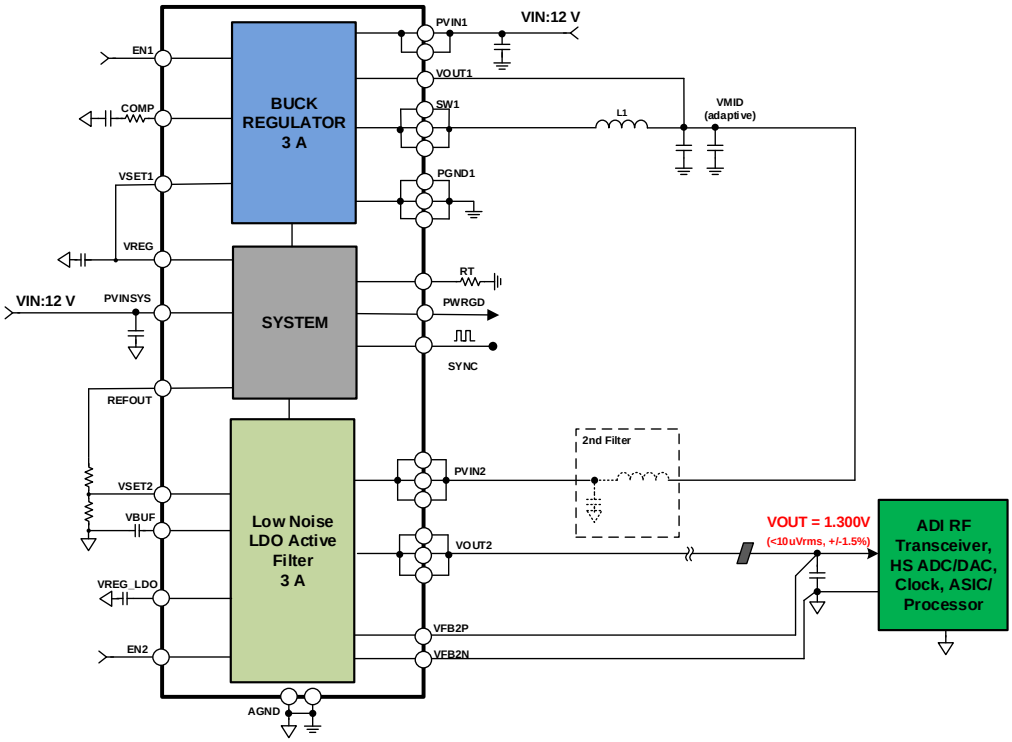


Figure 7. Adaptive Operation Mode

INDEPENDENT OPERATION

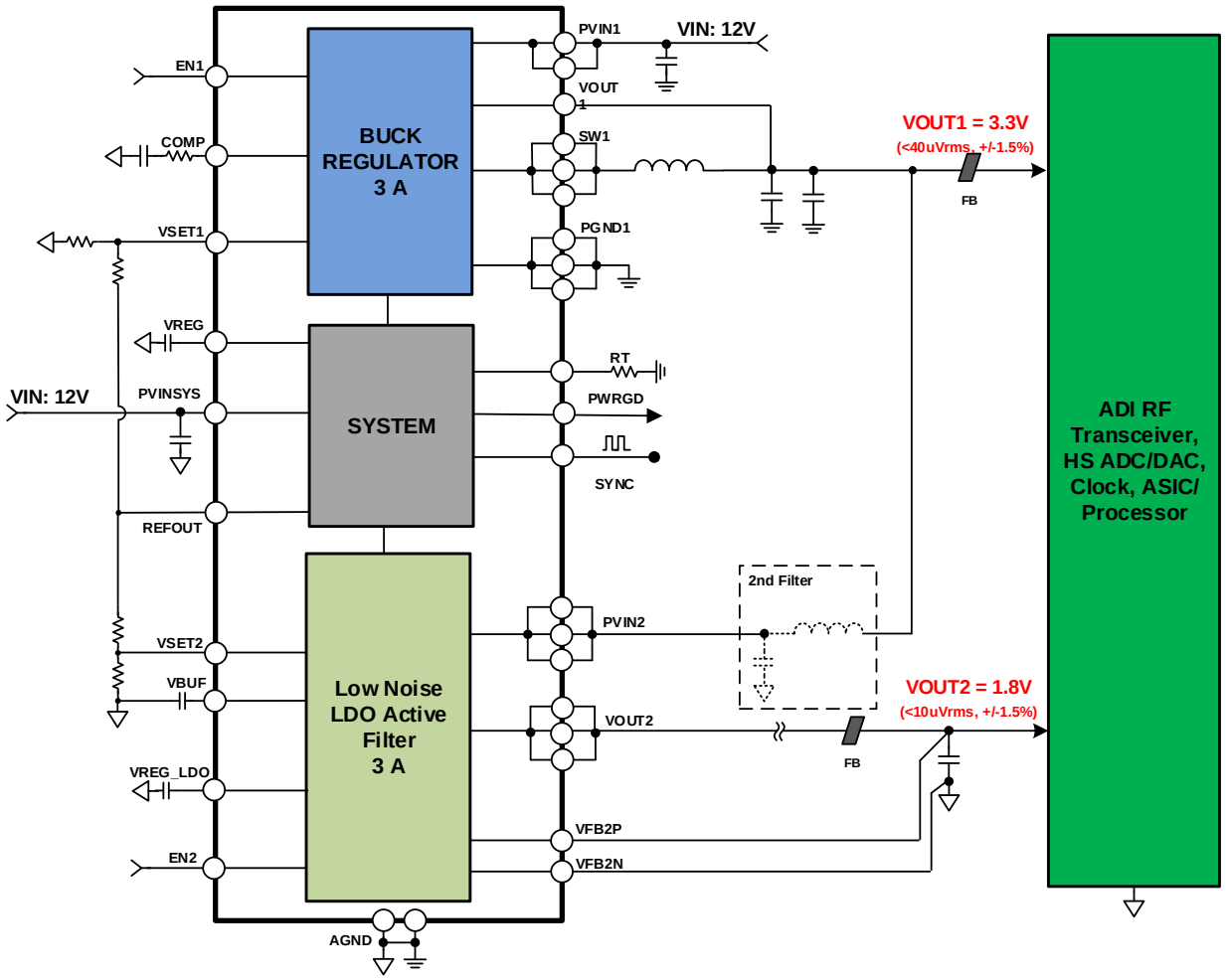


Figure 8. Independent Operation Mode (Dual Output)

COMPONENT SELECTION

Output Capacitors

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 25 V or 50 V (depending on output) are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

Calculate the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage using the following equation:

$$C_{EFFECTIVE} = C_{NOMINAL} \times (1 - TEMPCO) \times (1 - DCBIASCO) \times (1 - Tolerance)$$

where:
$C_{EFFECTIVE}$ is the effective capacitance at the operating voltage.
$C_{NOMINAL}$ is the nominal data sheet capacitance.
TEMPCO is the worst-case capacitor temperature coefficient.
DCBIASCO is the dc bias derating at the output voltage.
Tolerance is the worst-case component tolerance.

To guarantee the performance of the device, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

Capacitors with lower effective series resistance (ESR) and effective series inductance (ESL) are preferred to minimize output voltage ripple.

Input Capacitor

Higher value input capacitors help to reduce the input voltage ripple and improve transient response.

To minimize supply noise, place the input capacitor as close as possible to the relevant input pin.

LAYOUT CONSIDERATIONS

Layout is important for all switching regulators, but is particularly important for regulators with high switching frequencies. To achieve high efficiency, good regulation, good stability, and low noise, a well-designed PCB layout is required. Follow these guidelines when designing PCBs:

- Keep high current traces as short and wide as possible to minimize parasitic series inductance, which causes spiking and electromagnetic interference (EMI).
- Keep the input bypass capacitors, close to the PVIN1, PVIN2 and PVINSYS pins.
- Route the VFB2P and VFB2N LDO sense traces together connecting them at the point of load. Keep them as short as possible and away from noise sources.

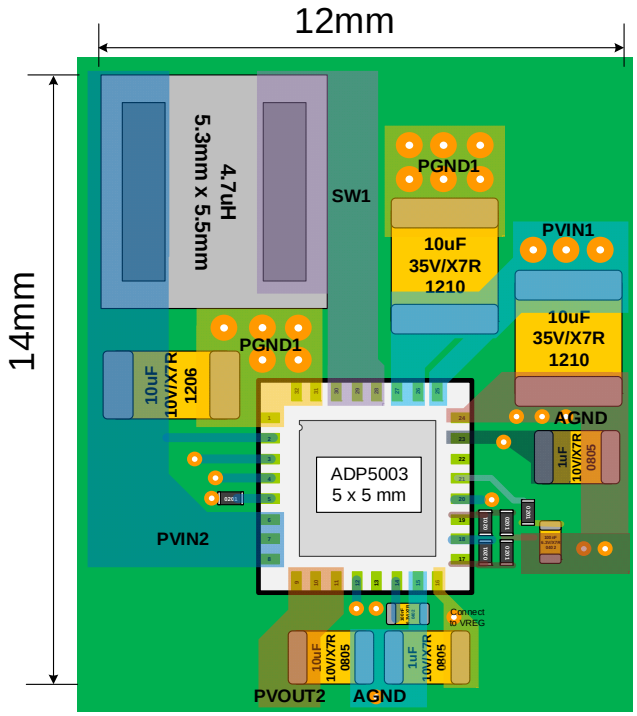
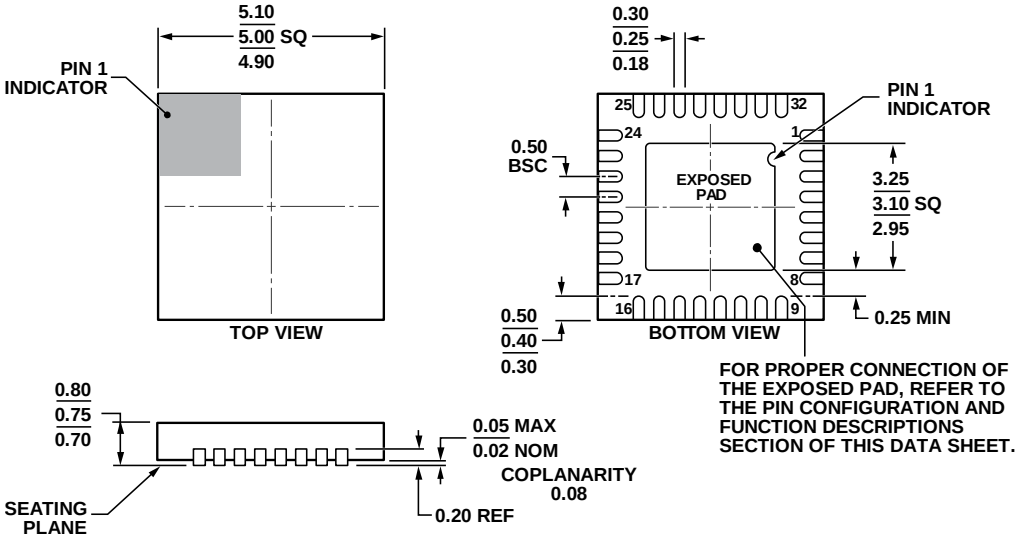


Figure 9. Example Outline Layout (Preliminary data subject to change)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 10. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5mm by 5mm Body, (CP-32-7)
Dimensions shown in millimetres