256-Channel, 24-Bit, Current-to-Digital ADC Module

Data Sheet **ADAS1135**

FEATURES

- 256-channel, current-to-digital converter module
- Up to 24-bit resolution
- Variable integration time
  - Fastest integration time: 22.6 kSPS maximum (44.2 µs minimum) at 20-bit resolution
- Low power dissipation: 2.3 mW per channel at any throughput
- Integral linearity
  - ±0.050% of reading, ±1.0 ppm of FSR: all channels active
- Very low noise
- Simultaneous sampling
  - No dead time, no loss of charge, 100% charge collection
- User adjustable full-scale range
- On-board temperature sensor and reference buffer
- 15 mm × 15 mm, CSP_BGA package
- Simple printed circuit board (PCB) design
  - Integrated capacitors for supply and reference decoupling
  - 0.80 mm pitch BGA allows low cost PCB technology
- Support tools
  - Evaluation board
  - Reference design with reference layout
  - FPGA Verilog code

APPLICATIONS

- Medical, industrial, and security CT scanner data acquisition
- Photodiode sensors
- Dosimetry and radiation therapy systems
- Optical fiber power monitoring
- X-ray detection systems
- High channel count data acquisition systems (current or voltage inputs)

GENERAL DESCRIPTION

The ADAS1135 is a 256-channel, current-to-digital, analog-to-digital converter (ADC) module. It contains 256 low power, low noise, low input current integrators, simultaneous sample-and-holds, and two high speed, high resolution ADCs with configurable sampling rate and resolutions of up to 24 bits. The signal chain and sampling architecture of the ADAS1135 is designed to guarantee that all channels are simultaneously sampled, and that no charge is lost throughout the sampling process.

All converted channel results are output on a dual, low voltage differential signaling (LVDS), self clocked serial interface, which reduces external hardware.

An SPI-compatible serial interface allows configuration of the ADC using the SDI_x input. The SDO_x output allows the user to daisy-chain several ADCs on a single, 4-wire bus. The ADAS1135 uses the separate supply, IOVDD, to reduce digital noise effect on the conversions.

The ADAS1135 is in a 15 mm × 15 mm, CSP_BGA package.

For more information on the ADAS1135, contact Analog Devices, Inc., at: adas@analog.com.

FUNCTIONAL BLOCK DIAGRAM

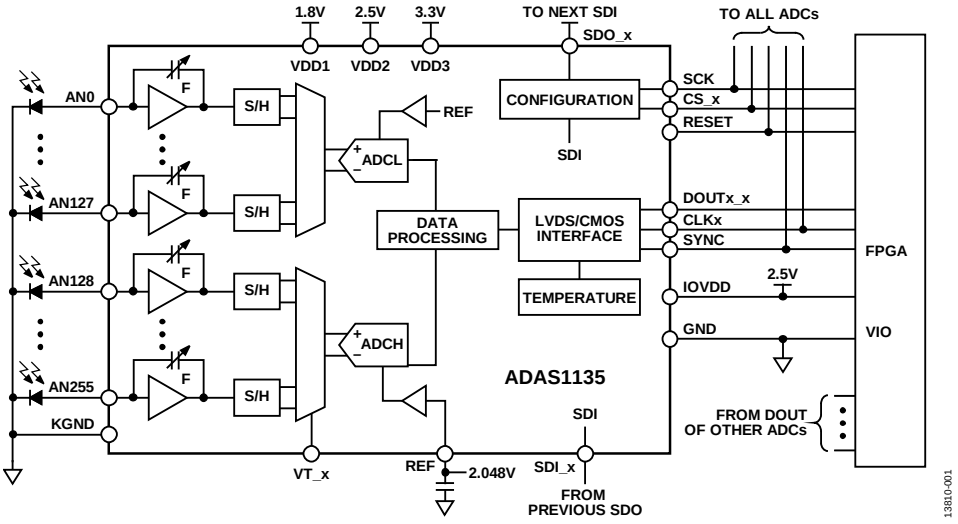

Figure 1.

Rev. SpC Document Feedback

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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Technical Support www.analog.com

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