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## FAN73933 半桥栅极驱动 IC

### 特性

- 浮动通道可实现高达 +600V 的自举运行
- 2.5A/2.5A 的典型源电流 / 灌电流驱动能力
- 将容许负  $V_S$  摆幅扩展至 -9.8V, 用于  $V_{BS}=15V$  时的信号传播
- 输出与输入信号同相
- 兼容 3.3V 和 5V 逻辑输入电平
- 适用于两个通道的匹配传播延迟
- 两个通道均内置欠压闭锁 (UVLO) 功能
- 内置共模 dv/dt 噪声消除电路
- 可编程死区时间控制功能
- $R_{DT}=0\Omega$  时, 内部最小死区时间为 220ns

### 应用

- 高速功率 MOSFET 和 IGBT 栅极驱动器
- 感应加热
- 大功率 DC-DC 转换器
- 同步降压转换器
- 电机驱动逆变器

### 说明

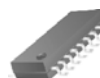
FAN73933 是一款具有关断和可编程死区控制功能的半桥栅极驱动 IC, 可驱动工作电压高达 +600V 的高速 MOSFET 和绝缘栅双极型晶体管 (IGBT)。它具有缓冲输出级, 且所有 NMOS 晶体管设计为具有高脉冲电流驱动能力和最低减少交叠导通。

飞兆半导体的高压工艺和共模噪声消除技术, 即使在较高 dv/dt 噪声环境中, 也能够保证高侧驱动器工作稳定。先进的电平转换电路, 能使高侧栅极驱动器的工作电压在  $V_{BS}=15V$  时  $V_S$  达到 -9.8V (典型值)。


UVLO 电路可防止驱动电路当  $V_{DD}$  和  $V_{BS}$  低于指定的阈值电压时发生故障。

高电流和低输出压降的特性, 使得该器件适合于不同的半桥和全桥逆变器、电机驱动逆变器、开关电源、感应加热, 以及大功率 DC-DC 转换器等应用。

14-SOP



### 订购信息

器件编号	封装	工作温度范围	 Eco 状态	包装方法
FAN73933M	14 引脚小外形集成电路 (SOIC)、 非 JEDEC、150 英寸窄体、 225SOP	-40°C 至 +125°C	RoHS	塑料管
FAN73933MX				卷带和卷盘

 对于飞兆公司的 Eco 状态定义, 请访问: [http://www.fairchildsemi.com/company/green/rohs\\_green.html](http://www.fairchildsemi.com/company/green/rohs_green.html).

应用电路图

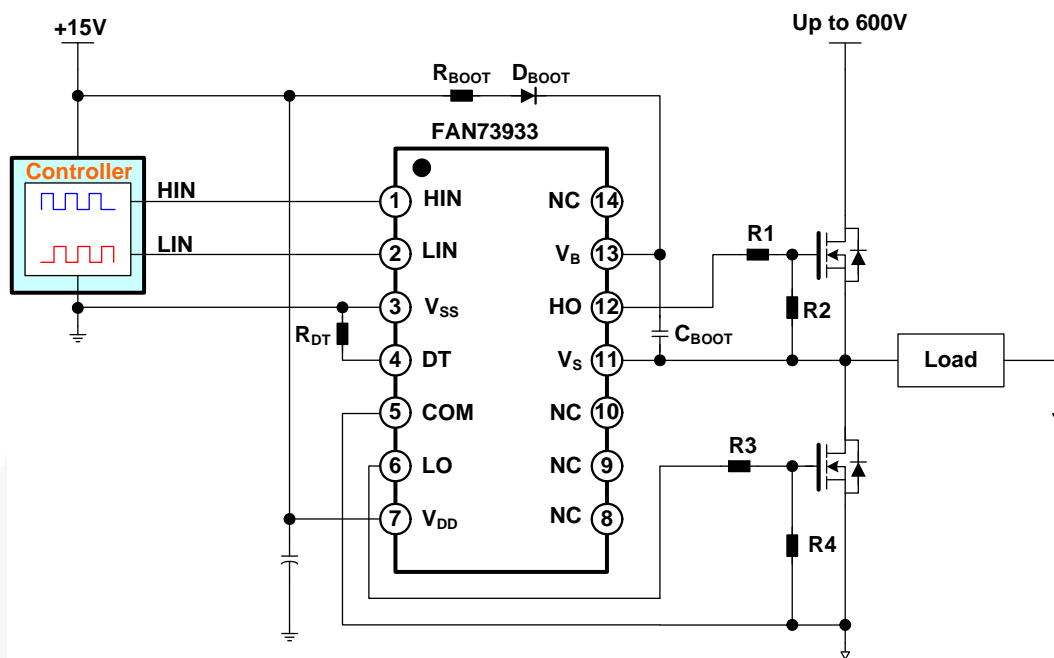


图 1. 典型应用电路

内部框图

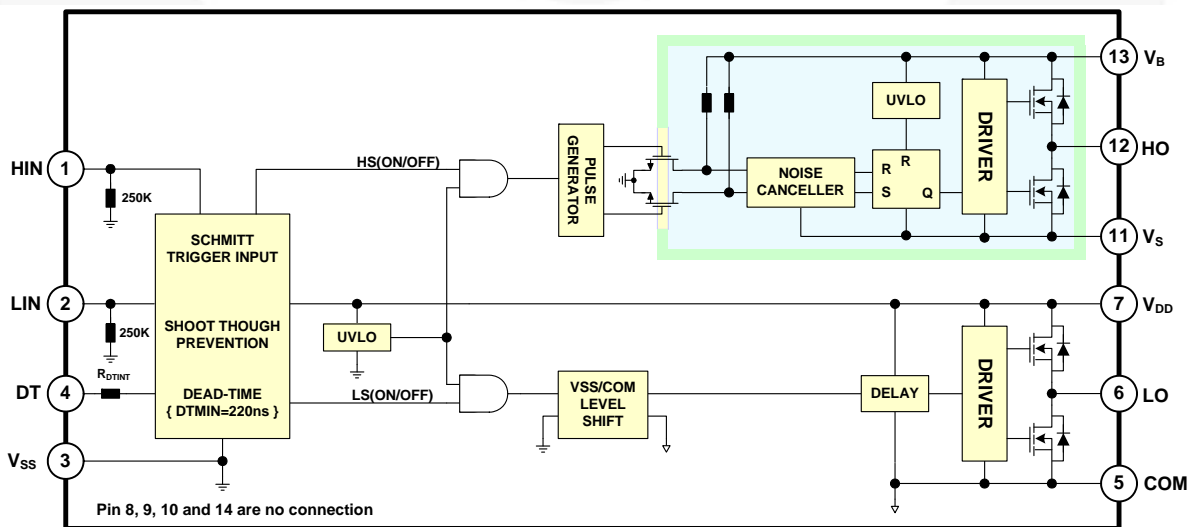


图 2. 功能框图

## 引脚布局

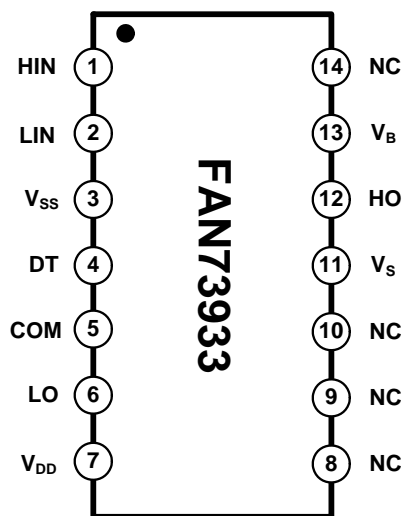


图 3. 引脚布局（顶视图）

## 引脚定义

引脚号	名称	说明
1	HIN	高侧栅极驱动器输出的逻辑输入
2	LIN	低侧栅极驱动器输出的逻辑输入
3	V <sub>SS</sub>	逻辑地
4	DT	外接电阻进行死区控制（参考 V <sub>SS</sub> ）
5	COM	接地
6	LO	低侧栅极驱动输出
7	V <sub>DD</sub>	电源电压
8	NC	无连接
9	NC	无连接
10	NC	无连接
11	V <sub>S</sub>	高压浮地
12	HO	高侧驱动输出
13	V <sub>B</sub>	高侧浮动电源
14	NC	无连接

## 绝对最大额定值

应力超过绝对最大额定值，可能会损坏器件。在超出推荐的工作条件的情况下，该器件可能无法正常工作，所以不建议让器件在这些条件下长期工作。此外，在远高于推荐的工作条件下工作，会影响器件的可靠性。绝对最大额定值仅是应力规格值。除非另有说明， $T_A=25^{\circ}\text{C}$ 。

符号	特性	最小值	最大值	单位
$V_B$	高侧浮动电源电压	-0.3	625.0	V
$V_S$	高侧浮动偏置电压	$V_B-25.0$	$V_B+0.3$	V
$V_{HO}$	高侧浮动输出电压	$V_S-0.3$	$V_B+0.3$	V
$V_{LO}$	低侧输出电压	-0.3	$V_{DD}+0.3$	V
$V_{DD}$	低侧和固定逻辑电源电压	-0.3	25.0	V
$V_{IN}$	逻辑输入电压 (HIN, LIN)	-0.3	$V_{DD}+0.3$	V
DT	可编程死区时间引脚电压	-0.3	$V_{DD}+0.3$	V
$V_{SS}$	逻辑地	$V_{DD}-25$	$V_{DD}+0.3$	V
$dV_S/dt$	允许的偏置电压变化速率		$\pm 50$	V/ns
$P_D$	功率耗散 <sup>(1, 2, 3)</sup>		1	W
$\theta_{JA}$	热阻		110	$^{\circ}\text{C}/\text{W}$
$T_J$	结温		+150	$^{\circ}\text{C}$
$T_{STG}$	存储温度	-55	+150	$^{\circ}\text{C}$

### 注意：

- 1 安装到 76.2 x 114.3 x 1.6mm PCB 板 (FR-4 环氧玻璃材料)。
- 2 参照下列标准：  
JESD51-2: 集成电路热测试方法环境条件 – 自然通风；  
JESD51-3: 含铅表面贴装封装的低有效导热系数测试板。
- 3 在任何情况下，都不要超过  $P_D$ 。

## 推荐工作条件

推荐的操作条件表定义了器件的真实工作条件。指定推荐的工作条件，以确保器件的最佳性能达到数据表中的规格。飞兆不建议超出额定或依照绝对最大额定值进行设计。

符号	参数	最小值	最大值	单位
$V_B$	高侧浮动电源电压	$V_S+10$	$V_S+20$	V
$V_S$	高侧浮动电源偏置电压	$6-V_{DD}$	600	V
$V_{HO}$	高侧输出电压	$V_S$	$V_B$	V
$V_{DD}$	低侧和固定逻辑电源电压	10	20	V
$V_{LO}$	低侧输出电压	COM	$V_{DD}$	V
$V_{IN}$	逻辑输入电压 (HIN, LIN)	$V_{SS}$	$V_{DD}$	V
DT	可编程死区时间引脚电压	$V_{SS}$	$V_{DD}$	V
$V_{SS}$	逻辑地	-5	+5	V
$T_A$	工作环境温度	-40	+125	$^{\circ}\text{C}$

## 电气特性

$V_{BIAS}(V_{DD}, V_{BS})=15.0V$ ,  $V_{SS}=COM=0V$ ,  $DT=V_{SS}$  且  $T_A = 25^\circ C$ , 除非另有说明参数  $V_{IN}$  和  $I_{IN}$  以  $0 V_{SS}/COM$  为参考, 并适用于相应的输入引脚: HIN 和 LIN。参数  $V_O$  和  $I_O$  以 COM 为参考, 并适用于相应的输出引脚: HO 和 LO。

符号	特性	测试条件	最小值	典型值	最大值	单位
<b>电源部分</b>						
$I_{QDD}$	VDD 电源静态电流	$V_{IN}=0V$ 或 $5V$		0.9	1.5	mA
$I_{QBS}$	VBS 静态电源电流	$V_{IN}=0V$ 或 $5V$		50	100	$\mu A$
$I_{PDD}$	VDD 电源工作电流	$f_{IN}=20KHz$ , 无负载		1.3	1.9	mA
$I_{PBS}$	VBS 电源静态电流	$C_L=1nF$ , $f_{IN}=20KHz$ , rms		450	800	$\mu A$
$I_{LK}$	偏置漏电流	$V_B=V_S=600V$			10	$\mu A$
<b>自举电源部分</b>						
$V_{DDUV+}$ $V_{BSUV+}$	$V_{DD}$ 和 $V_{BS}$ 电源欠压正向 (电压从高到低) 阈值电压	$V_{IN}=0V$ , $V_{DD}=V_{BS}=Sweep$	8.0	9.0	10	V
$V_{DDUV-}$ $V_{BSUV-}$	$V_{DD}$ 和 $V_{BS}$ 电源欠压负向 (电压从低到高) 阈值电压	$V_{IN}=0V$ , $V_{DD}=V_{BS}=Sweep$	7.4	8.4	9.4	V
$V_{DDUVH}$ $V_{BSUVH}$	$V_{DD}$ 和 $V_{BS}$ 电源欠压锁定滞回电压回差	$V_{IN}=0V$ , $V_{DD}=V_{BS}=Sweep$		0.6		V
<b>输入逻辑部分</b>						
$V_{IH}$	逻辑“1”输入电压适用于 HO, 逻辑“0”适用于 LO		2.5			V
$V_{IL}$	逻辑“0”输入电压适用于 HO, 逻辑“1”适用于 LO				0.8	V
$I_{IN+}$	逻辑输入高偏置电流	$V_{IN}=5V$		20	50	$\mu A$
$I_{IN-}$	逻辑输入低偏置电流	$V_{IN}=0V$			2	$\mu A$
$R_{IN}$	逻辑输入下拉电阻		100	250		K $\Omega$
<b>栅级驱动输出部分</b>						
$V_{OH}$	高电平输出电压 ( $V_{BIAS} - V_O$ )	无负载			1.5	V
$V_{OL}$	低电平输出电压	无负载			100	mV
$I_{O+}$	输出高电平短路脉冲电流 <sup>(4)</sup>	$V_{HO}=0V$ , $V_{IN}=5V$ , $PW \leq 10\mu s$	2.0	2.5		A
$I_{O-}$	输出低电平短路脉冲电流 <sup>(4)</sup>	$V_{HO}=15V$ , $V_{IN}=0V$ , $PW \leq 10\mu s$	2.0	2.5		A
$V_S$	允许的做为输入信号传播到 HO 的 $V_S$ 负电压			-9.8	-7.0	V

注:

4. 这些参数由设计者确定。

## 动态电气特性

$V_{BIAS}(V_{DD}, V_{BS})=15.0V$ ,  $V_{SS}=COM=0V$ ,  $C_L=1000pF$ ,  $DT=V_{SS}$  且  $T_A=25^\circ C$ , 除非另有说明。

符号	参数	工作条件	最小值	典型值	最大值	单位
$t_{ON}$	导通传播延时 <sup>(5)</sup>	$V_S=0V$ , $R_{DT}=0\Omega$		160	230	ns
$t_{OFF}$	关断传播延时	$V_S=0V$		160	230	ns
$Mt_{ON}$	延时匹配, HO 与 LO 导通			0	50	ns
$Mt_{OFF}$	延时匹配, HO 与 LO 关断			0	50	ns
$t_R$	开通上升时间	$V_S=0V$		40	60	ns
$t_F$	关断下降时间	$V_S=0V$		20	35	ns
DT	死区时间: LO 关断至 HO 导通, 以及 HO 关断至 LO 导通	$R_{DT}=0\Omega$	170	220	270	ns
		$R_{DT}=300K\Omega$	400	500	600	ns
MDT	死区时间匹配 $= DT_{LO-HO} - DT_{HO-LO} $	$R_{DT}=0\Omega$		0	50	ns
		$R_{DT}=300K\Omega$		0	100	ns

注:

5 导通传播延时不包括死区时间

典型特性

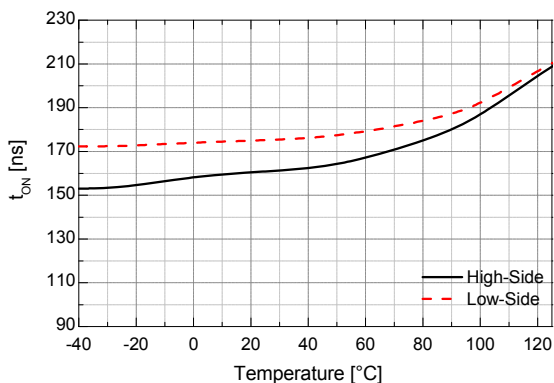


图 4. 导通传播延时与温度的关系

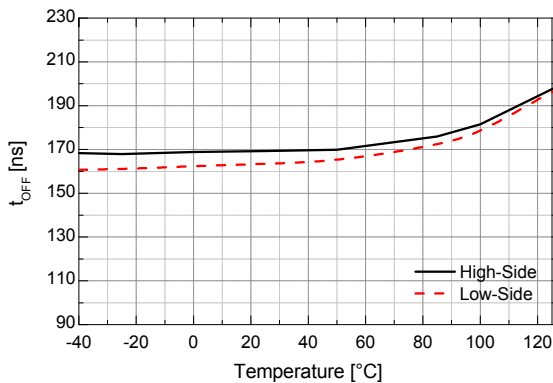


图 5. 关断传播延时与温度的关系

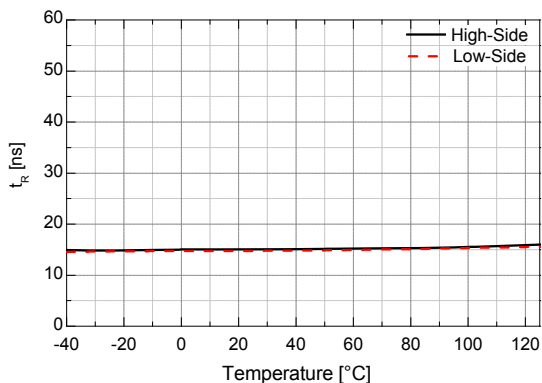


图 6. 导通上升时间与温度的关系

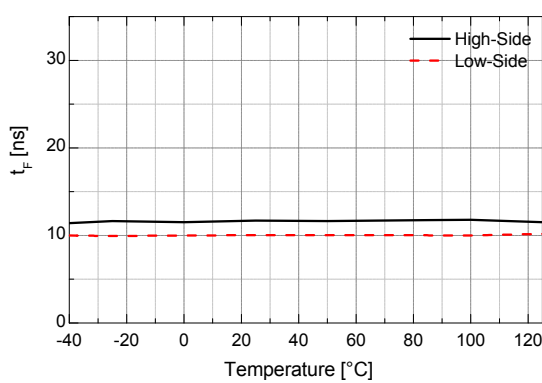


图 7. 关断下降时间与温度的关系

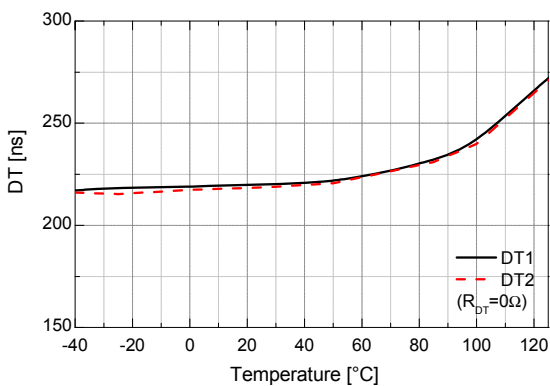


图 8. 死区时间 ( $R_{DT}=0\Omega$ ) 与温度的关系

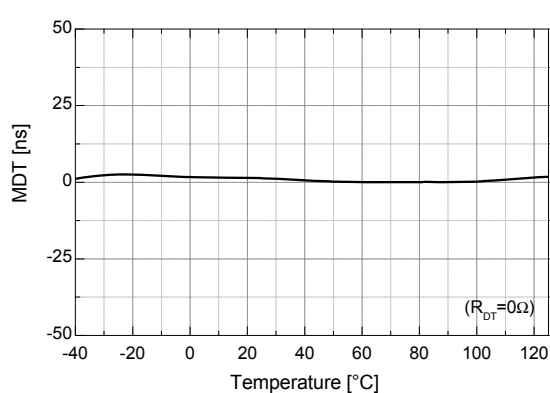


图 9. 死区时间匹配 ( $R_{DT}=0\Omega$ ) 与温度的关系



典型特性 (续)

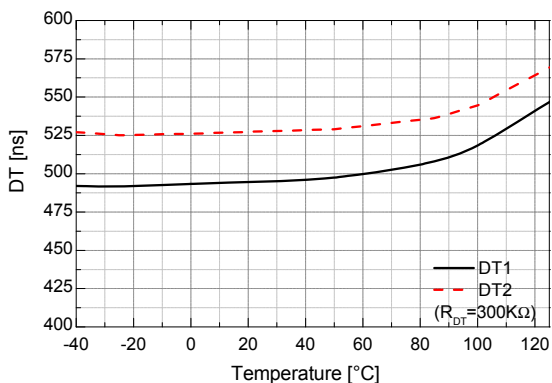


图 10. 死区时间 (R<sub>DT</sub>=300KΩ) 与温度的关系

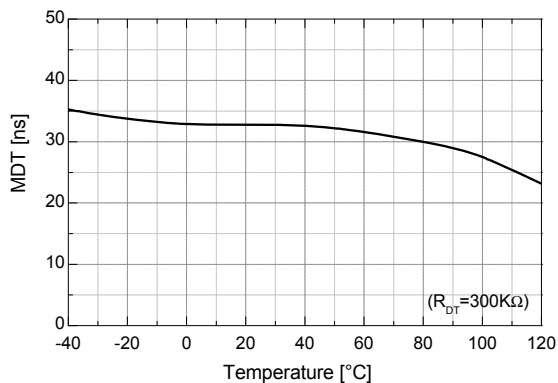


图 11. 死区时间匹配 (R<sub>DT</sub>=300KΩ) 与温度的关系

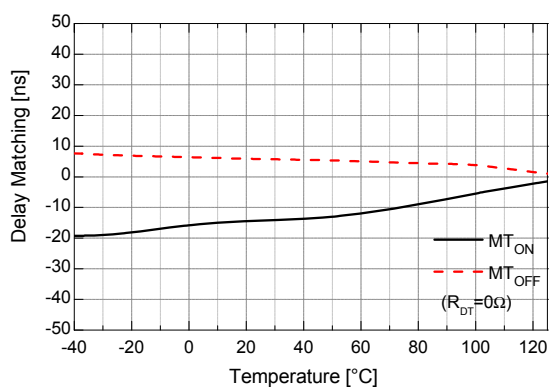


图 12. 延迟匹配与温度的关系

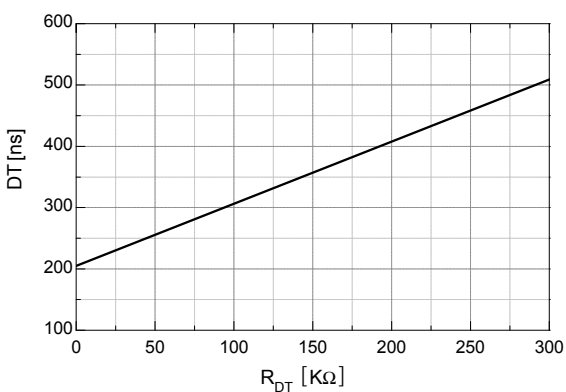


图 13. 死区时间与 R<sub>DT</sub>

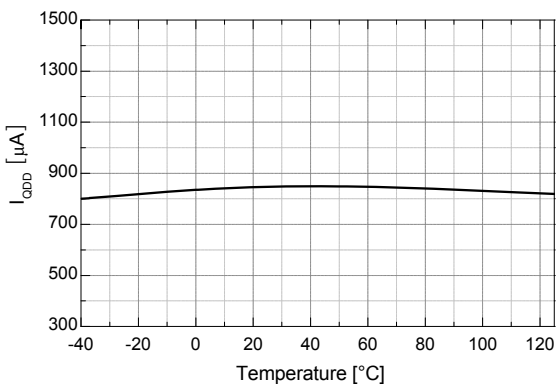


图 14. 静态 V<sub>DD</sub> 电源电流与温度的关系

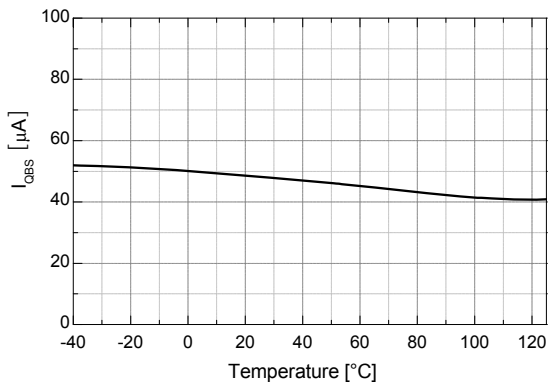


图 15. 静态 V<sub>BS</sub> 电源电流与温度的关系

典型特性 (续)

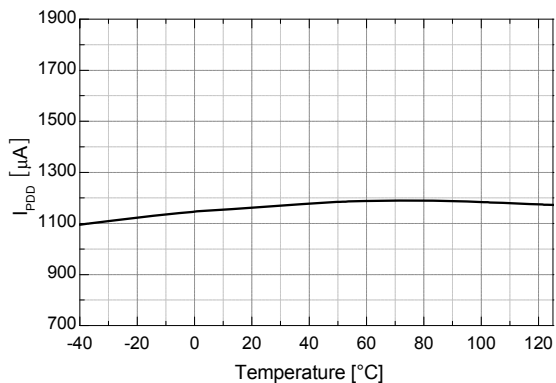


图 16. 工作时  $V_{DD}$  电源电流与温度的关系

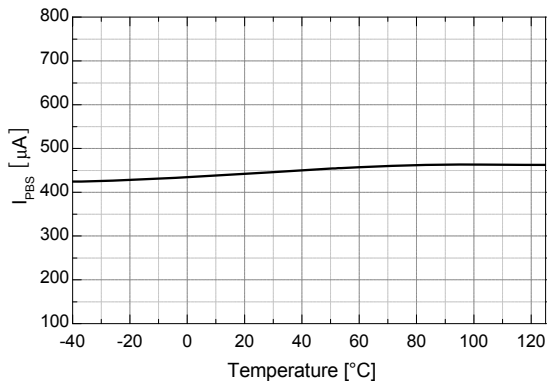


图 17. 工作时  $V_{BS}$  电源电流与温度的关系

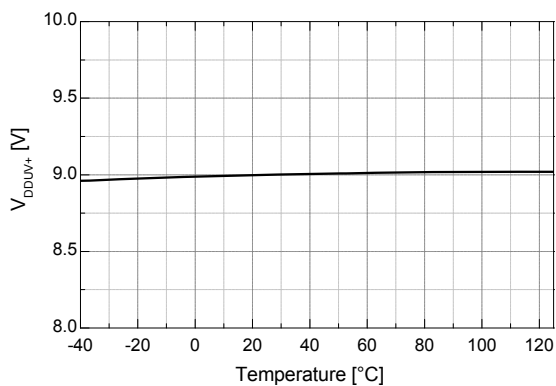


图 18.  $V_{DD}$  UVLO+ 与温度的关系

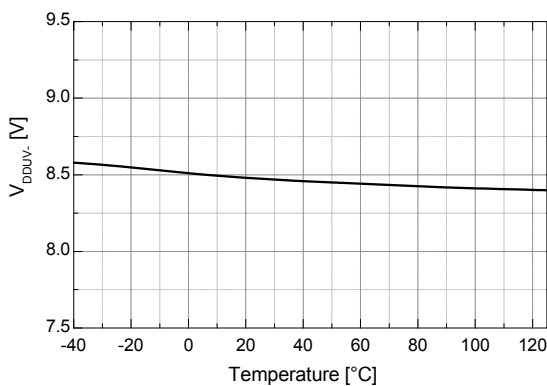


图 19.  $V_{DD}$  UVLO- 与温度的关系

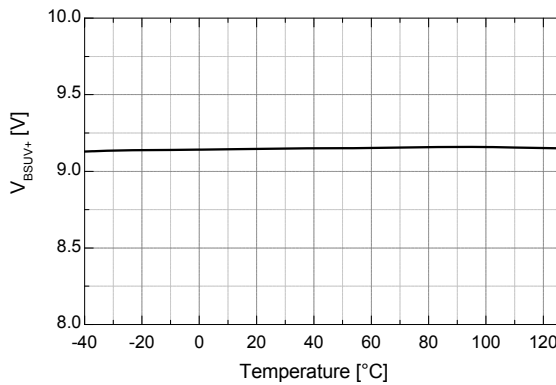


图 20.  $V_{BS}$  UVLO+ 与温度的关系

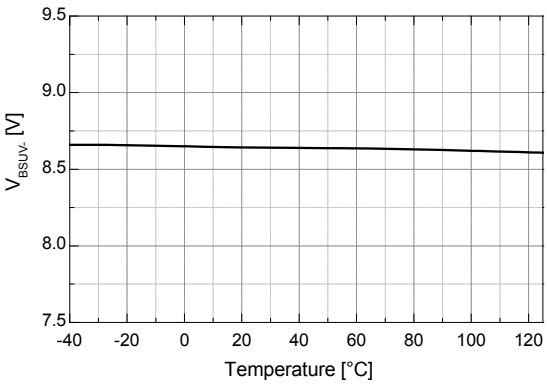


图 21.  $V_{BS}$  UVLO- 与温度的关系

典型特性 (续)

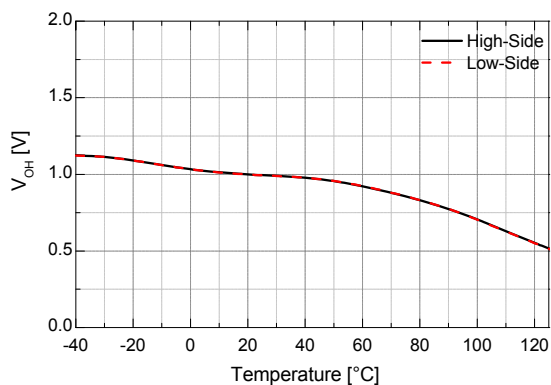


图 22. 高电平输出电压与温度的关系

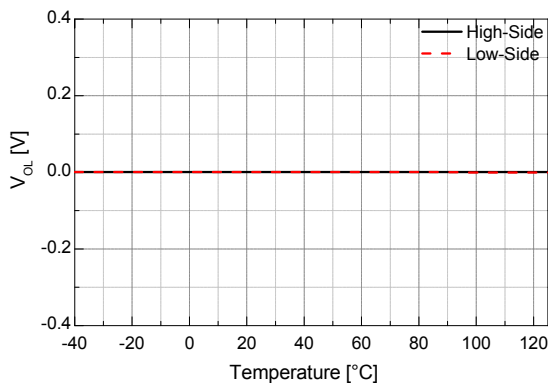


图 23. 低电平输出电压与温度的关系

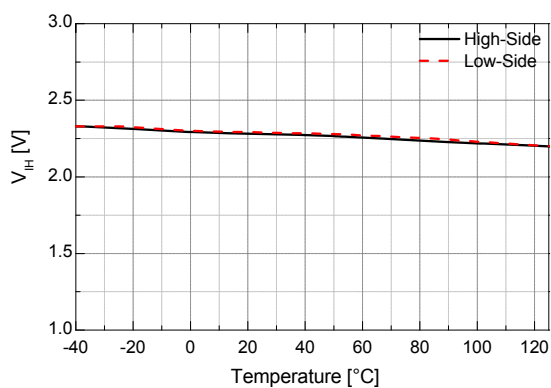


图 24. 逻辑高电平输入电压与温度的关系

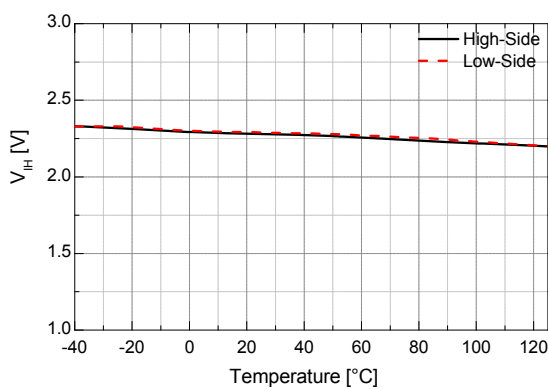


图 25. 逻辑低电平输入电压与温度的关系

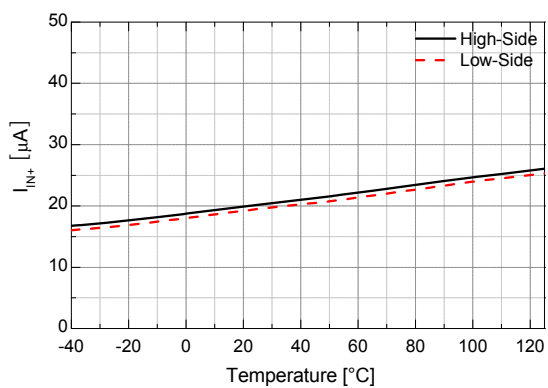


图 26. 逻辑输入高电平偏置电流与温度的关系

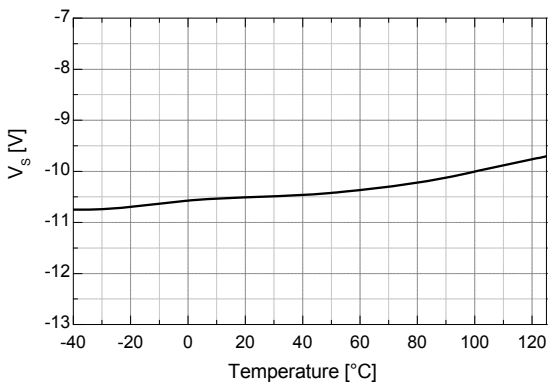


图 27. 容许的负  $V_S$  电压与温度的关系

典型特性 (续)

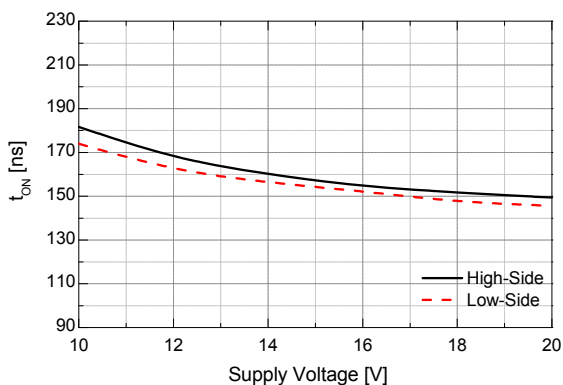


图 28. 导通传播延迟与电源电压的关系

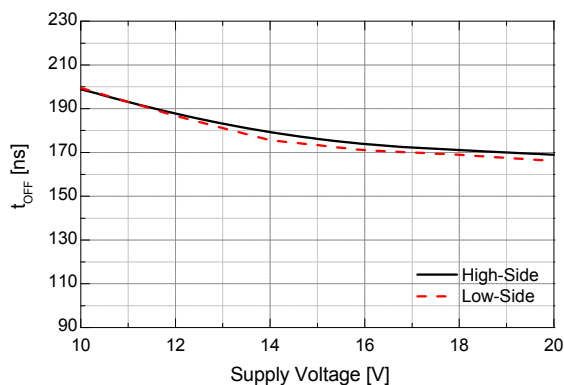


图 29. 关断传播延迟与电源电压的关系

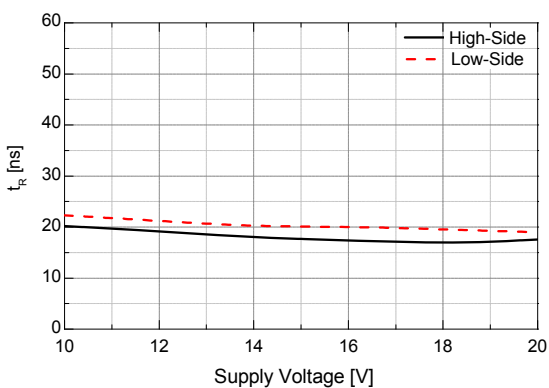


图 30. 导通上升时间与电源电压的关系

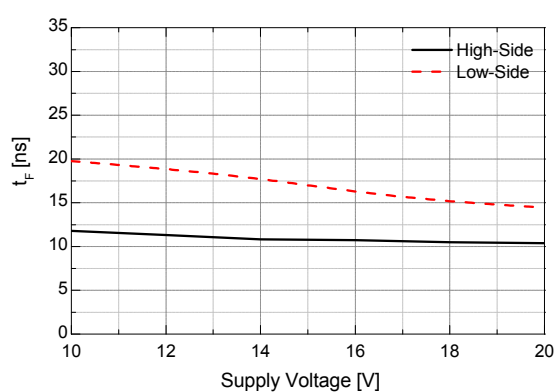


图 31. 关断下降时间与电源电压的关系

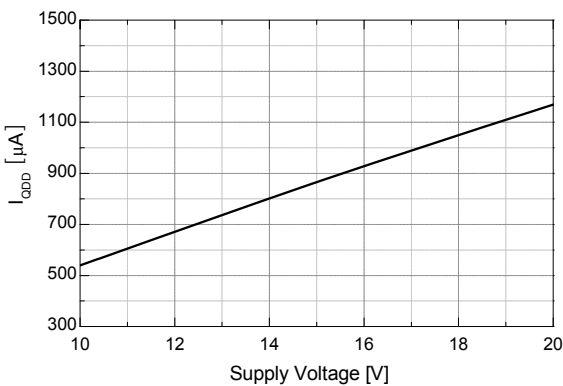


图 32. 静态  $V_{DD}$  电源电流与电源电压的关系

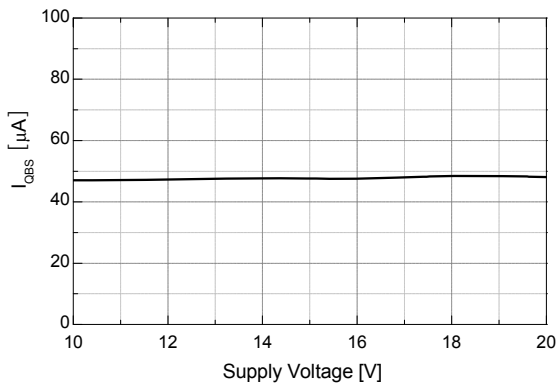


图 33. 静态  $V_{BS}$  电源电流与电源电压的关系

典型特性 (续)

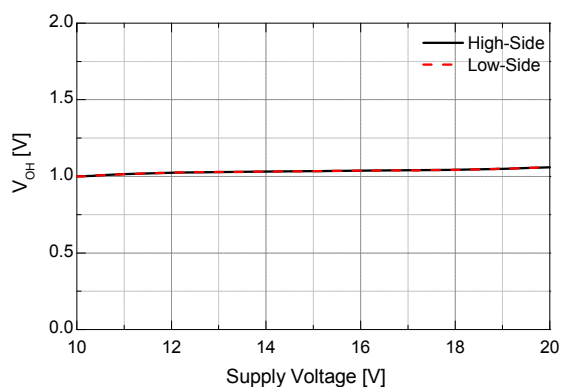


图 34. 高电平输出电压与电源电压的关系

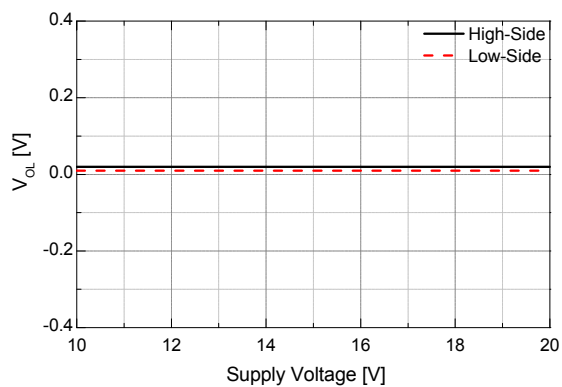


图 35. 低电平输出电压与电源电压的关系

### 开关时间定义

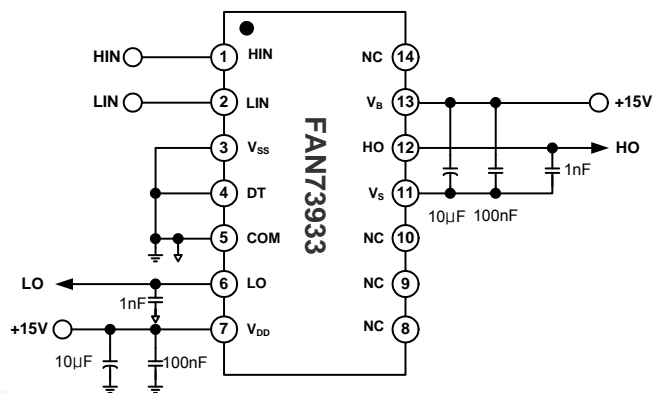


图 36. 开关时间测试电路

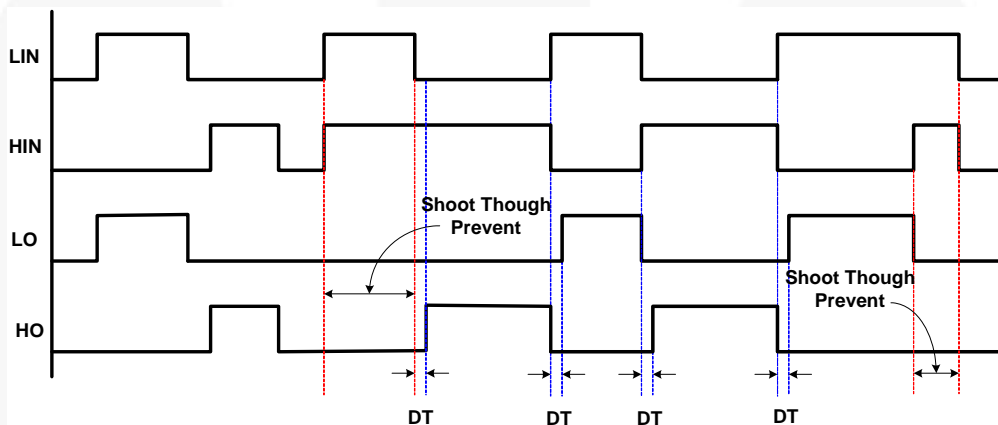


图 37. 输入 / 输出时序图

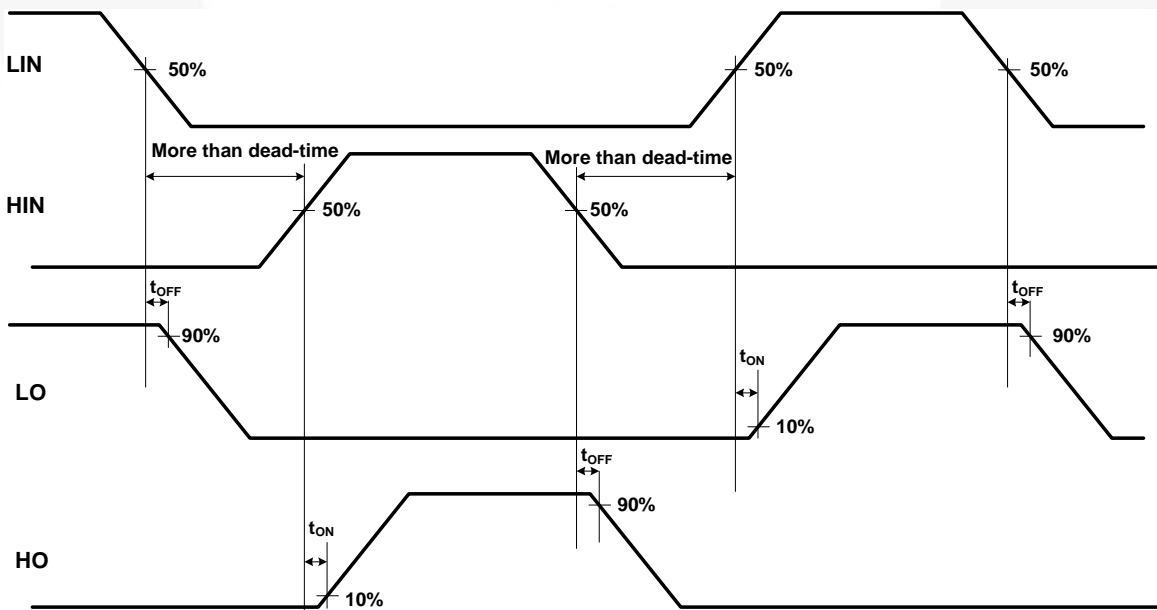


图 38. 开关时间波形定义

## 应用信息

### 瞬变 $V_S$ 负电压

自举电路具有简单和低成本的优点，但是，它也有一些局限。此电路的最大难题是，在半桥应用中，高侧的开关器件关断时在其发射极存在负电压。

如果高侧开关 Q1 关断，同时负载电流流向电感负载；从高侧开关 Q1 至二极管 D3（与同一逆变器桥的低侧开关并联）出现电流转移。然后，负电压出现在高侧开关器件的发射极，在续流二极管开始箝位前，负载电流突然流向低侧续流二极管 D3，如图 39. 所示：

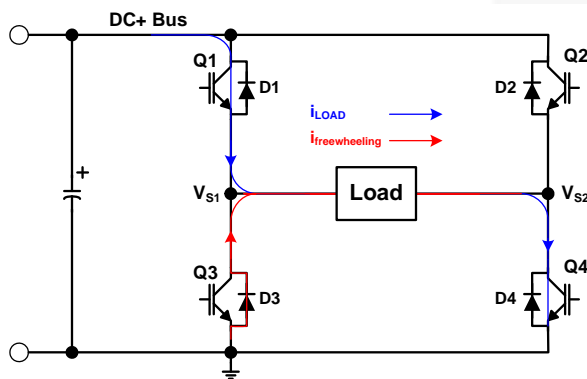


图 39. 半桥应用电路

此负电压给栅极驱动器输出时带来麻烦。很可能产生自举电容过压的情况，输入信号丢失以及闭锁问题，因为它直接影响栅极驱动器的电源  $V_S$  引脚，如图 40. 所示。此负尖峰电压称为“瞬变  $V_S$  负电压”。

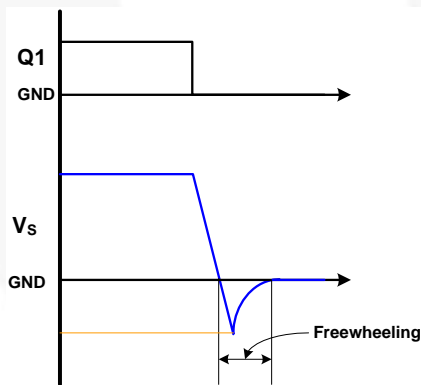


图 40. Q1 关断期间的  $V_S$  波形

图 41. 和图 42. 显示了同一逆变桥中，高侧开关 Q1 和低侧续流二极管 D3 间的负载电流换流。逆变电路中从裸片引脚绑定到 PCB 走线的寄生电感对于每个 IGBT 的就是  $L_C$  和  $L_E$ 。当高侧开关 Q1 和低侧开关 Q4 导通时，由于负载电流从 Q1 流向 Q4， $V_{S1}$  节点电压低于  $DC+$  电压（跟电路的电源开关和寄生电感相关的电压降有关）如图 41. 所示；当高侧开关 Q1 关断而 Q4 仍然导通时，由于  $V_{S1}$  连有感性负载，负载电流通过低侧续流二极管 D3 续流，如图 42. 所示。电流从地（连接至栅极驱动器的 COM 引脚）流向负载，且负电压出现在高侧开关器件的发射极。

在此情况下，栅极驱动器的 COM 引脚电势高于  $V_S$  引脚，因为电压降与续流二极管 D3、寄生元件  $L_{C3}$  和  $L_{E3}$  相关。

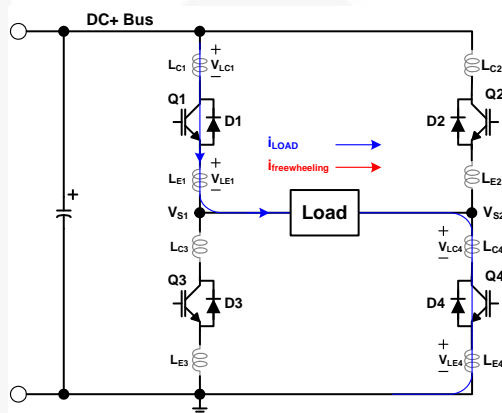


图 41. Q1 和 Q4 导通

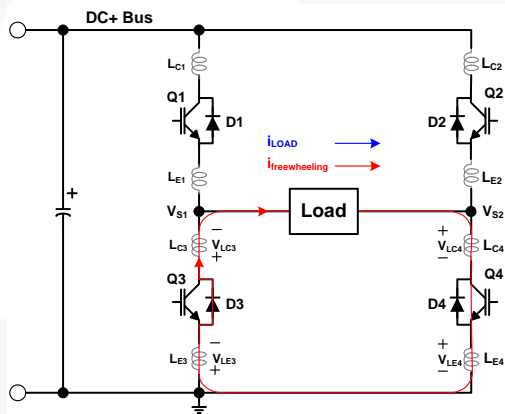


图 42. Q1 关断且 D3 导通

FAN73933 具有负极性  $V_S$  瞬变性能曲线，如图 43. 所示

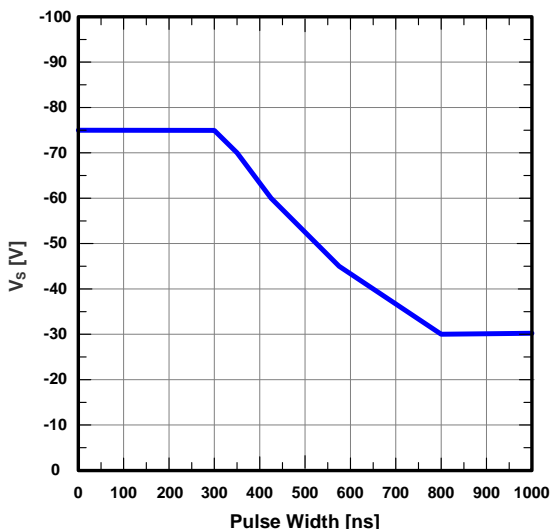


图 43. 瞬变  $V_S$  负电压特性

即使所示 FAN73933 能够处理这些负极性  $V_S$  瞬变情况，仍然强烈建议电路设计人员通过谨慎处理电路板布局，最大限度地减小寄生参数，从而尽可能限制该瞬变  $V_S$  负电压。负性  $V_S$  电压的振幅与开关器件的寄生电感、关断速度、 $di/dt$  成正比。

## 一般准则

### 印刷电路板布局

为了最大限度地减少寄生元件，建议如下电路板布局：

- 开关之间的走线没有回路或偏差。
- 避免互连链路。它会显著增加电感。
- 降低封装体距离 PCB 板的高度，以减少引脚电感效应。
- 考虑所有功率开关的配合放置，以减少走线长度。
- 为了最大限度地减少噪声耦合，接地层不应置于高压浮置侧下方或附近。
- 为了减少 EM 耦合及改善电源开关导通 / 关断性能，必须尽可能减少栅极驱动环路。

## 元件布置

建议选择如下所示元件：

- 在  $V_{DD}$  和  $V_{SS}$  引脚之间放置旁路电容。1 $\mu$ F 陶瓷电容适用于大多数应用。此元件应尽可能靠近引脚放置，以减少寄生元件。
- $V_{DD}$  和 COM 之间的旁路电容同时支持低侧驱动器和自举电容的再充电。建议该电容值至少是自举电容的十倍以上。
- 在量化自举阻抗和初次自举充电时的电流时，必须考虑自举电阻  $R_{BOOT}$ 。如果电阻需要与自举二极管并联，请确认  $V_B$  不会下降至低于 COM（接地）。通常建议采用 5 ~ 10 $\Omega$ ，这可增加  $V_{BS}$  时间常量。如果自举电阻和二极管间的电压降太大或电路拓扑不能提供足够的充电时间，我们可以使用一个快速恢复或超快恢复二极管。
- 自举电容  $C_{BOOT}$  使用一个低 ESR 电容，比如陶瓷电容。

强烈建议如下布置元件：

- 布置元件连接到浮动电压引脚 ( $V_B$  和  $V_S$ )，靠近器件和 FAN73933 各自的高压部分。此封装中的 NC（非连接）引脚应最大化高压和低压引脚之间的距离，如 (see 图 3.) 所示。
- 旁路电容和栅极电阻的布局和布线，应尽可能靠近栅极驱动 IC。
- 使自举二极管  $D_{BOOT}$  尽可能靠近自举电容  $C_{BOOT}$ 。
- 自举二极管必须使用有较低的正向压降和开关时间很快的快恢或超快恢复二极管。



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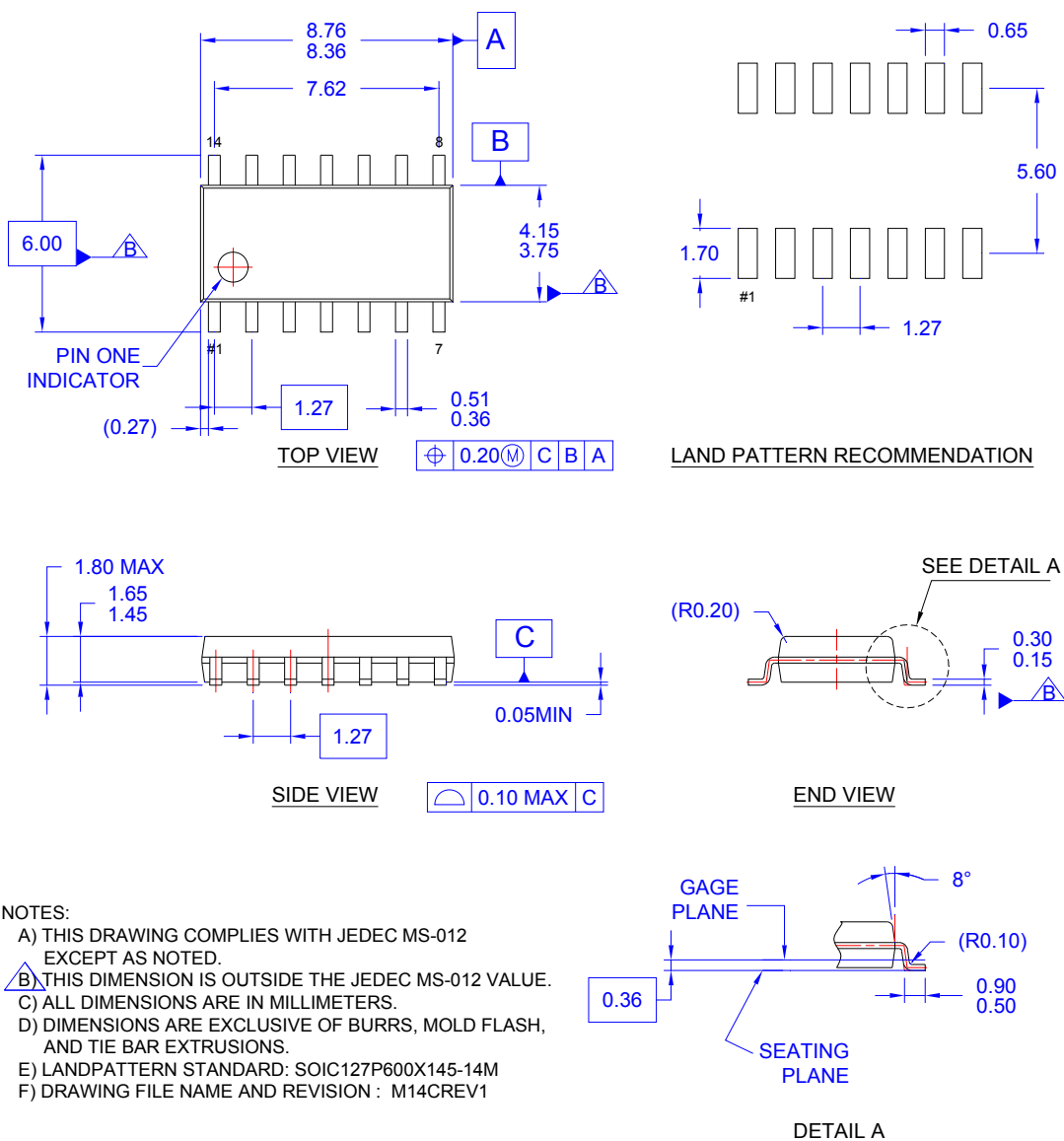


图 44.14 引脚、小外形集成电路 (SOIC)、非 JEDEC、150 英寸窄体、225SOP

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