LC786965UW

Single Chip Digital Signal Processor LSI for Compact Disc Players

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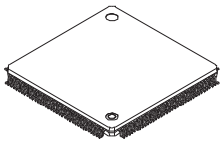


SPQFP144 20x20 / SQFP144

Overview

The LC786965UW integrates ARM7TDMI-S™, CD servo control, CD signal processing, compressed audio decode processing, audio signal processing in a package. Furthermore, various kinds of interface functions such as SIO, UART etc. reduce the external main controller's processing load and make high performance and much functional CD player system, using with less components.

Features

- RF signal processing for CD-DA/R/RW, servo control, EFM signal processing, and anti-shock processing
- MP3*, WMA*, AAC* decoder processing
- Sampling rate convertor, and other various audio signal processing
- ARM7TDMI-S™ as internal CPU core, Mask-ROM for program storage
- Host controller interface with SIO, I^2C

Applications

- Car Navigation
- Car Audio
- Home Audio System
- Mobile CD system

* MP3
  MPEG Layer-3 Audio Coding
* WMA
  Windows Media Audio
* AAC
  Advanced Audio Coding

Detail of Functions

[CD DSP functions]

<Playback functions>

- Playback mode: CLV playback/Jitter free playback (VCEC)
- Playback speed: Normal speed, double speed , Quadruple speed

<RF Processing block>

- RF system:AGC, CD-R and CD-R/W playback support, peak hold, bottom hold
- Error system: TE signal generation, FE signal generation
- Detection: Track count signal, Jitter, Defect (black, mirror)
- LASER power controller (APC)
- DC offset voltage cancellation

<Servo control block>

- All servo systems as tracking, focus, sled and spindle are implemented with digital processing.
- Automatic adjustment functions: focus gain, focus bias, focus offset, tracking gain, tracking offset and tracking balance
- Shock detection / Interruption detection

<CD signal processing block>

- EFM signal synchronization detection, protection and interpolation
- Error detection, correction (C1=double, C2=quadruple/double)
- Jitter margin ±19 frames

<CD TEXT processing block>

- Buffers CD-TEXT data to the desired area of SDRAM
- Starts buffering desired ID3/ID4 of CD-TEXT data.

<CD-DA Anti-shock processing block>

- Anti-shock processing using with SDRAM
  Maximum about 10 seconds with 16M bit SDRAM and about 40 seconds with 64M bit SDRAM

<CD-ROM processing block>

- CD-ROM decoding (Mode1, Mode2 <form1, form2>)
- Outputs CD-ROM decoded data

[Compressed audio decode functions]

- MP3 decode (ISO/IEC 11172-3, ISO/IEC 13818-3)
  - Sampling rate support: MPEG1-Layer1/2/3 (32kHz, 44.1kHz, 48kHz)
    MPEG2-Layer1/2/3 (16kHz, 22.05kHz, 24kHz)
    MPEG2.5-Layer3 (8kHz, 11.025kHz, 12kHz)
  - Bit rate support: All Bit Rate (Variable Bit Rate support)
  - MPEG header read support
- WMA decode (Version 9 standard)
  - Sampling rate support: 8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz, 44.1kHz, 48kHz
  - Bit rate support: 5kbps to 384kbps (Variable Bit Rate support)
- AAC decode (ISO/IEC 14496-3, ISO/IEC 13818-7)
  - Profile: MPEG4-AAC-LowComplexity
  - Sampling rate support: 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz
  - Bit rate support: Monaural 8kbps to 160kbps (Variable bit rate support)
    Stereo 16kbps to 320kbps (Variable bit rate support)

[Audio processing functions]

<Audio processing block>

- Sampling rate converter (SRC) for compressed audio data playback
- Interpolation (CD-DA only)
- Digital attenuator
- Bilingual function
- Mute function (−12dB, −∞)
- De-emphasis filter
- Bass / Treble filter

<Interface block>

- Various external audio data output format
  IIS (48fs/64fs), MSB first right justified (32fs/48fs/64fs), 16 bit data length

[Internal Microcontroller functions]

<Sequencer control>

- CD playback control
  Servo control, CD anti-shock playback control, CD-ROM file analysis, etc.

<Communication control between main controller>

- Communication format: SIO, I^2C

<Peripheral interface block>

- GPIO port 20ports maximum (Shared with other functions.)
- External interrupt pins 4pins maximum (Shared with other functions.)
- Serial interface

SIO	clock synchronized full duplex (3 lines)	1 channel
UART	full duplex	1 channel

<Program memory block>

- Mask-ROM size: 256kB
- ROM Collect function is built in for the partial change of the program and Host controller can use this.

<Others>

- System Clock
  1'Xtal (16.9344MHz)
- Watch Dog Timer
  Notify to outside from pin or reset internally.
- Power management
  2 kinds of sleep mode
  (1) Only CPU core operates at slow clock and clocks for other blocks are stopping.
  (2) All clocks are stopping.

[Others]

<External memory>

- External SDRAM Memory size : 16Mbit or 64Mbit
  Data width : 16bit
  CAS latency : 2
  Burst length : Full

  Used for CD-DA anti-shock control, CD-ROM decoding.

<Internal power supply>

- 1.2V regulator for internal blocks

Sample Application Circuit

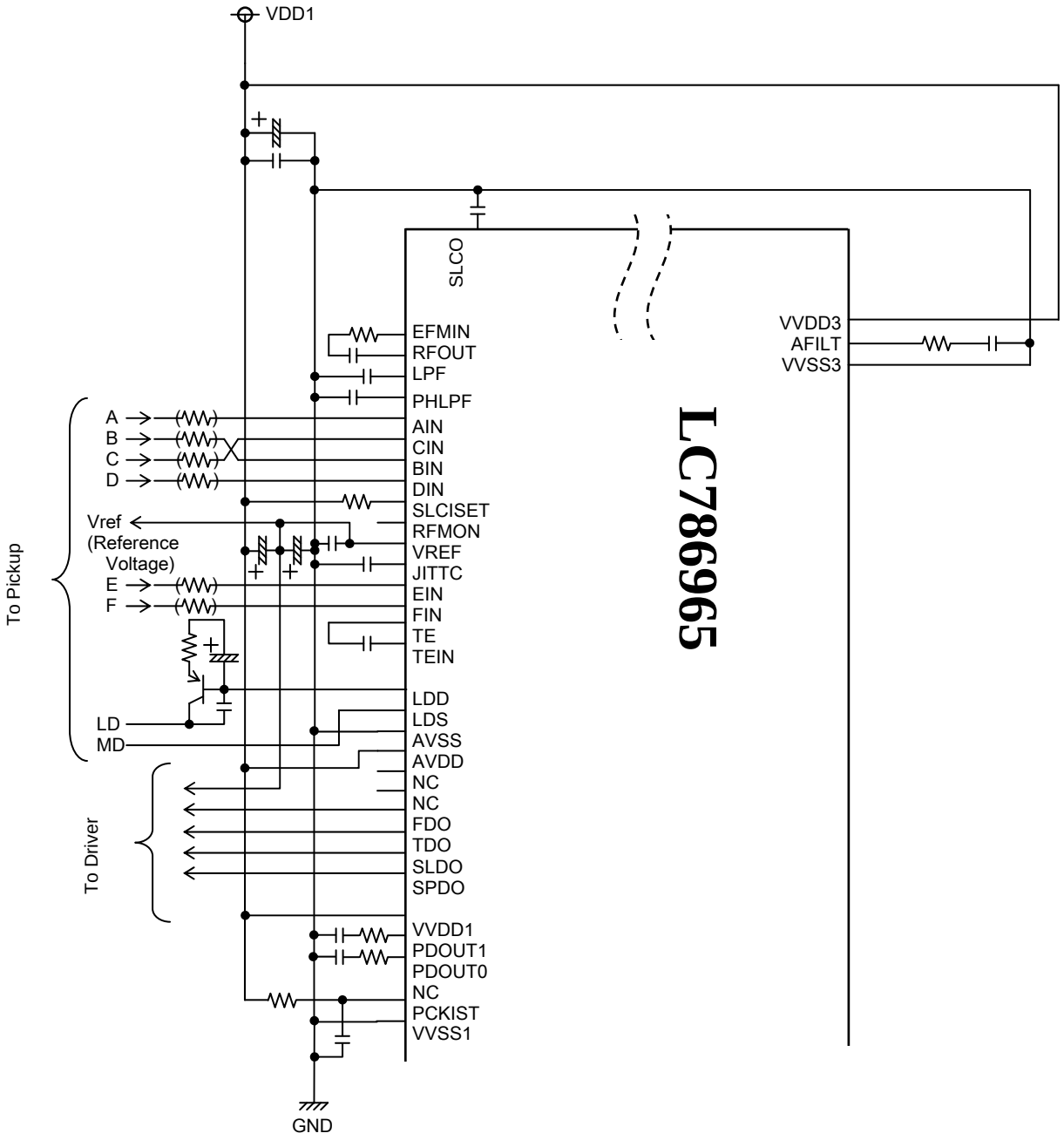
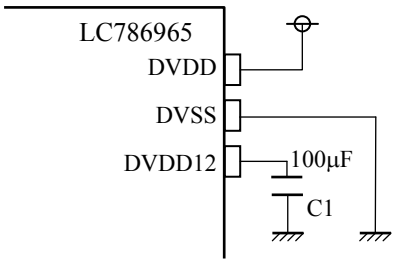


Figure 1. Application Schematic (CD Servo / PLL)

*This sample circuit is only for CD servo block, each PLL block.
The value of each component needs to be adjusted under the target conditions.
The circuit for CD servo shown above could be changed depending on the CD mechanism used.



*Same circuit need to be mounted both two DVDD12 pins (No.58 and No.124)
*The capacitor C1 must be greater than 50μF and low secure 50μF or more for low ESR and capacity value in the range of operating temperature so that there is a possibility of the oscillation when the capacity value changes by the temperature change etc. (The recommended value is 100μF)

Figure 2. Application Schematic (Regulator)

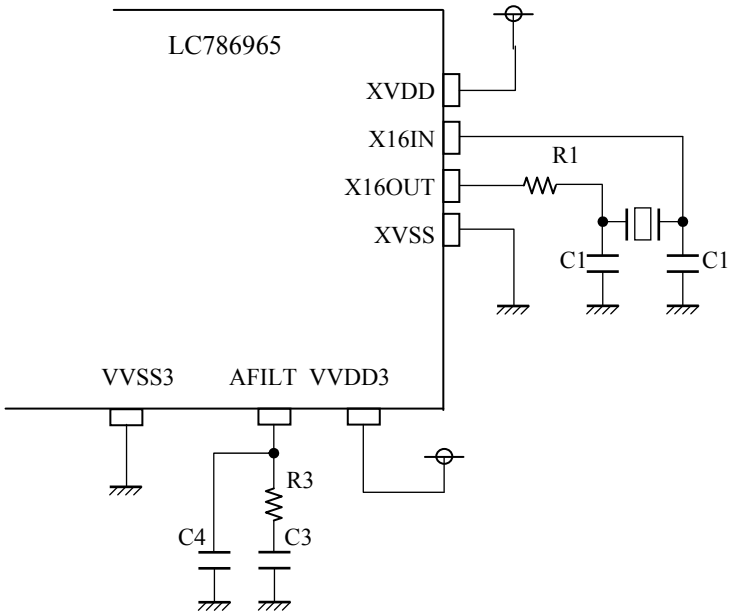


Figure 3. Application Schematic (oscillator / PLL)

<X16IN/X16OUT> : 16.9344MHz

Nihon Dempa Kogyo Co.,Ltd.

Type	Recommended value
AT51-CD2	R1=0Ω, C1=8pF

Murata Manufacturing Co.,Ltd.

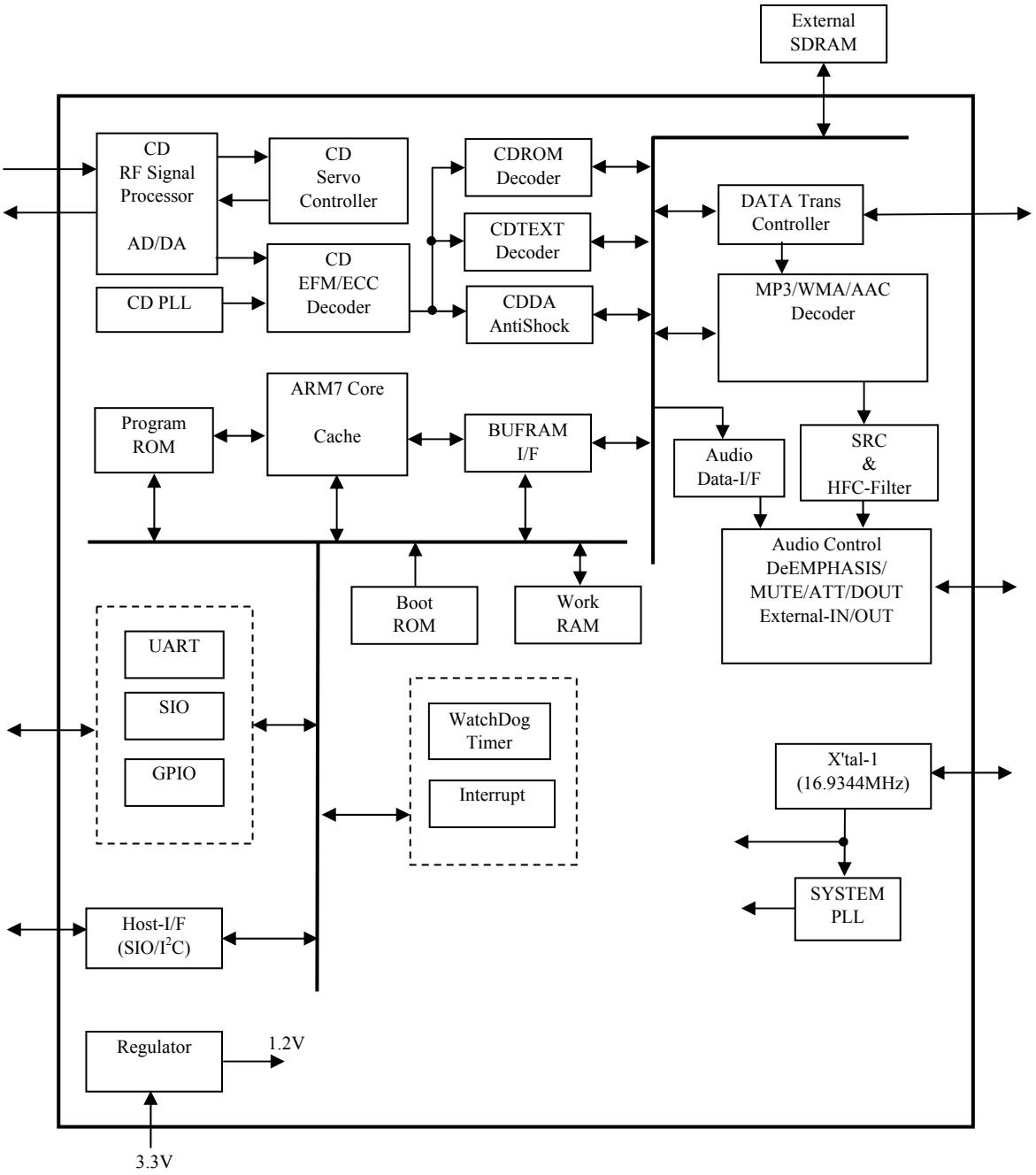
Type	Recommended value
CSTCE16M9V53-R0	R1=0Ω, C1=open
CSTCW16M9X51008-R0	R1=0Ω, C1=open
CSTLS16M9X53-B0	R1=0Ω, C1=open

<About PLL> : PLL filter circuit has to connect resistor (R3) and capacitance (C3,C4) to AFILT pin.
Recommended value is the following.
R3=3.3(kΩ), C3=0.1(μF), C4=1000(pF)

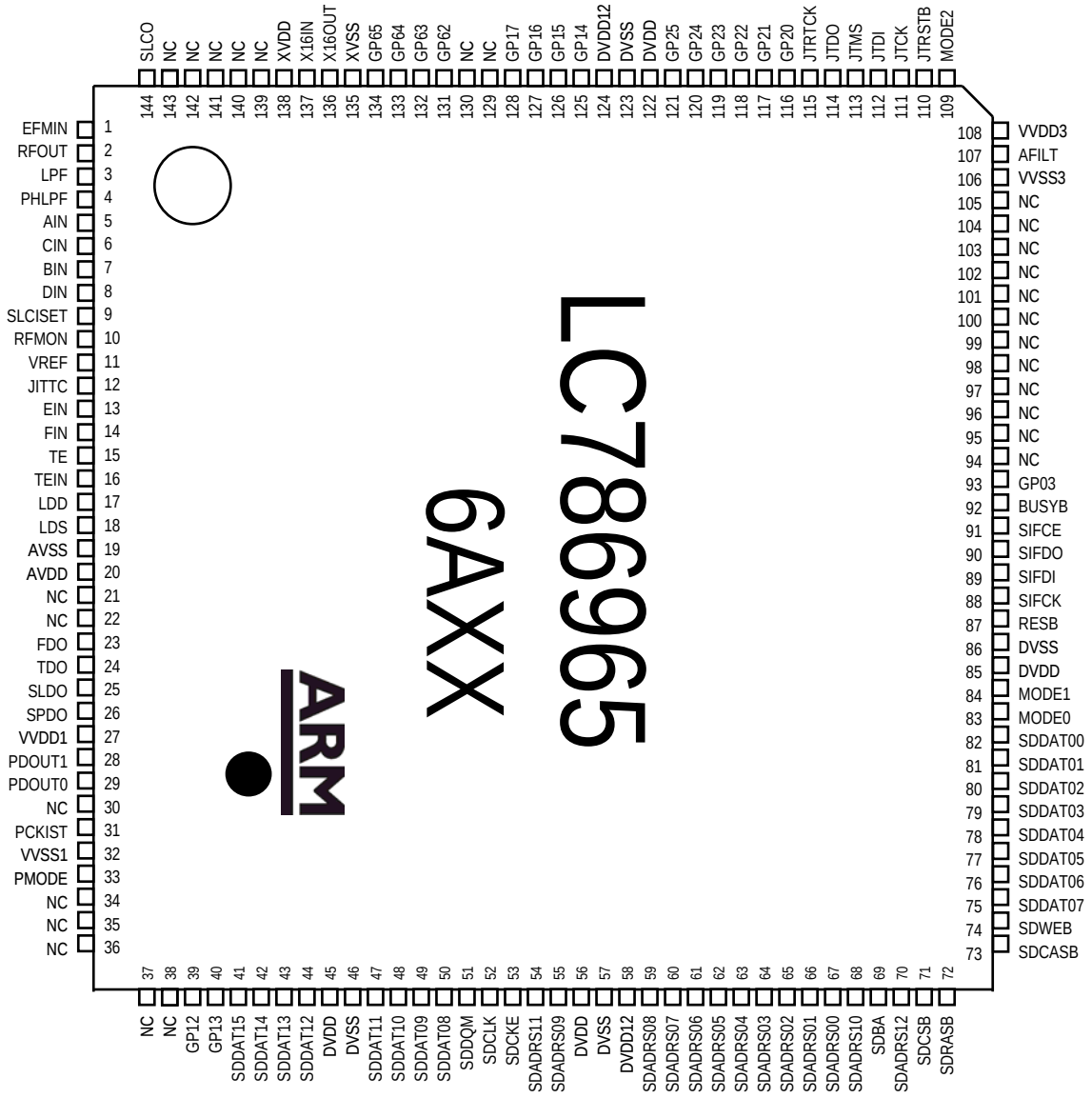
<Notes>

- Because the characteristics of oscillator could be changed according to the circuit board, ask evaluation with the individual original circuit board to the oscillator maker.
- If oscillation clock is disturbed by noise or by the other factors, it may lead to operation failure. Hence, make sure to connect resistor and capacitor for oscillation circuit and PLL2filter circuit as close as connect pins, and the wire should be as short as possible.
- See the section on "Analog Pin Internal Equivalent Circuits" for the internal configuration of XIN/XOUT, X16IN/X16OUT and AFILT.

Block Diagram



Pin Assignment



Pin Description

Pin No.	Pin name	I/O	State when "Reset"	Function
1	EFMIN	AI	Input	RF signal input
2	RFOUT	AO	Undefined	RF signal output
3	LPF	AO	Undefined	RF signal DC level detection low-pass filter capacitor connection
4	PHLPF	AO	Undefined	Defect detection low-pass filter capacitor connection
5	AIN	AI	Input	A signal input
6	CIN	AI	Input	C signal input
7	BIN	AI	Input	B signal input
8	DIN	AI	Input	D signal input
9	SLCISET	AI	Input	SLCO output current setting resistor connection
10	RFMON	AO	Undefined	IC internal analog signal monitor 1
11	VREF	AO	AVDD/2	VREF voltage output
12	JITTC	AO	Undefined	Jitter detection capacitor connection
13	EIN	AI	Input	E signal input
14	FIN	AI	Input	F signal input
15	TE	AO	Undefined	TE signal output
16	TEIN	AI	Input	TE signal input used for TES signal generation
17	LDD	AO	Undefined	Laser power control signal output
18	LDS	AI	Input	Laser power detection signal input
19	AVSS	-	-	Analog system ground. This pin must be connected to the 0V level.
20	AVDD	-	-	Analog system power supply
21	NC	-	-	NC pin. This pin must be left open.
22	NC	-	-	NC pin. This pin must be left open.
23	FDO	AO	AVDD/2	Focus control signal output
24	TDO	AO	AVDD/2	Tracking control signal output
25	SLDO	AO	AVDD/2	Sled control signal output
26	SPDO	AO	AVDD/2	Spindle control signal output
27	VVDD1	-	-	EFMPLL power supply
28	PDOUT1	AO	Undefined	EFMPLL charge pump output 1
29	PDOUT0	AO	Undefined	EFMPLL charge pump output 0
30	NC	-	-	NC pin. This pin must be left open.
31	PCKIST	AI	Input	EFMPLL charge pump current setting resistor connection pin
32	VVSS1	-	-	EFMPLL ground. This pin must be connected to the 0V level.
33	PMODE	I	Input	Must be connected to the DVDD.
34	NC	-	-	NC pin. This pin must be left open.
35	NC	-	-	NC pin. This pin must be left open.
36	NC	-	-	NC pin. This pin must be left open.
37	NC	-	-	NC pin. This pin must be left open.
38	NC	-	-	NC pin. This pin must be left open.
39	GP12	I/O	Input(L)	General purpose I/O port with pull down resistor Clock control input 1 Watch Dog Timer state monitor output
40	GP13	I/O	Input(L)	General purpose I/O port with pull down resistor Clock control input 2 Watch Dog Timer state monitor output SDRAM lower byte data mask control output SDRAM-DQML(LDQM) pin should be connected for 64Mbit-SDRAM
41	SDDAT15	I/O	Input(L)	SDRAM data input/output 15 (pull down resistor)

Pin No.	Pin name	I/O	State when "Reset"	Function
42	SDDAT14	I/O	Input(L)	SDRAM data input/output 14 (pull down resistor)
43	SDDAT13	I/O	Input(L)	SDRAM data input/output 13 (pull down resistor)
44	SDDAT12	I/O	Input(L)	SDRAM data input/output 12 (pull down resistor)
45	DVDD	-	-	Digital system power supply
46	DVSS	-	-	Digital system ground. This pin must be connected to the 0V level.
47	SDDAT11	I/O	Input(L)	SDRAM data input/output 11 (pull down resistor)
48	SDDAT10	I/O	Input(L)	SDRAM data input/output 10 (pull down resistor)
49	SDDAT09	I/O	Input(L)	SDRAM data input/output 9 (pull down resistor)
50	SDDAT08	I/O	Input(L)	SDRAM data input/output 8 (pull down resistor)
51	SDDQM	O	Low	SDRAM data mask control output Connect to SDRAM-DQMH(UDQM) pin
52	SDCLK	O	Low	SDRAM clock output
53	SDCKE	O	Low	SDRAM clock enable output
54	SDADRS11	O	Low	SDRAM address output 11 No use(NC) for 16Mbit-SDRAM SDRAM-ADRS11 pin connection for 64Mbit-SDRAM
55	SDADRS09	O	Low	SDRAM address output 9
56	DVDD	-	-	Digital system power supply
57	DVSS	-	-	Digital system ground. This pin must be connected to the 0V level.
58	DVDD12	AO	High	Capacitor connection pin for internal regulator
59	SDADRS08	O	Low	SDRAM address output 8
60	SDADRS07	O	Low	SDRAM address output 7
61	SDADRS06	O	Low	SDRAM address output 6
62	SDADRS05	O	Low	SDRAM address output 5
63	SDADRS04	O	Low	SDRAM address output 4
64	SDADRS03	O	Low	SDRAM address output 3
65	SDADRS02	O	Low	SDRAM address output 2
66	SDADRS01	O	Low	SDRAM address output 1
67	SDADRS00	O	Low	SDRAM address output 0
68	SDADRS10	O	Low	SDRAM address output 10
69	SDBA	O	Low	SDRAM bank select address output SDRAM-BANK pin connection for 16Mbit-SDRAM SDRAM-BANK1 pin connection for 64Mbit-SDRAM
70	SDADRS12	O	Low	SDRAM address output 12 16Mbit-SDRAM: connect to SDRAM-DQML(LDQM) pin 64Mbit-SDRAM: connect to SDRAM-BANK0 pin
71	SDCSB	O	Low	SDRAM Chip Select output
72	SDRASB	O	Low	SDRAM Row Address Strobe output
73	SDCASB	O	Low	SDRAM Column Address Strobe output
74	SDWEB	O	Low	SDRAM Write Enable output
75	SDDAT07	I/O	Input(L)	SDRAM data input/output 7 (pull down resistor)
76	SDDAT06	I/O	Input(L)	SDRAM data input/output 6 (pull down resistor)
77	SDDAT05	I/O	Input(L)	SDRAM data input/output 5 (pull down resistor)

Pin No.	Pin name	I/O	State when "Reset"	Function
78	SDDAT04	I/O	Input(L)	SDRAM data input/output 4 (pull down resistor)
79	SDDAT03	I/O	Input(L)	SDRAM data input/output 3 (pull down resistor)
80	SDDAT02	I/O	Input(L)	SDRAM data input/output 2 (pull down resistor)
81	SDDAT01	I/O	Input(L)	SDRAM data input/output 1 (pull down resistor)
82	SDDAT00	I/O	Input(L)	SDRAM data input/output 0 (pull down resistor)
83	MODE0	I	Input	LSI mode set pin 0 This pin must be connected to the 0V level.
84	MODE1	I	Input	LSI mode set pin 1 This pin must be connected to the 0V level.
85	DVDD	-	-	Digital system power supply
86	DVSS	-	-	Digital system ground. This pin must be connected to the 0V level.
87	RESB	I	-	IC reset input ("L"-active) This pin must be set low once after power is first applied.
88	SIFCK	I	Input	Host-I/F Data transmit clock input for serial communication 1 Data transmit clock input for I^2C communication
89	SIFDI	I/O	Input	Host-I/F Data input for serial communication 1 Data input/output for I^2C communication
90	SIFDO	I/O	Input	Host-I/F Data output for serial communication 1 (CMOS or 3-State output) General purpose I/O port with pull down resistor (GP00)
91	SIFCE	I/O	Input	Host -I/F Enable signal input for serial communication 1 ("H"-active) General purpose I/O port with pull down resistor (GP01)
92	BUSYB	I/O	Input(L)	Host -I/F System busy signal output ("L"-active) General purpose I/O port with pull down resistor (GP02) External interruption function 0
93	GP03	I/O	Input(L)	General purpose I/O port with pull down resistor Watch Dog Timer state monitor output External interruption function 1
94	NC	-	-	NC pin. This pin must be left open.
95	NC	-	-	NC pin. This pin must be left open.
96	NC	-	-	NC pin. This pin must be left open.
97	NC	-	-	NC pin. This pin must be left open.
98	NC	-	-	NC pin. This pin must be left open.
99	NC	-	-	NC pin. This pin must be left open.
100	NC	-	-	NC pin. This pin must be left open.
101	NC	-	-	NC pin. This pin must be left open.
102	NC	-	-	NC pin. This pin must be left open.
103	NC	-	-	NC pin. This pin must be left open.
104	NC	-	-	NC pin. This pin must be left open.
105	NC	-	-	NC pin. This pin must be left open.
106	VVSS3	-	-	SYSTEM PLL ground. This pin must be connected to the 0V level.
107	AFILT	AO	Undefined	SYSTEM PLL charge pump output
108	VVDD3	-	-	SYSTEM PLL power supply
109	MODE2	I	Input	LSI mode set pin 2. This pin must be connected to the 0V level.
110	JTRSTB	I	Input	JTAG reset input (Connect to pull-down resister or 0V level in normal mode.)
111	JTCK	I	Input	JTAG clock input (Connect to pull-down resister or 0V level in normal mode.)

Pin No.	Pin name	I/O	State when "Reset"	Function
112	JTDI	I	Input	JTAG data input (Connect to pull-down resister or 0V level in normal mode.)
113	JTMS	I	Input	JTAG mode input (Connect to pull-up resister or DVDD level in normal mode.)
114	JTDO	O	Low	JTAG data output (Leave open in normal mode.)
115	JTRTCK	O	Low	JTAG return clock output (Leave open in normal mode.)
116	GP20	I/O	Input (L)	General purpose I/O port with pull down resistor Request flag input/output 1 for Stream data Clock(Fs384)output for Audio DAC
117	GP21	I/O	Input (L)	General purpose I/O port with pull down resistor Transmit data output for serial communication 3 LR clock input/output 1 for Stream data LR clock input/output 1 for Audio interface
118	GP22	I/O	Input (L)	General purpose I/O port with pull down resistor Master clock output for serial communication 3 Bit clock input/output 1 for Stream data Bit clock input/output 1 for Audio interface
119	GP23	I/O	Input (L)	General purpose I/O port with pull down resistor Receive data input for serial data communication 3 Data input/output 1 for Stream data Data output 1 for Audio interface
120	GP24	I/O	Input (L)	General purpose I/O port with pull down resistor Emphasis flag input/output for Audio
121	GP25	I/O	Input (L)	General purpose I/O port with pull down resistor Digital audio output<SPDIF>
122	DVDD	-	-	Digital system power supply
123	DVSS	-	-	Digital system ground. This pin must be connected to the 0V level.
124	DVDD12	AO	High	Capacitor connection pin for internal regulator
125	GP14	I/O	Input (L)	General purpose I/O port with pull down resistor LR clock input/output 2 for Stream data LR clock input/output 2 for Audio interface
126	GP15	I/O	Input (L)	General purpose I/O port with pull down resistor Bit clock input/output 2 for Stream data Bit clock input/output 2 for Audio interface
127	GP16	I/O	Input (L)	General purpose I/O port with pull down resistor Data input/output 2 for Stream data Data input/output 2 for Audio interface
128	GP17	I/O	Input (L)	General purpose I/O port with pull down resistor Request flag input/output 2 for Stream data Clock(Fs384) input/output 2 for Audio DAC
129	NC	-	-	NC pin. This pin must be left open.
130	NC	-	-	NC pin. This pin must be left open.
131	GP62	I/O	Input (L)	General purpose I/O port with pull down resistor
132	GP63	I/O	Input (L)	General purpose I/O port with pull down resistor
133	GP64	I/O	Input (L)	General purpose I/O port with pull down resistor UART2 data transmit (exclusive with GP26)
134	GP65	I/O	Input (L)	General purpose I/O port with pull down resistor UART2 data receive (exclusive with GP27)

Pin No.	Pin name	I/O	State when "Reset"	Function
135	XVSS	-	-	Oscillator ground. This pin must be connected to the 0V level.
136	X16OUT	O	Oscillation	16.9344MHz oscillator connection
137	X16IN	I	Oscillation	16.9344MHz oscillator connection
138	XVDD	-	-	Oscillator power supply
139	NC	-	-	NC pin. This pin must be left open.
140	NC	-	-	NC pin. This pin must be left open.
141	NC	-	-	NC pin. This pin must be left open.
142	NC	-	-	NC pin. This pin must be left open.
143	NC	-	-	NC pin. This pin must be left open.
144	SLCO	AO	Undefined	Slice Level Control output

<Note>

(1) For unused pins:

- The unused input pins must be connected to the GND(0V) level if there is no individual note in the above table.
- The unused output pins must be left open(No connection) if there is no individual note in the above table.
- The unused input/output pins must be connected to the GND(0V) or power supply pin for I/O block with internal pull down resistor OFF or be left open with internal pull down resistor ON when input pin mode or must be left open(No connection) when output pin mode if there is no individual note in the above table.
  When you connect an I/O pin which is an input pin without internal pull-down resistor at reset mode to the GND or power supply level, we recommend you to use pull-down resistor or pull-up resistor individually as fail-safe.

(2) For power supply pins:

- Same voltage level must be supplied to DVDD, AVDD, XVDD, VVDD1 and VVDD3 power supply pins.
  (Refer to “Allowable operating ranges”.)

(3) For “Reset” condition:

- This LSI is not reset only by making the RESB pin “Low”.
  Refer to “Power on and Reset control” for detail of “Reset” condition.

Electric Characteristics

1. Absolute Maximum at Ta = 25°C, DVSS = AVSS = XVSS = VVSS1 = VVSS2 = 0 V (Note 1)

Item	Symbol	Ratings	Unit
Maximum supply voltage	VDDmax	–0.3 to +3.95	V
Input voltage	VIN	–0.3 to DVDD+0.3	V
Output voltage	VOUT	–0.3 to DVDD+0.3	V
Allowable power dissipation Ta ≤ 85°C Mounted reference PCB(*)	Pdmax	540	mW
Operating temperature	Topr	–40 to +85	°C
Storage temperature	Tstg	–40 to +125	°C
Maximum junction temperature	Tj(max)	125	°C

(*)Reference PCB : 114.3 mm × 76.1 mm × 1.6 mm, glass epoxy resin

Note 1 : Stresses exceeding those listed in Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Allowable Operating Ranges at Ta = –40°C to 85°C, DVSS = AVSS = XVSS = VVSS1 = VVSS3 = 0 V (Note 2)

Parameter	Symbol	Pin Names	Type	Conditions	MIN	TYP	MAX	Unit
Supply voltage	VDD1	DVDD, AVDD, XVDD VVDD1, VVDD3			3.00		3.60	V
High-level input voltage	VIH	RESB, SIFCK, SIFDI, SIFCE, BUSYB, GP03, GP12, GP13, GP14, GP15, GP16, GP17, GP20, GP21, GP22, GP23, GP62, GP63, GP64, GP65, SDDAT00 to SDDAT15, JTMS, JTRSTB, JTCK, JTDI, PMODE	Schmitt		2.00		VDD1	
Low-level input voltage	VIL	RESB, SIFCK, SIFDI, SIFCE, BUSYB, GP03, GP12, GP13, GP14, GP15, GP16, GP17, GP20, GP21, GP22, GP23, GP62, GP63, GP64, GP65, SDDAT00 to SDDAT15, JTMS, JTRSTB, JTCK, JTDI, MODE0, MODE1, MODE2	Schmitt		0.00		0.80	
Crystal Oscillator Frequency	FX	X16IN X16OUT	Oscillator circuit			16.9344		MHz

Note 2 : Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Electrical Characteristics at Ta = –40°C to 85°C, DVSS = AVSS = XVSS = VVSS1 = VVSS3 = 0 V (Note3)

Parameter	Symbol	Pin Names	Type	Conditions	MIN	TYP	MAX	Unit
Current drain	IDD1	DVDD, AVDD, XVDD, VVDD1, VVDD3				110	140	mA
High-level input current	IIH	RESB, SIFCK, SIFDI,SIFCE, BUSYB, GP03, GP12, GP13, GP14,GP15, GP16, GP17, GP20, GP21, GP22, GP23, GP62, GP63, GP64, GP65, SDDAT00 to SDDAT15 JTMS, JTRSTB, JTCK, JTDI, PMODE	Schmitt	VIN = VDD1 Built-in Pull-down resistor OFF			10.00	µA
Low-level input current	IIL	RESB, SIFCK, SIFDI,SIFCE, BUSYB, GP03, GP12, GP13, GP14, GP15, GP16, GP17, GP20, GP21, GP22, GP23, GP62, GP63, GP64, GP65, SDDAT00 to SDDAT15 JTMS, JTRSTB, JTCK, JTDI, MODE0, MODE1, MODE2,	Schmitt	VIN = 0.0 V	–10.00			
High-level output voltage	VOH(1)	GP12, GP13, GP14, GP15, GP16, GP17, GP20, GP21, GP22, GP23, GP62, GP63, GP64, GP65, SDBA, SDDAT00 to SDDAT15, SDADRS00 to SDADRS12, SDCSB, SDRASB, SDCASB, SDWEB, SDCKE, SDDQM	CMOS	IOH = –2 mA	VDD1 –0.6			V
	VOH(2)	SIFDI, SIFDO, SIFCE, BUSYB, GP03, SDCLK, JTDO, JTRTCK	CMOS	IOH = –4 mA				
Low-level output voltage	VOL(1)	GP12, GP13, GP14, GP15, GP16, GP17, GP20, GP21, GP22, GP23, GP62, GP63, GP64, GP65, SDBA, SDDAT00 to SDDAT15, SDADRS00 to SDADRS12, SDCSB, SDRASB, SDCASB, SDWEB, SDCKE, SDDQM	CMOS	IOL = 2 mA			0.40	
	VOL(2)	SIFDI, SIFDO, SIFCE, BUSYB, GP03, SDCLK, JTDO, JTRTCK	CMOS	IOL = 4 mA				
Output off-leakage current	IOFF(1)	PDOUT0,PDOUT1,AFILT		Hi-Z Out	–10.00		10.00	µA
	IOFF(2)	SIFDO		Hi-Z Out	–10.00		10.00	
Built-in Pull down resistor	RPD	SIFDO, SIFCE, BUSYB, GP03, GP12, GP13, GP14, GP15, GP16, GP17, GP20, GP21, GP22, GP23, GP62, GP63, GP64, GP65, SDDAT00 to SDDAT15			50	100	200	kΩ
Charge pump output current	IPDOH	PDOUT1,PDOUT0		PCKIST = 100 kΩ Current value setting : 1x	42.50	50.00	57.50	µA
	IPDOL	PDOUT1,PDOUT0			–57.50	–50.00	–42.50	
	IAFILH	AFILT				15.0		µA
	IAFILL	AFILT				15.0		

<Note>

- Put an internal pull down resistor or external pull down resistor or external pull up resistor to the SIFDO pin if its output condition is set to 3-State mode.

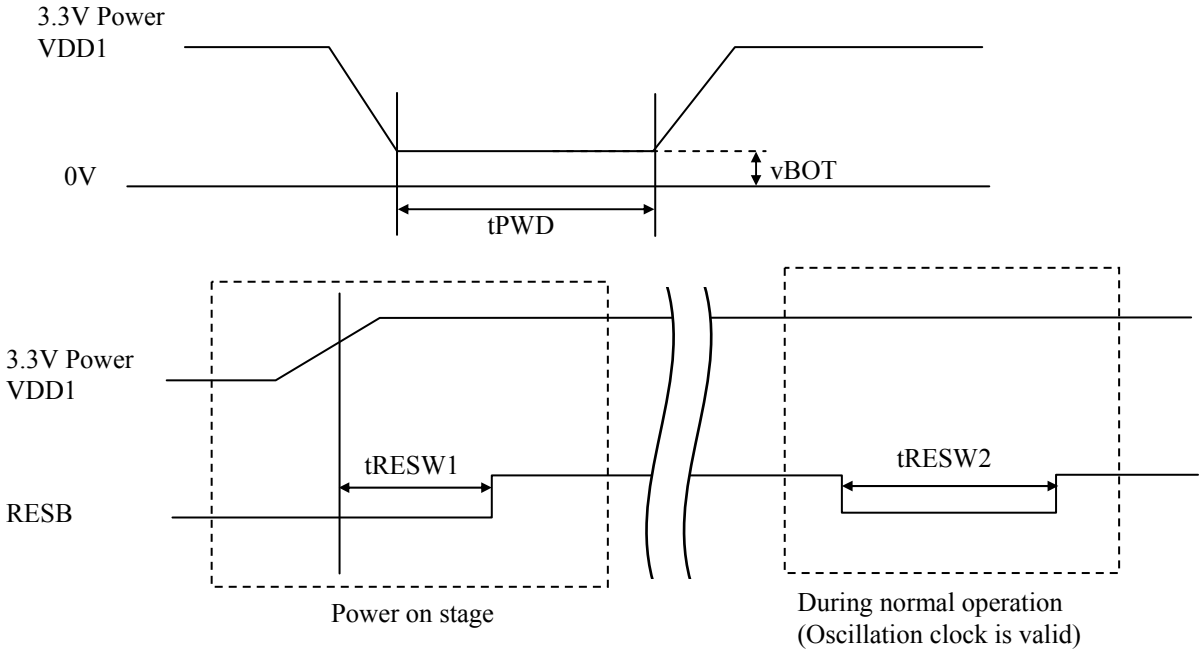
Note 3 : Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Power on and Reset control

- **Attention when power on**

The RESB pin must be set to “Low” level to initialize the operating state of this LSI when power is first supplied. If the power is on during the RESB pin is “High” level, this LSI may operate incorrectly because this LSI is not initialized.
You may input the voltage VDD1 or less to each input pin when the power supply is off.

<Figure 4-1> Power ON / Power Down / Reset timing



Parameter	Symbol	Min	Typ	Max	Unit
Power Down Time	tPWD	10			ms
Power Down Voltage	vBOT	0		0.2	V
Reset time(Power on)	tRESW1	20			ms
Reset time(Normal) (*1)	tRESW2	1			ms

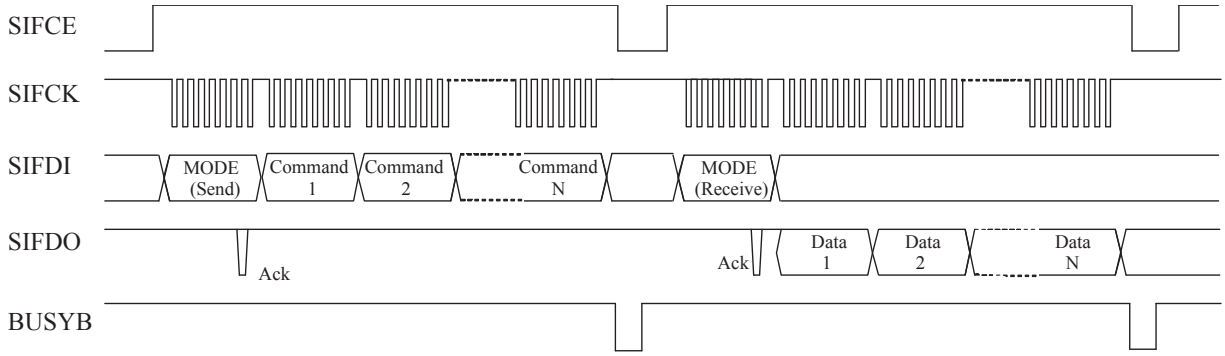
*1 : The specification of tRESW2 above is the time defined while steady the X16 clock and having oscillated. When the X16 clock has been stopped by the command etc. , the specification of tRESW2 could be larger than the value shown above, because it takes time that the X16 oscillator becomes stable.

5. Host interface

The data transmission between this LSI and Host controller is performed with SPI type synchronous SIO protocol.
The transmission procedure is as follows.

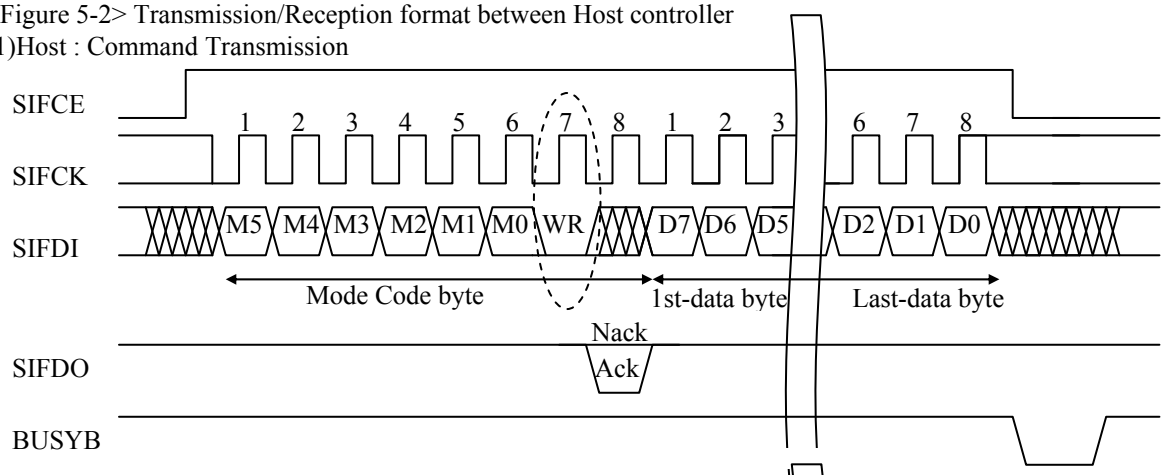
- Refer to the internal software specification of this LSI about M5 to M0 code in Mode code transmission.
  When the input data of M5 to M0 coincide to the data in the internal register, the SIFDO pin becomes to "Low" level(Ack) then the transmission is enabled.
  When not coincide, the SIFDO pin keeps "High" level(Nack) then the transmission is not enabled.
- The seventh data in Mode code transmission shows whether the following procedure is the Command transmission or the Data reception. When the seventh data is "Low", the following procedure is Command transmission. When the seventh data is "High", the following procedure is Data reception.
- Attention because the specifications of transmission timings are different depending on the internal CPU's operating speed modes(Low speed or Normal speed). Refer to the table in next page.

<Figure 5-1> Communication Interface format between Host controller

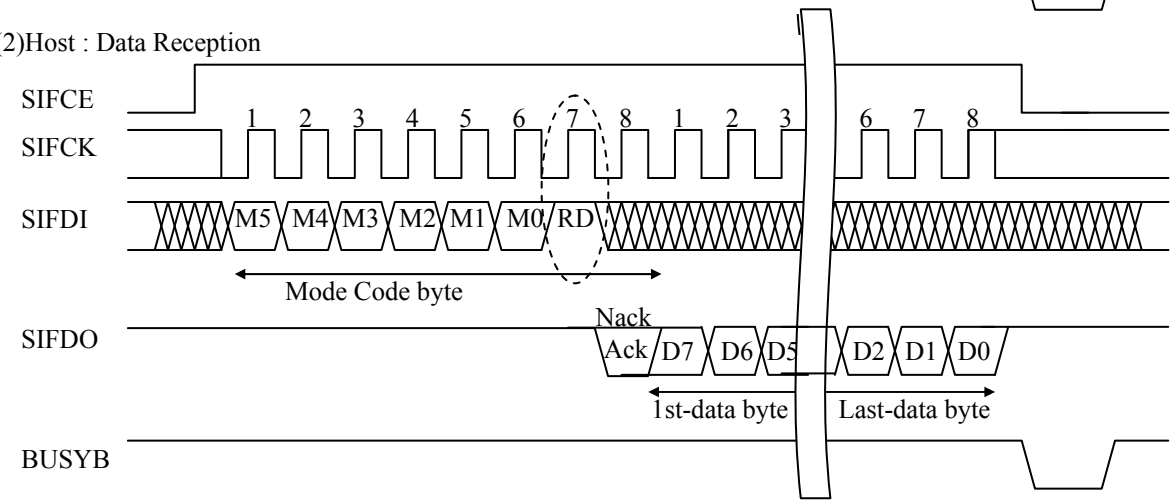


<Figure 5-2> Transmission/Reception format between Host controller

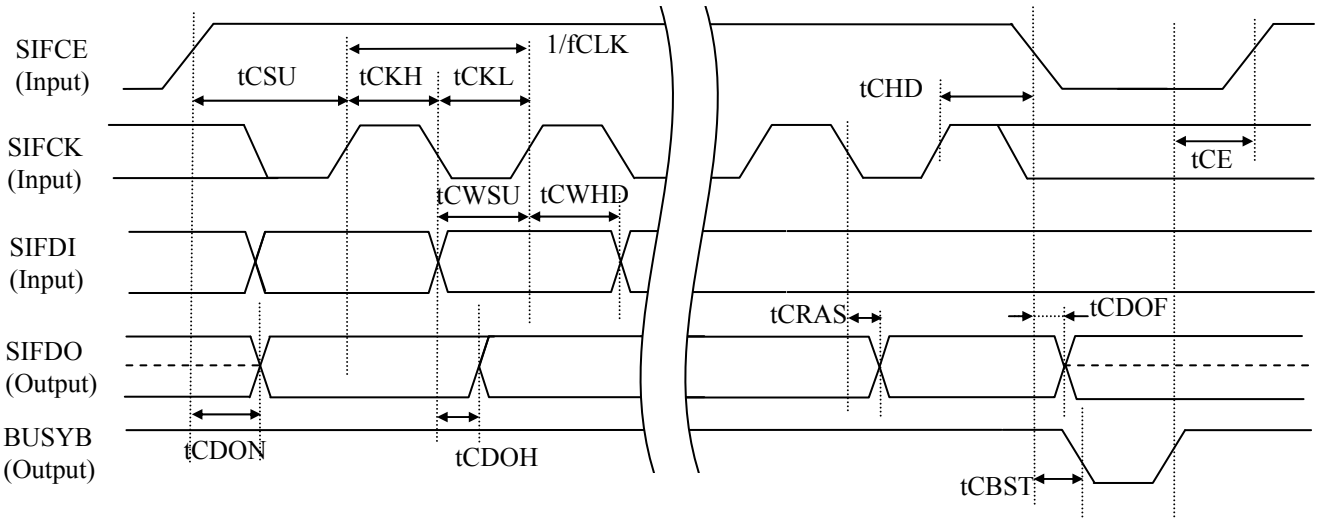
(1)Host : Command Transmission



(2)Host : Data Reception



<Figure5-3> Communication Timing specification between Host controller



Parameter	Symbol	Pin Names	Conditions	Min	Typ	Max	Unit
SIFCK clock Frequency	fCLK	SIFCK	Figure 5-3			3.3 0.725	MHz
SIFCK clock "H" level width	tCKH	SIFCK	Figure 5-3	150 690			ns
SIFCK clock "L" level width	tCKL	SIFCK	Figure 5-3	150 690			
Transfer Start Enable time	tCE	BUSYB,SIFCE	Figure 5-3	0 0			
Setup time for Transfer Start	tCSU	SIFCE,SIFCK	Figure 5-3	100 200			
Hold time for Transfer End	tCHD	SIFCE,SIFCK	Figure 5-3	100 200			
Setup time for SIFDI	tCWSU	SIFDI,SIFCK	Figure 5-3	75 75			
Hold time for SIFDI	tCWHD	SIFDI,SIFCK	Figure 5-3	75 200			
Output Delay time for SIFDO “H”	tCDOH	SIFDO,SIFCK	Figure 5-3			100 350	
Output Delay time for SIFDO	tCRAS	SIFDO,SIFCK	Figure 5-3			100 350	
Turn On time for SIFDO *1	tCDON	SIFDO,SIFCE	Figure 5-3			100 100	
Turn Off time for SIFDO *1	tCDOF	SIFDO,SIFCE	Figure 5-3			150 150	
BUSYB "L" level output Delay time	tCBST	BUSYB	Figure 5-3			150 350	

Internal CPU operating speed mode Upper step : Normal speed
Lower step : Low speed

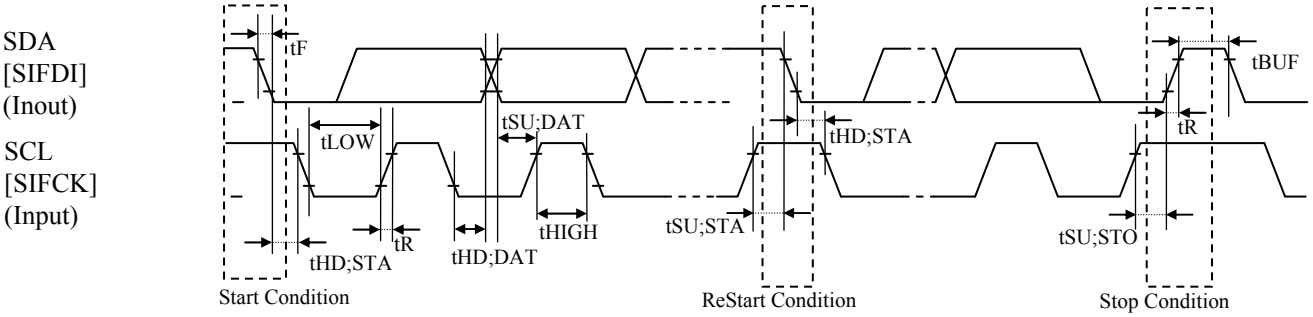
*1 : The tCDON and tCDOF specifications are for when the SIFDO pin is set to the 3-State mode.

The I^2C transmission is also available for the communication between this LSI and Host controller.
The available modes are follows.

Normal speed mode : 100k bps
High speed mode : 400k bps

The slave address is 0x16(7bit).

<Figure 5-4> Communication Timing specification between Host controller (I^2C)



Parameter	Symbol	Conditions	Normal(100kbps)		High(400kbps)		Unit
			Min	Max	Min	Max	
SCL clock Frequency	fSCL	Figure 5-4	0	100	0	400	kHz
Bus Free period	tBUF	Figure 5-4	4.7		1.3		µs
SCL clock "L" level width	tLOW	Figure 5-4	4.7		1.3		µs
SCL clock "H" level width	tHIGH	Figure 5-4	4.0		0.6		µs
Hold time for Start/ReStart condition	tHD;STA	Figure 5-4	4.0		0.6		µs
Setup time for Start/ReStart condition	tSU;STA	Figure 5-4	4.7		0.6		µs
Hold time for SDA	tHD;DAT	Figure 5-4	0		0		µs
Setup time for SDA	tSU;DAT	Figure 5-4	250		100		ns
Rising time for SDA, SCL	tR	Figure 5-4		1000	20+0.1Cb	300	ns
Falling time for SDA, SCL	tF	Figure 5-4		300	20+0.1Cb	300	ns
Setup time for Stop condition	tSU;STO	Figure 5-4	4.0		0.6		µs

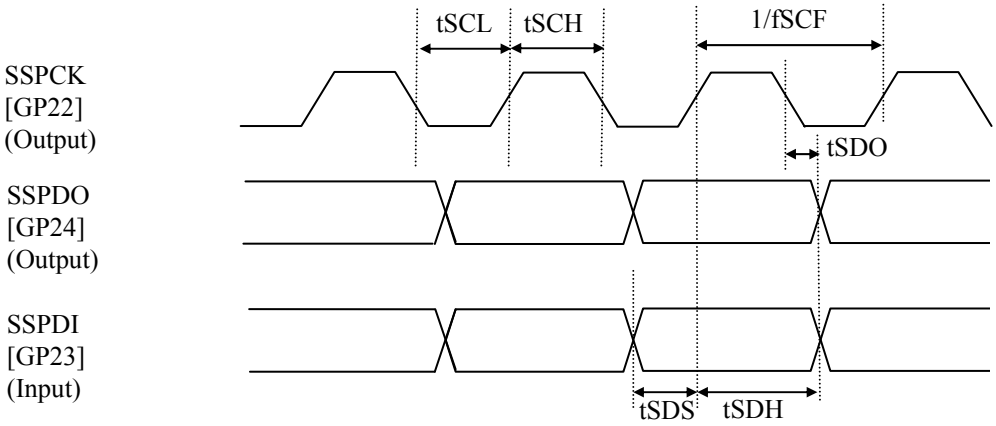
Note : Cb is the total capacitance of all loads connected to the Bus(Unit : pF).

In case of I^2C transmission mode, the SIFDO, SIFCE and BUSYB pins are used as the general purpose I/O ports individually.

SIFDO : GP00
SIFCE : GP01
BUSYB : GP02

6. Serial Communication Port

<Figure 6-1> Input/Output Timing specification for Serial communication (SIO) Master mode



Parameter	Symbol	Pin Names	Conditions	Min	Typ	Max	Unit
SIO clock(SSPCK) Frequency	fSCF	SSPCK	Figure 6-1	0.008		5.0	MHz
SIO clock(SSPCK) "H" level width	tSCH	SSPCK	Figure 6-1	100		62500	ns
SIO clock(SSPCK) "L" level width	tSCL	SSPCK	Figure 6-1	100		62500	
SIO data output(SSPDO) Delay time	tSDO	SSPDO,SSPCK	Figure 6-1			100	
Setup time for SIO data input(SSPDI)	tSDS	SSPDI,SSPCK	Figure 6-1	50			
Hold time for SIO data input(SSPDI)	tSDH	SSPDI,SSPCK	Figure 6-1	75			

Note : In condition under the internal CPU (ARM7) is operated at the normal mode.

7. Stream Data Input/Output function

There are two methods to input or output the stream data shown below.

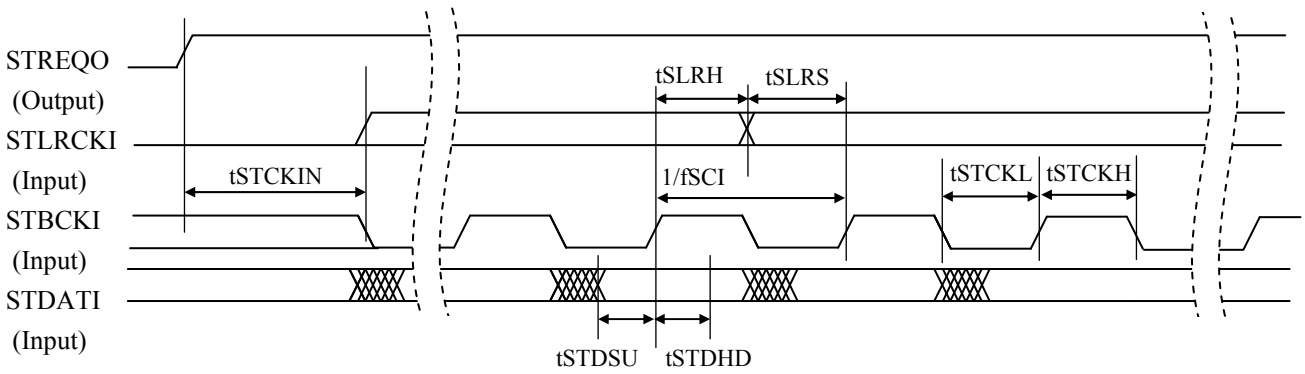
(1)4 lines method

Stream Input : Input signals to STLRCKI, STBCKI and STDATI when STREQO="H".
Stream Output : Output signals from STLRCKO, STBCKO and STDATO when STREQI="H".
In this method, the signal input or output timings for STLRCKI/STBCKI/STDATI(Input) pins and STLRCKO/STBCKO/STDATO(Output) pins are same as for traditional audio input or output timings. That is to say 4 bytes(32 bits) of data should be transferred in one period of STLRCKI(Input) or STLRCKO(Output).

(2)3 lines method

Stream Input : Input signals to STBCKI and STDATI when STREQO="H".
Stream Output-1 : Output signals from STBCKO and STDATO when STREQI="H".
Stream Output-2 : Input signal from STBCKI and output signal from STDATO when STREQI="H".
In this method, the Bit Clock and Data should be input or output according to the condition of STREQO or STREQI. The data transfer is performed at 2 bytes(16bits) unit.

<Figure 7-1> Stream Data Input timing specification



*Relationship between signal name and pin name

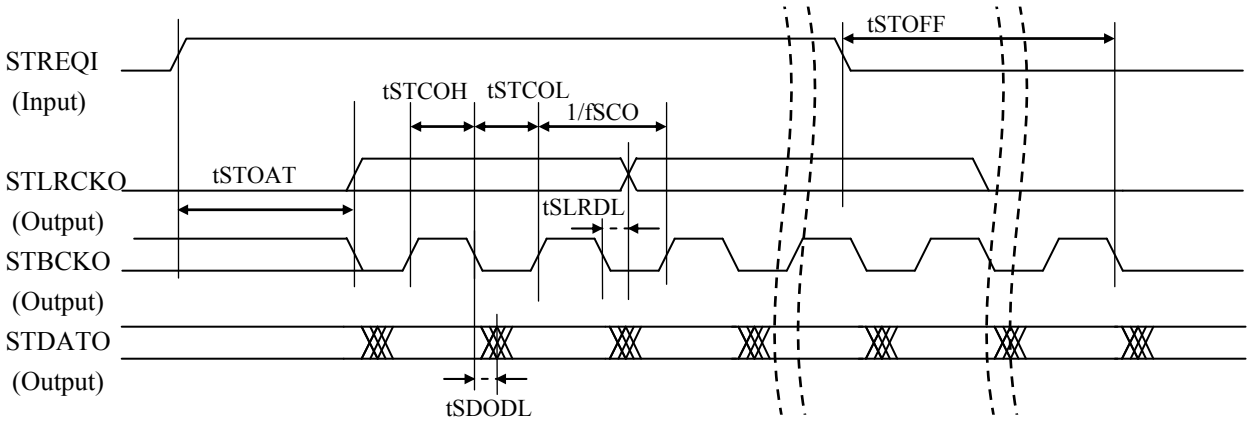
STREQO : GP17 or GP20 STLRCKI : GP14 or GP21
STBCKI : GP15 or GP22 STDATI : GP16 or GP23

Note : When the pins from GP14 to GP17 and pins from GP20 to GP23 are set to be the stream input pins simultaneously, the setting for pins from GP14 to GP17 is available. Recommend the setting of the stream input pins only to either of the pins of GP14 to GP17 or the pins of GP20 to GP23.

Parameter	Symbol	Pin Names	Conditions	Min	Typ	Max	unit
STBCKI clock Frequency	fSCI	STBCKI	Figure 7-1			4.24	MHz
Stream Input Start time	tSTCKIN	STREQO, STBCKI,STLRCKI	Figure 7-1	50			ns
STBCKI clock "H" level width	tSTCKH	STBCKI	Figure 7-1	100			ns
STBCKI clock "L" level width	tSTCKL	STBCKI	Figure 7-1	100			ns
Setup time for STLRCKI	tSLRS	STLRCKI,STBCKI	Figure 7-1	75			ns
Hold time for STLRCKI	tSLRH	STLRCKI,STBCKI	Figure 7-1	75			ns
Setup time for STDATI	tSTDSU	STDATI,STBCKI	Figure 7-1	75			ns
Hold time for STDATI	tSTDHD	STDATI,STBCKI	Figure 7-1	75			ns

Note : The Figure 9-1 shows the case that the data are latched at the rising edge of the STBCKI clock. In case of falling edge mode, the timings are same.

<Figure 7-2> Stream Data Output timing specification : STBCK output mode



*Relationship between signal name and pin name

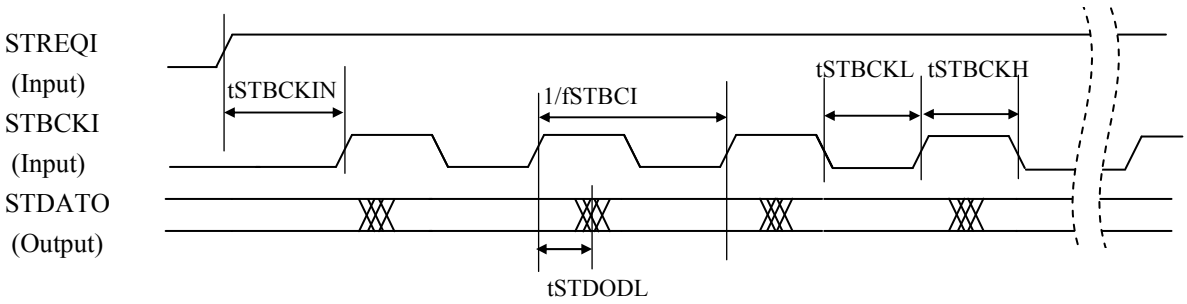
STREQI : GP17 or GP20 STLRCKO : GP14 or GP21

STBCKO : GP15 or GP22 STDATO : GP16 or GP23

Parameter	Symbol	Pin Names	Conditions	Min	Typ	Max	unit
STBCKO clock Frequency	fSCO	STBCKO	Figure 7-2			4.24	MHz
Stream Output Start time	tSTOAT	STREQI, STBCKO,STLRCKO	Figure 7-2			(1/fSCO) *48	ns
Stream Output Stop time	tSTOFF	STREQI,STBCKO	Figure 7-2			(1/fSCO) *48	ns
STBCKO clock "H" level width	tSTCOH	STBCKO	Figure 7-2	100			ns
STBCKO clock "L" level width	tSTCOL	STBCKO	Figure 7-2	100			ns
STLRCKO Output Delay time	tSLRDL	STLRCKO,STBCKO	Figure 7-2	0		50	ns
STDATO Output Delay time	tSDODL	STDATO,STBCKO	Figure 7-2	0		50	ns

Note : he Figure 7-2 shows the case that the data are output at the falling edge of the STBCKO clock. In case of rising edge mode, the timings are same.

<Figure 7-3> Stream Data Output timing specification : STBCK input mode



*Relationship between signal name and pin name
STREQI : GP17 or GP20
STBCKI : GP15 or GP22 STDATO : GP16 or GP23

Parameter	Symbol	Pin Names	Conditions	Min	Typ	Max	unit
STBCKI clock Frequency	fSTBCI	STBCKI	Figure 7-3			1.25	MHz
STBCKI Input Start time	tSTBCKIN	STREQI, STBCKI	Figure 7-3	1000			ns
STBCKI clock "H" level width	tSTBCKH	STBCKI	Figure 7-3	400			ns
STBCKI clock "L" level width	tSTBCKL	STBCKI	Figure 7-3	400			ns
STDATO Output Delay time	tSTDODL	STBCKI, STDATO	Figure 7-3			250	ns

<Note>
There are two polarity modes for the STBCKI signal. The STDATO output timing is different for the two modes as shown below.

①The case that the STBCKI starts from "L" level.
The STDATO signal will be output from the rising edge of the STBCKI signal.
②The case that the STBCKI starts from "H" level.
The STDATO signal will be output from the falling edge of the STBCKI signal.

The Figure 9-3 shows the timing chart of case ①.

8. Digital Audio Data Interface

- Digital Audio Interface Output Format

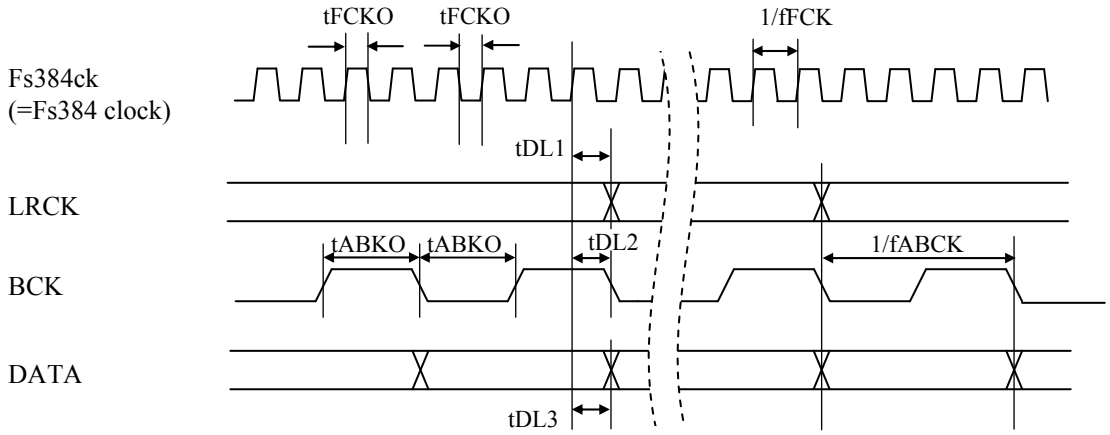
Mode	Data Length	Slot Length	System Clock
IIS MSB First Right Justified	16-bit 24-bit	32 fs, 48 fs, 64 fs	Fs384 Output clock

- Used pins

LRCK	BCK	DATA	Fs384 clock
GP14 GP21	GP15 GP22	GP16 GP23	GP17 GP20

- Others
  - The audio output is available for three kinds of Fs (32 kHz / 44.1 kHz / 48 kHz).
  - GP25 pin is available for Digital audio output (SPDIF).

<Figure 8-1> Digital Audio Data Output timing



Parameter	Symbol	Pin Names	Conditions	Min	Typ	Max	unit
Fs384 clock Frequency	fFCKO	Fs384ck	Figure 8-1		16.9344 *1		MHz
Fs384 clock "H" level width	tFCKOH	Fs384ck	Figure 8-1		29.5 *1		ns
Fs384 clock "L" level width	tFCKOL	Fs384ck	Figure 8-1		29.5 *1		ns
Bit clock Frequency	fABCKO	BCK	Figure 8-1		2.1168 *1		MHz
Bit clock "H" level width	tABKOH	BCK	Figure 8-1		236.2 *1		ns
Bit clock "L" level width	tABKOL	BCK	Figure 8-1		236.2 *1		ns
LRCK output Delay time	tDL1	LRCK,Fs384ck	Figure 8-1	0		50	ns
BCK output Delay time	tDL2	BCK,Fs384ck	Figure 8-1	0		50	ns
DATA output Delay time	tDL3	DATA,Fs384ck	Figure 8-1	0		50	ns

*1 : Case of setting the output Fs is 44.1KHz and the output slot length format is 48 fs.

9. Internal Voltage Regulator

at Ta = –40°C to 85°C, DVSS = AVSS = XVSS = VVSS1 = VVSS3 = 0 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Output Voltage	DVDD12	VDD1 = 3.0 V to 3.6 V	1.08	1.20	1.32	V
Load current	Iope	VDD1 = 3.3 V			200	mA

Note : The spec. of “load current” above is sum of the load current of two internal voltage regulator.

10. A/D, D/A converter Characteristics for servo

at Ta = –40°C to 85°C, VDD1 = 3.3 V, DVSS = AVSS = XVSS = VVSS1 = VVSS3 = 0 V

Parameter	Symbol	Min	Typ	Max	Unit
Resolution	Res		8		bit
Maximum input/output range	Vaio1		4/5*VDD1		V
Minimum input/output range	Vaio2		1/5*VDD1		V

11. SDRAM Interface

(1) Required specification for external SDRAM

Memory size	16M bit or 64M bit
Data width	16 bit
CAS latency	2
Burst length	Full

(2) Interface pins to external SDRAM

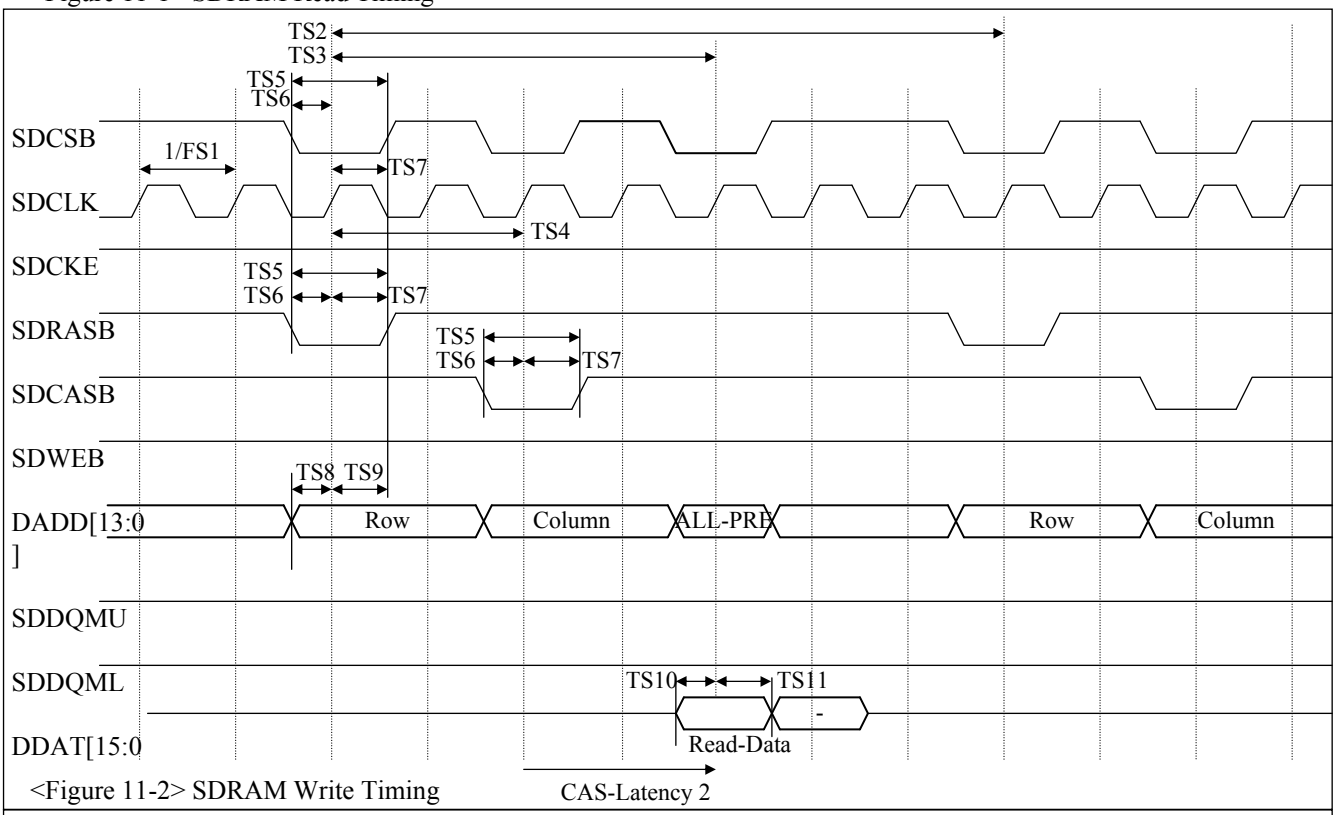
Pin Name	Function at 16Mbit-SDRAM	Function at 64Mbit-SDRAM	Signal name in Figure11-1,2,3
SDDAT15 to SDDAT00	Data Input/Output (16bit)	Data Input/Output (16bit)	DDAT[15:0] DDAT[15:0]
SDADRS10 to SDADRS00	Address Output (11bit)	Address Output (11bit)	DADD[10:0] DADD[10:0]
SDADRS11	Not used	Address(A11) Output	- DADD[11]
SDADRS12	DQML(LDQM) Output Lower byte data mask control	Address(A12) or Bank0 Output	SDDQML DADD[12]
SDBA	Bank Output	Bank or Bank1 Output	DADD[11] DADD[13]
SDDQM	DQMH(UDQM) Output Upper byte data mask control	DQMH(UDQM) Output Upper byte data mask control	SDDQMU SDDQMU
GP13	Not used	DQML(LDQM) Output Lower byte data mask control	- SDDQML
SDCSB	CSB Output	CSB Output	SDCSB SDCSB
SDRASB	RASB Output	RASB Output	SDRASB SDRASB
SDCASB	CASB Output	CASB Output	SDCASB SDCASB
SDWEB	WEB Output	WEB Output	SDWEB SDWEB
SDCKE	Clock Enable Output	Clock Enable Output	SDCKE SDCKE
SDCLK	Clock Output	Clock Output	SDCLK SDCLK

Notes

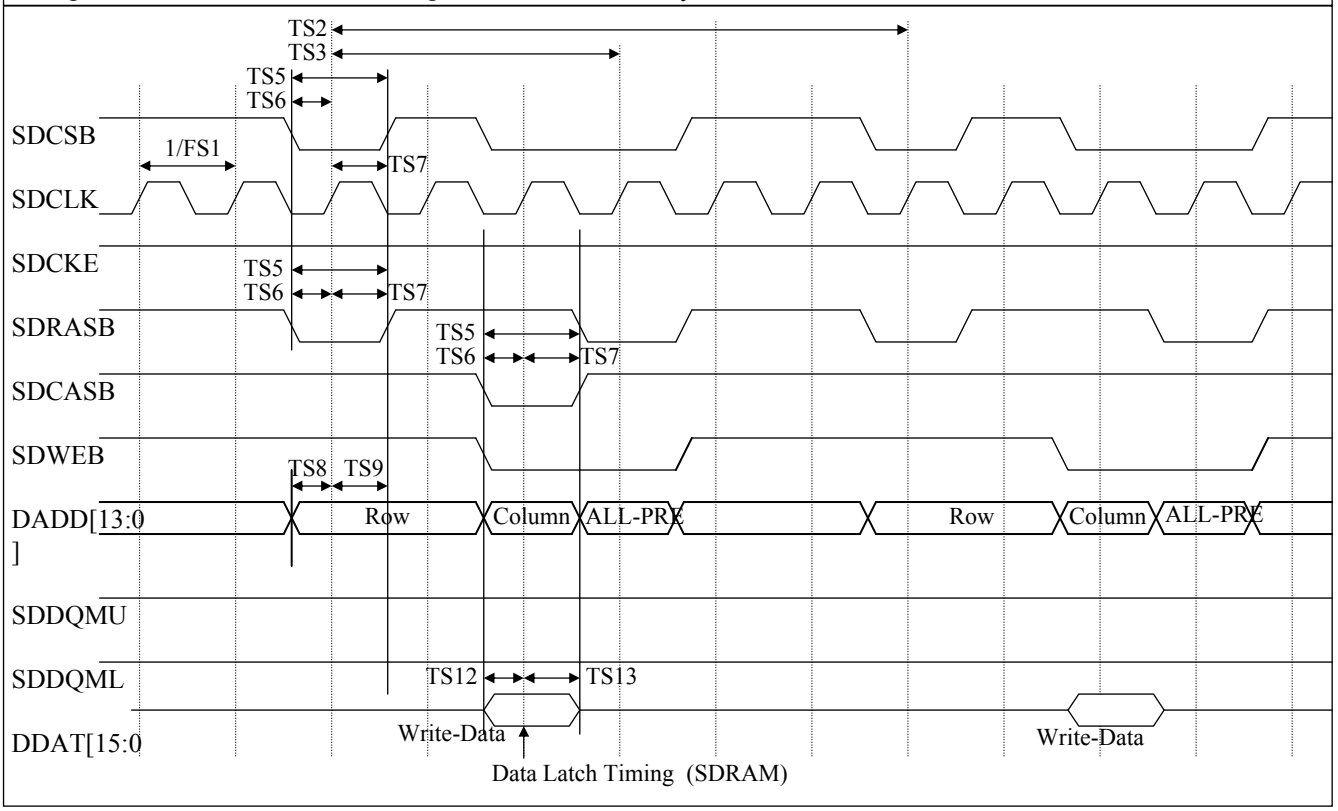
- SDADRS11 and GP13 in 16Mbit-SDRAM using mode should be treated as described below.
  SDADRS11 : Open (No connect)
  GP13 : Use as other function or Open
- SDDAT00 to SDDAT15 pins can have internal pull down resistor optionally. Those pull down resistors are set to ON mode in initialization.
  When setting the SDRAM using mode, those pull down resistors will be set to OFF mode.
- Some signals named in Figure 11-1 to Figure 11-3 use different pins according to the using SDRAM. The signal name in Figure 11-1 to Figure 11-3 for the actual pin is shown at the most right column in above table.
  Upper step : Signal name in 16Mbit-SDRAM using mode
  Lower step : Signal name in 64Mbit-SDRAM using mode

(3) SDRAM Access Timing

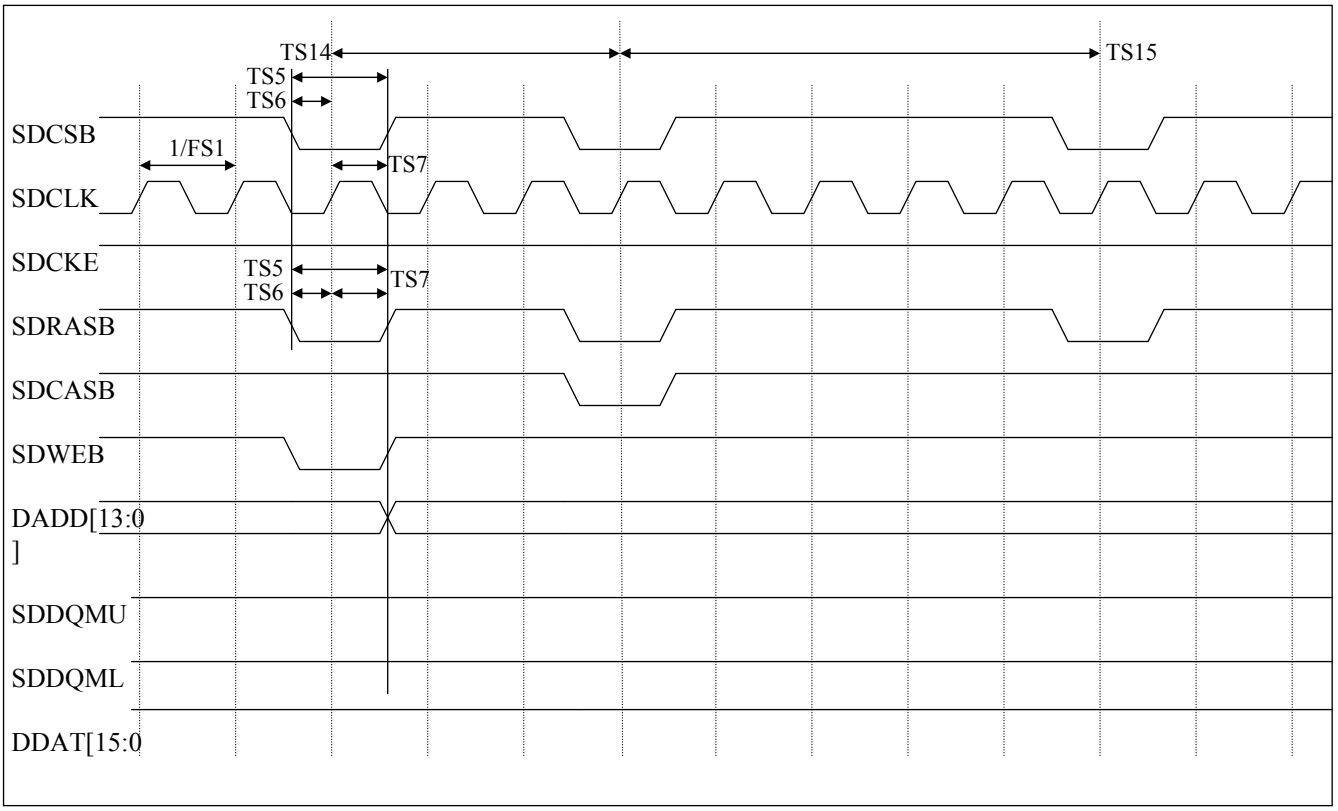
<Figure 11-1> SDRAM Read Timing



<Figure 11-2> SDRAM Write Timing



<Figure 11-3> SDRAM Refresh Timing (Auto Refresh)

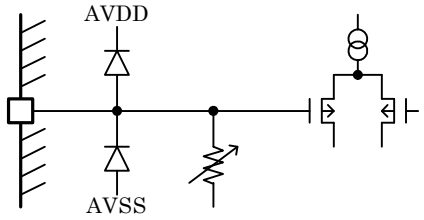
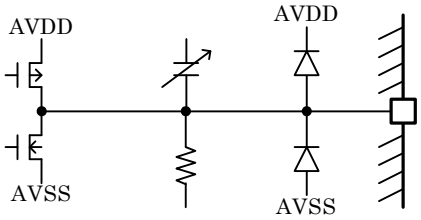
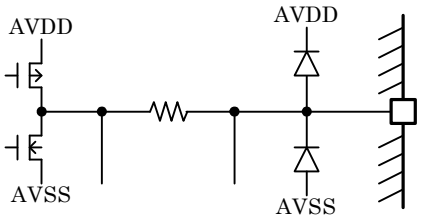
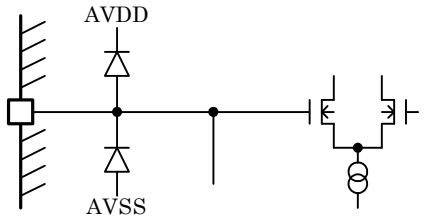
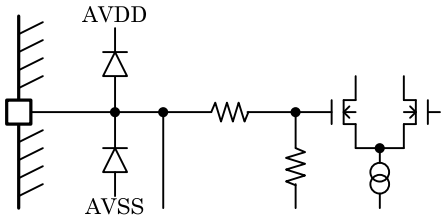
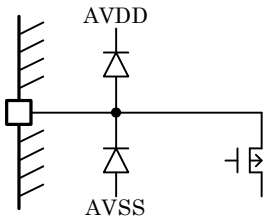
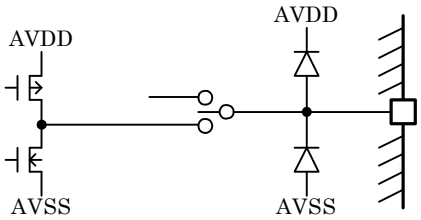


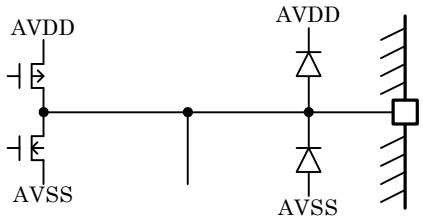
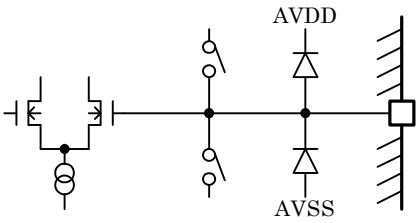
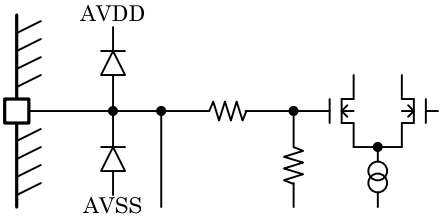
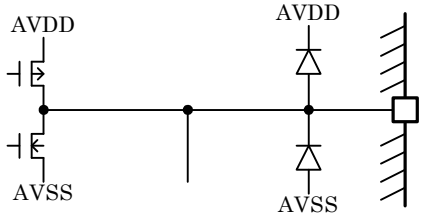
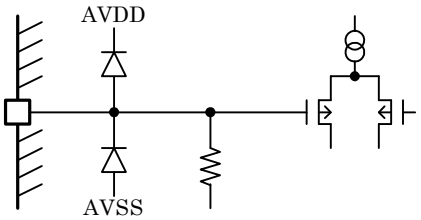
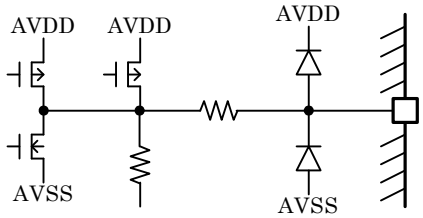
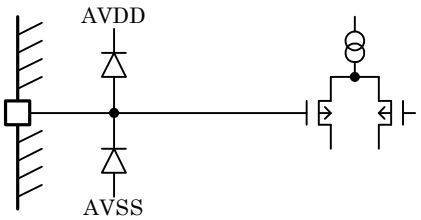
symbol	parameter	Min	typ	max	unit
FS1	SDRAM clock (SDCLK) Frequency		16.9344		MHz
TS2	Row (SDRASB) Cycle time	(1/FS1)*5	-	-	ns
TS3	Row (SDRASB) Active time	(1/FS1)*3	-	-	ns
TS4	RASB-CASB Delay time (SDRASB-SDCASB)	(1/FS1)*2	-	-	ns
TS5	Command "L" level width (SDCSB,SDCKE,SDRASB,SDCASB,SDWEB)	40	-	-	ns
TS6	Command Setup time (SDCSB,SDCKE,SDRASB,SDCASB,SDWEB,SDDQMU,SDDQML)	10	-	-	ns
TS7	Command Hold time (SDCSB,SDCKE,SDRASB,SDCASB,SDWEB,SDDQMU,SDDQML)	10	-	-	ns
TS8	Address(DADD) Setup time	10	-	-	ns
TS9	Address(DADD) Hold time	10	-	-	ns
TS10	SDRAM Read Data Setup time (Data read from SDRAM)	20	-	-	ns
TS11	SDRAM Read Data Hold time (Data read from SDRAM)	0	-	-	ns
TS12	SDRAM Write Data Hold time before rising edge of SDCLK (Data write to SDRAM)	10	-	-	ns
TS13	SDRAM Write Data Hold time after rising edge of SDCLK (Data write to SDRAM)	10	-	-	ns
TS14	Row (SDRASB) Pre-charge time	(1/FS1)*3	-	-	ns
TS15	Row (SDRASB) Active time after Refresh	(1/FS1)*5	-	-	ns

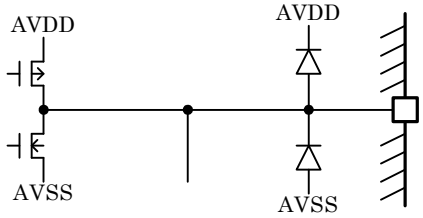
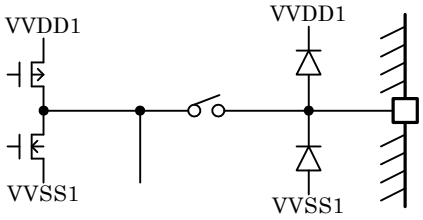
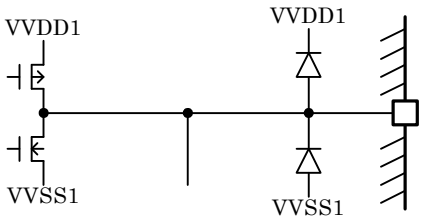
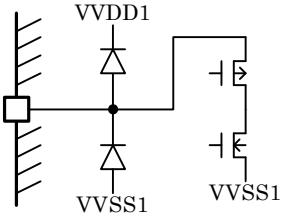
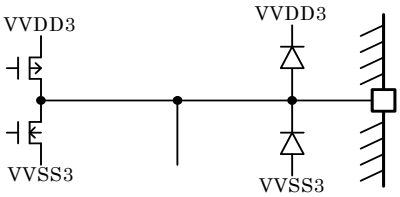
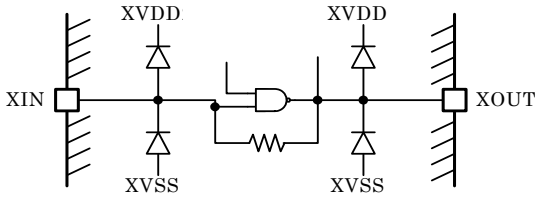
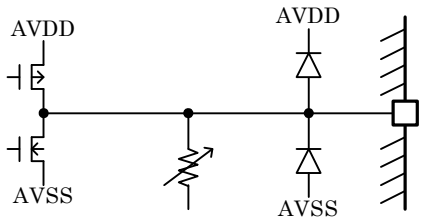
Notes

- Setup time and Hold time specifications in above table are measured from the rising edge of SDCLK signal.
- All the specifications in above table are applied to Read mode, Write mode and Refresh mode.

Analog Pin Internal Equivalent Circuits

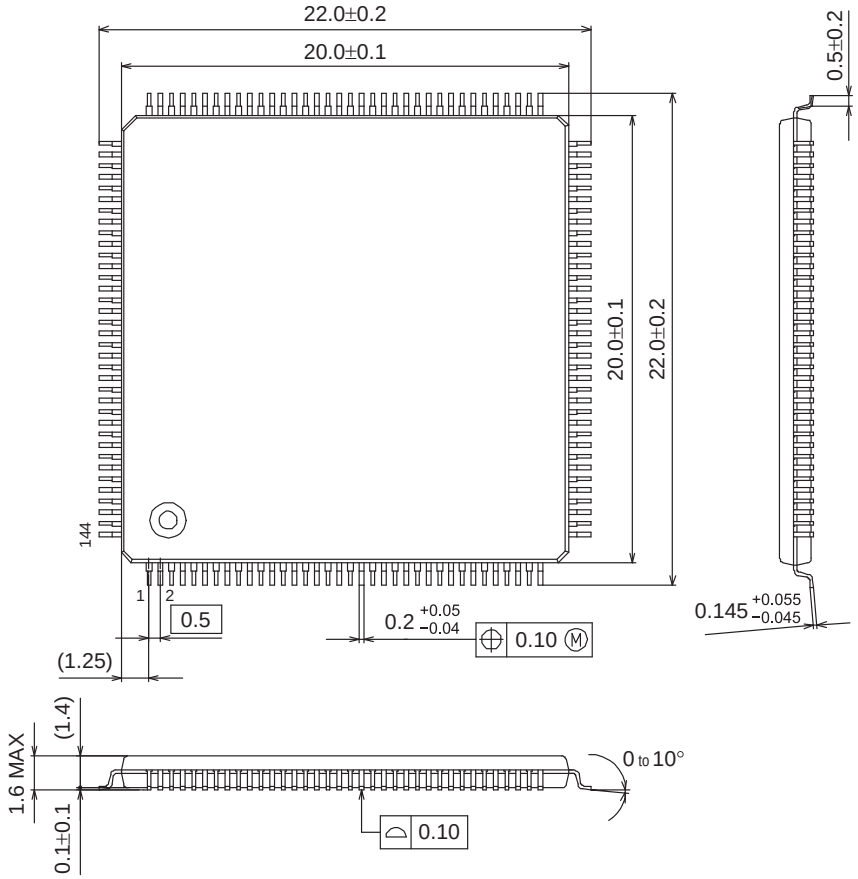
Pin Name (Pin No.)	Equivalent Circuit
EFMIN (1)	
RFOUT (2)	
LPF (3)	
PHLPF (4)	
AIN (5) CIN (6) BIN (7) DIN (8)	
SLCISET (9)	
RFMON (10)	

Pin Name (Pin No.)	Equivalent Circuit
VREF (11)	
JITTC (12)	
EIN (13) FIN (14)	
TE (15)	
TEIN (16)	
LDD (17)	
LDS (18)	

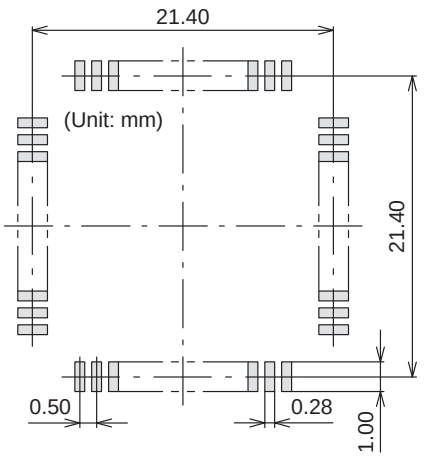
Pin Name (Pin No.)	Equivalent Circuit
FDO (23) TDO (24) SLDO (25) SPDO (26)	
PDOUT1 (28)	
PDOUT0 (29)	
PCKIST (31)	
AFILT (107)	
X16OUT (136) X16IN (137)	
SLCO (144)	

Package Dimensions
unit : mm

SPQFP144 20x20 / SQFP144
CASE 131AD
ISSUE A



SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*

XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “▪”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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