

ESD5482

ESD Protection Diode Micro-Packaged Diodes for ESD Protection

The ESD5482 is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, this part is well suited for use in cellular phones, MP3 players, digital cameras and many other portable applications where board space comes at a premium.

Specification Features

- Low Capacitance 5 pF
- Low Clamping Voltage
- Small Body Outline Dimensions: 0.60 mm x 0.30 mm
- Low Body Height: 0.3 mm
- Stand-off Voltage: 3.3 V
- Low Leakage
- Response Time is < 1 ns
- IEC61000-4-2 Level 4 ESD Protection
- IEC61000-4-4 Level 4 EFT Protection
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Mechanical Characteristics

MOUNTING POSITION: Any

QUALIFIED MAX REFLOW TEMPERATURE: 260°C

Device Meets MSL 1 Requirements

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000-4-2 (ESD) Contact Air		±10 ±10	kV
Total Power Dissipation on FR-5 Board (Note 1) @ T _A = 25°C	P _D	300	mW
Thermal Resistance, Junction-to-Ambient	R _{θJA}	400	°C/W
Junction and Storage Temperature Range	T _J , T _{stg}	-55 to +150	°C
Lead Solder Temperature - Maximum (10 Second Duration)	T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-5 = 1.0 x 0.75 x 0.62 in.

See Application Note AND8308/D for further description of survivability specs.



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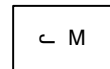
www.onsemi.com



X3DFN2
CASE 152AF

MARKING DIAGRAM

PIN 1



J = Specific Device Code
(Rotated 90° Clockwise)

ORDERING INFORMATION

Device	Package	Shipping†
ESD5482MUT5G	X3DFN2 (Pb-Free)	10000 / Tape & Reel

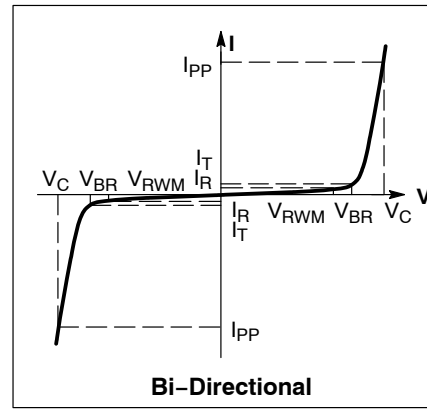
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I _{PP}	Maximum Reverse Peak Pulse Current
V _C	Clamping Voltage @ I _{PP}
V _{RWM}	Working Peak Reverse Voltage
I _R	Maximum Reverse Leakage Current @ V _{RWM}
V _{BR}	Breakdown Voltage @ I _T
I _T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V _{RWM}				3.3	V
Breakdown Voltage	V _{BR}	I _T = 1 mA (Note 2)	5.0			V
Reverse Leakage Current	I _R	V _{RWM} = 3.3 V		< 1	50	nA
Clamping Voltage	V _C	I _{PP} = 1 A (Note 3)		7.8	9.1	V
ESD Clamping Voltage	V _C	Per IEC61000-4-2	See Figures 1 and 2			
Junction Capacitance	C _J	V _R = 0 V, f = 1 MHz V _R = 0 V, f = 1 GHz		5.0 5.0	7.0 7.0	pF
Dynamic Resistance	R _{DYN}	TLP Pulse		0.60		Ω
Insertion Loss		f = 1 MHz f = 8.5 GHz		0.20 0.56		dB

- Breakdown voltage is tested from pin 1 to 2 and pin 2 to 1.
- Non-repetitive current pulse at 25°C, per IEC61000-4-5 waveform.

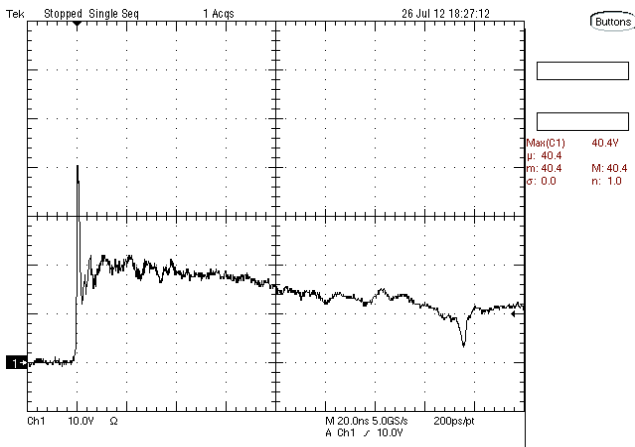


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2

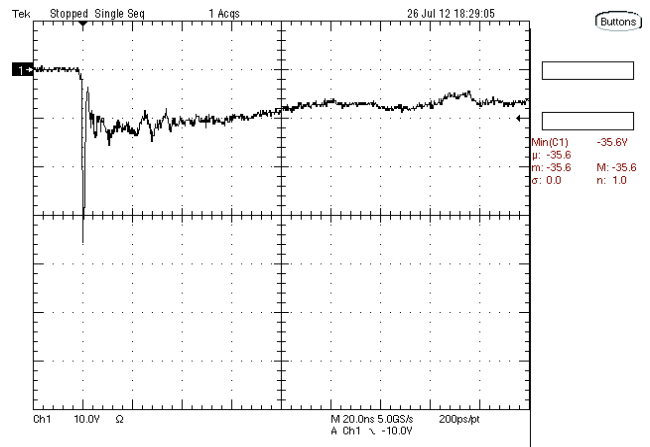


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2

TYPICAL CHARACTERISTICS

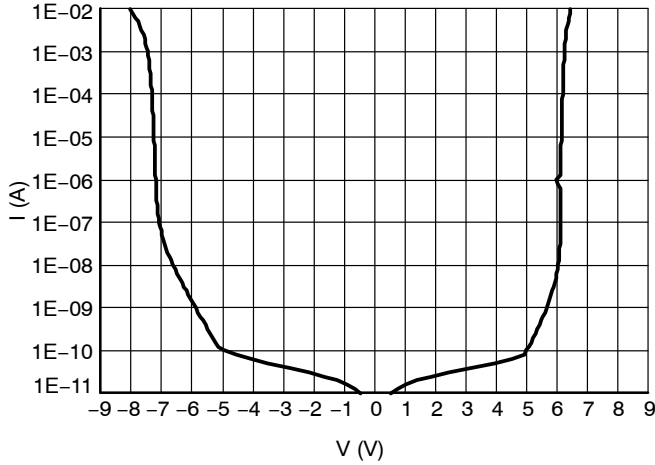


Figure 3. IV Characteristics

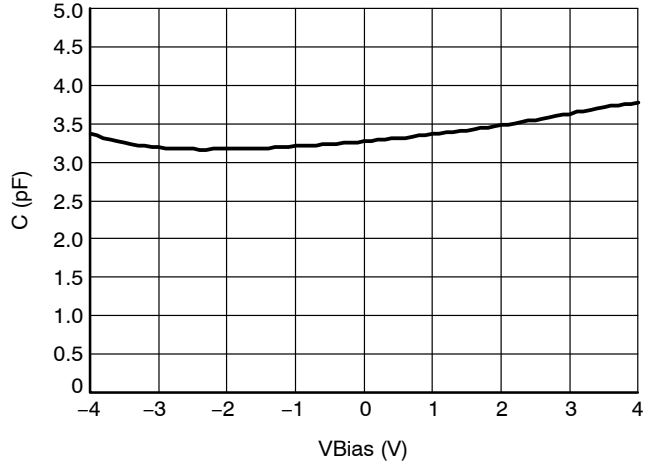


Figure 4. CV Characteristics

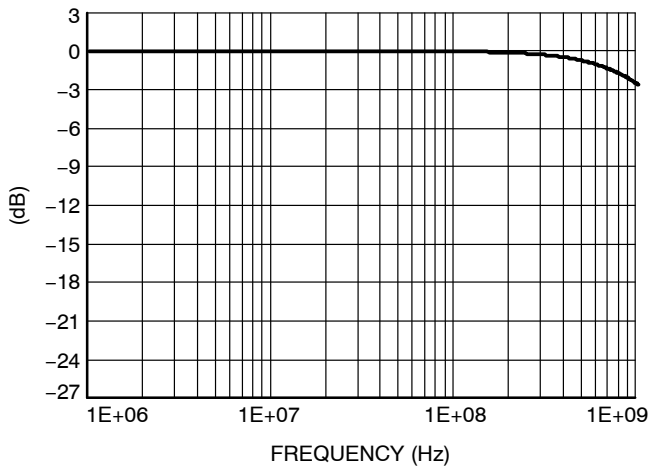


Figure 5. RF Insertion Loss

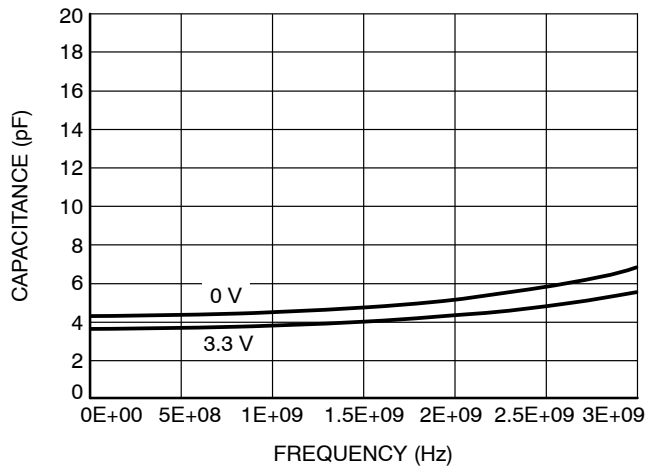


Figure 6. Capacitance over Frequency

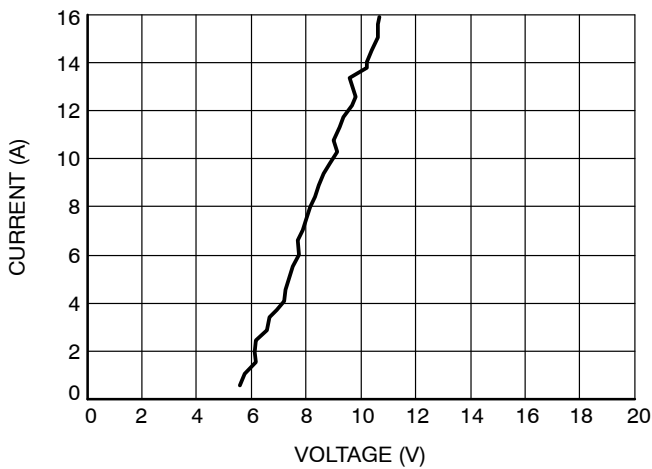


Figure 7. Positive TLP I-V Curve

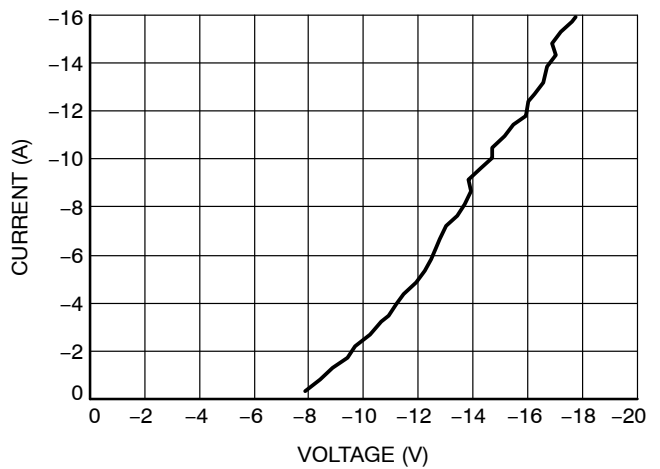


Figure 8. Negative TLP I-V Curve

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Figure 9. IEC61000-4-2 Spec

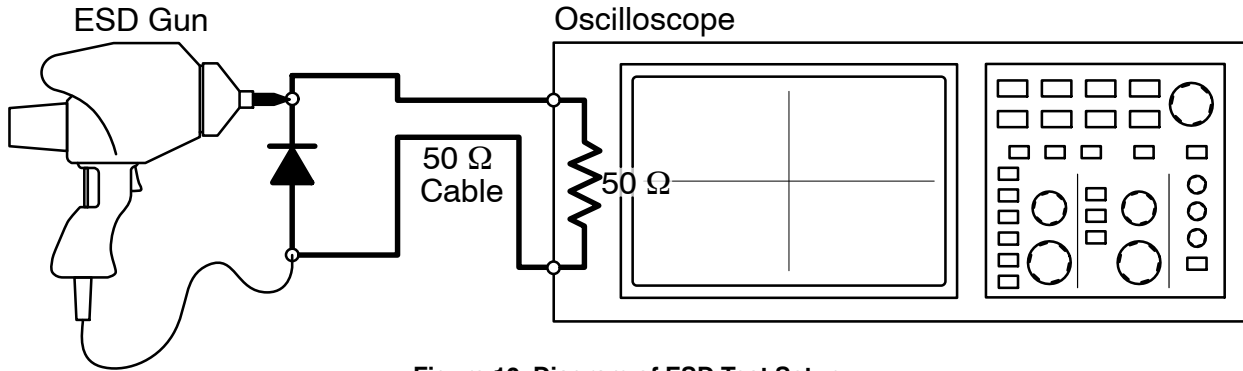


Figure 10. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

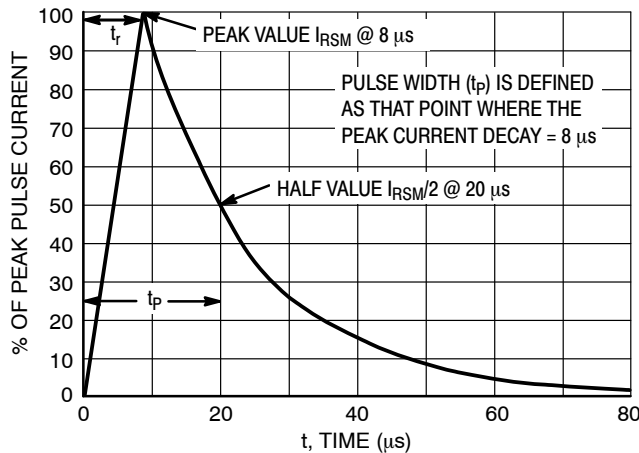
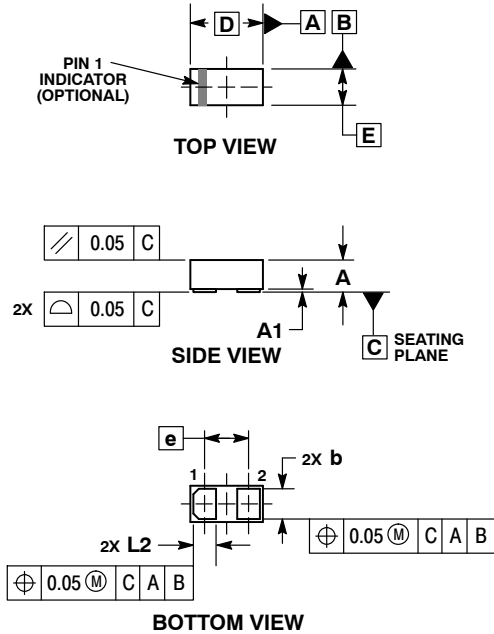


Figure 11. 8 X 20 μs Pulse Waveform

ESD5482

PACKAGE DIMENSIONS

X3DFN2, 0.62x0.32, 0.355P, (0201)
CASE 152AF
ISSUE A

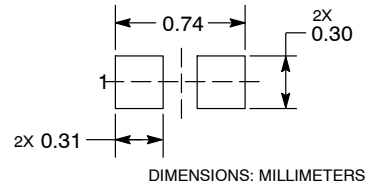


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

MILLIMETERS		
DIM	MIN	MAX
A	0.25	0.33
A1	---	0.05
b	0.22	0.28
D	0.58	0.66
E	0.28	0.36
e	0.355 BSC	
L2	0.17	0.23

RECOMMENDED MOUNTING FOOTPRINT*



See Application Note AND8398/D for more mounting details
 *For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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