AND9107/D

Guidelines for SMT Assembly of 0201 DSN Package

ON Semiconductor®

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APPLICATION NOTE

Package Overview

ON Semiconductor's 0.6 x 0.3 mm DSN (Dual Silicon No−lead) two pin package. This small package outline provides a component option that can be added to a design with minimal impact to the overall PCB area budget enhancing the ease of layout in space constrained applications.

The DSN package is a chip level package using solder−able metal contacts under the package similar to DFN style packages. The DSN style package enables 100% utilization of the package area for active silicon with, offering a significant performance per board area advantage compared to products in plastic molded packages. A finished package is shown in Figure 1.

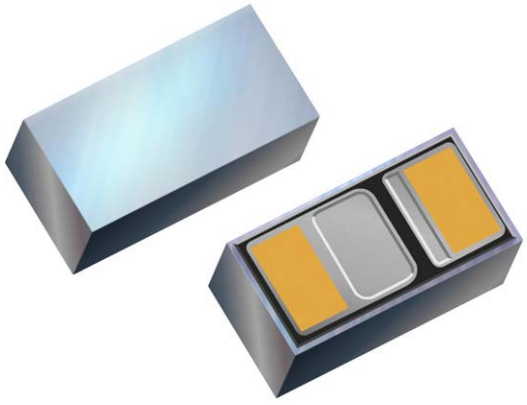

Figure 1. 0.60 mm x 0.30 mm Two−Lead Package

Component Placement

DSN packages must be mounted properly to avoid any misplacement which can result in well−soldered devices, for small 0201 DSN package with smaller pitch <0.45 mm NSMD pads is recommended, to provide a solder mask opening larger than the footprint of the package. This is a very critical step to prevent the tilting of devices from side−to−side or end−to−end and creating short circuit by solder/flux bridge as shown in Figures 2, 3 and 4.

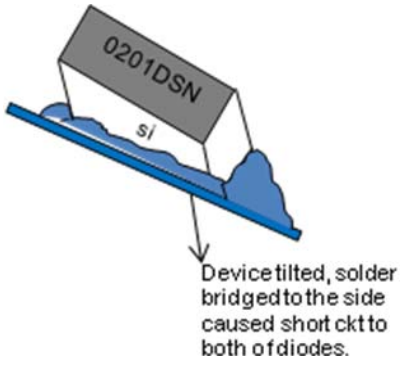

Figure 2. Solder Bridge

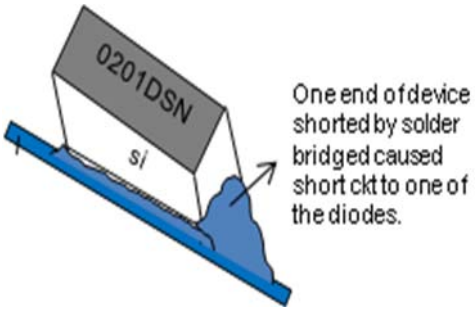

Figure 3. Solder Bridge

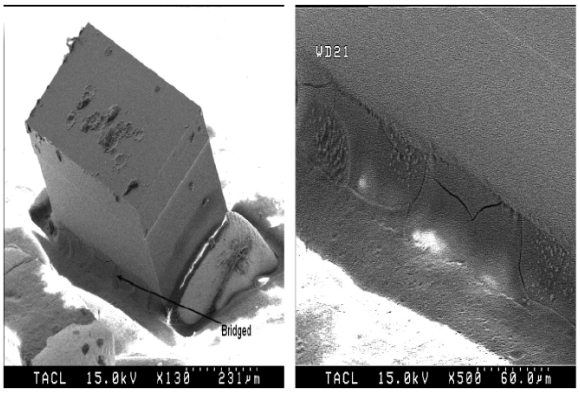

Figure 15: SEM image showing the other side of D2.

Figure 16: SEM image showing the continuous bridging by material (most probably flux).

Figure 4. Actual Solder Bridge Caused by Improper Mounting

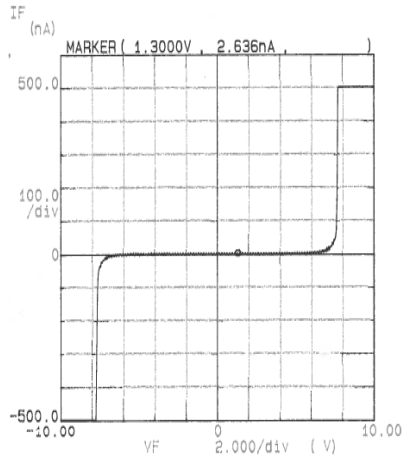

Figure 5. IV Curve Before Solder Bridge Caused by Improper Mounting

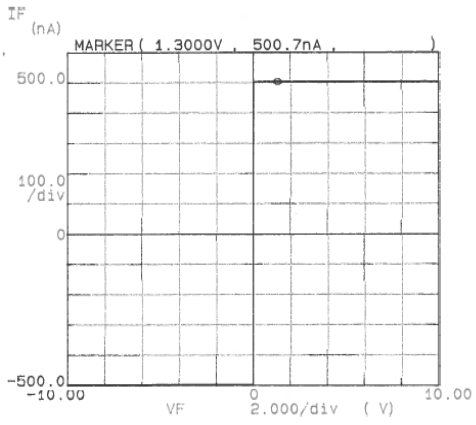

Figure 6. Short Circuit IV Caused by Improper Mounting

Recommended Board Mounting Process

The package board mounting process can be optimized by first defining and controlling the following:

1. Mounting pads.
2. Solder mask design guidelines.
3. Stencil for applying solder paste on to the PCB.
4. Choice of proper solder paste.
5. Package placement.
6. Reflow of the solder paste.
7. Final inspection of the solder joints.
8. PCB circuit traces width.

Figure 7 shows the size and orientation of the package on the recommended PCB mounting pads, solder mask and solder stencil.

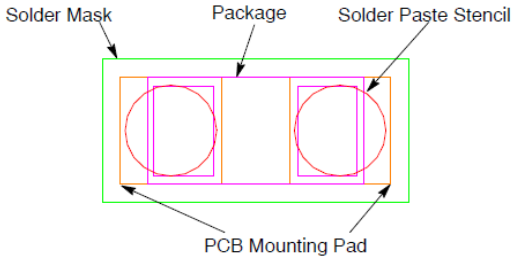

Figure 7. Recommended Mounting Pattern

Solder Mask

Two types of PCB solder mask openings commonly used for surface mount leadless style packages are:

1. Non Solder Masked Defined (NSMD)
2. Solder Masked Defined (SMD)

The solder mask is pulled away from the solder−able metallization for NSMD pads, while the solder mask overlaps the edge of the metallization for SMD pads as shown in Figure 8. For SMD pads, the solder mask restricts the flow of solder paste on the top of the metallization and prevents the solder from flowing down the side of the metal pad. This is different from the NSMD configuration where the solder flows both across the top and down the sides of the PCB metallization.

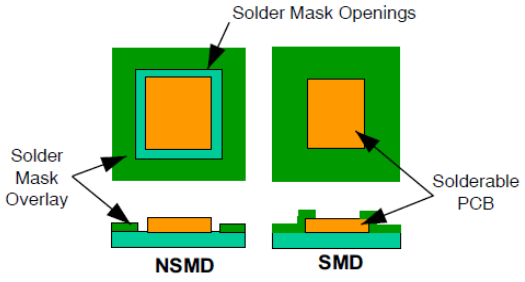

Figure 8. Comparison of NSMD vs. SMD Pads

NSMD pad is recommended over SMD pads. It is easier to define and control the location and size of copper pad verses the solder mask opening. This is because the copper etch process capability has a tighter tolerance than that of the solder mask process. NSMD pads also allow for easier visual inspection of the solder fillet.

Printed Circuit Board Solder Pad Design

Based on results of board mount testing, ON Semiconductor's recommended mounting pads and solder mask opening are shown in Figures 9 and 10. Maximum acceptable nPCB mounting pads and solder mask opening are shown in Figure 9, and summary in Table 1.

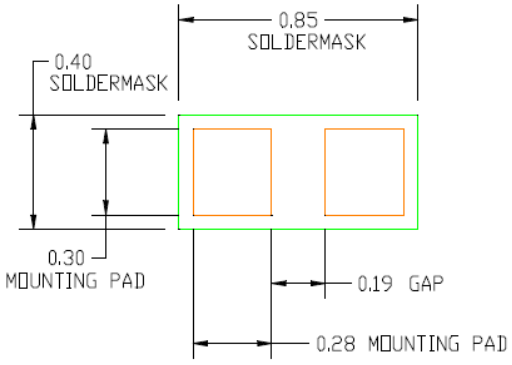

Figure 9. Recommended Mounting Pattern

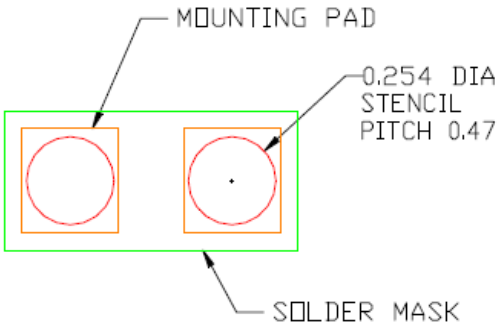

Figure 10. Recommended Stencil Pattern

Table 1. SOLDER PAD DESIGN

Parameters	Solder Mask
Solder Mask L	0.85 mm
Solder Mask W	0.45 mm
Mounting Pad L	0.30 mm
Mounting Pad W	0.35 mm
Stencil Thickness	80−120 μm
Stencil Aperture	~0.30 mm
Stencil Paste	90%wt alloy 10% system flux

Conclusions

The 0201 DSN2 package offers a 70% board space reduction from the popular 0402 outline. The guidelines outlined in this application note will ensure optimal board mounting results with maximized bond strength and minimal tilting causing short circuit, and avoiding misalignment between solder mask and board pads can result high SMT failure rate.

References

1. EIA 726:2002
   − 8 mm Punched And Embossed Carrier Taping Of Surface Mount Components For Automatic Handling Of Devices Generally Smaller Than 2.0 mm X 1.2 mm.
2. IEC 60286
   − 3 Packaging of components for automatic handling − Part 3: Packaging of Surface−Mount Devices (SMDs) or components on continuous tapes.
3. On Semiconductor
   − Board Application note − AND8398/D

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