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FSA642 低功率，3端口，高速 MIPI 开关

特性

- 低导通电容： 7.0pF（典型值）
- 低导通电阻： 7.0Ω（典型值）
- -3db带宽： 1GHz（典型值）
- 24-引脚 UMLP (2.5 x 3.4mm) 封装
- 额定值 8kV ESD ; >16kV Power/GND ESD

应用

- 手机上的双镜头应用
- 手机上的双 LCD 应用，数码相机显示和取景器

说明

FSA642是双向低功率高速模拟开关。引脚排列专为简化差分信号布局而设计，配置为三刀双掷开关 (TPDT)。

FSA642专为两个MIPI器件之间切换进行优化，如相机或液晶显示器以及板上多媒体应用处理器 (MAP)。

FSA642符合移动行业处理器接口 (MIPI) 的要求。低电容设计使得FSA642可切换频率超过500MHz的信号。出色的通道间抗串扰能力可以最大程度地减小干扰，实现MIPI规范所描述的高速差分信号和单端信号传输。

订购信息

器件编号	顶标	工作温度范围	封装
FSA642UMX	JG	-40 至 +85° C	24引脚，方形，超薄膜塑无铅封装 (UMLP)，2.5 x 3.4mm

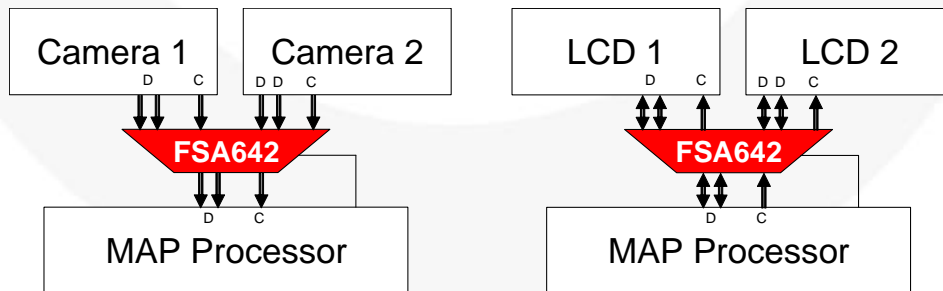


图 1. 应用模块图

引脚布局

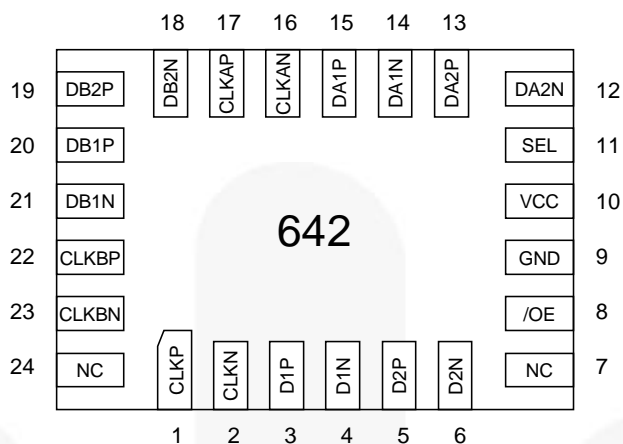


图 2. 引脚配置 (俯视图)

引脚说明

引脚号	名称	说明
1, 2	CLKP, CLKN	时钟路径 (公共)
3, 4	D1P, D1N	数据路径1 (公共)
5, 6	D2P, D2N	数据路径2 (公共)
7, 24	NC	未连接 (浮空)
8	/OE	输出使能 (低电平有效)
9	GND	接地
10	VCC	功率
11	SEL	选择 (0=A, 1=B)
12, 13	DA2N, DA2P	数据路径 (A2)
14, 15	DA1N, DA1P	数据路径 (A1)
16, 17	CLKAN, CLKAP	时钟路径 (A)
18, 19	DB2N, DB2P	数据路径 (2B)
20, 21	DB1P, DB1N	数据路径 (1B)
22, 23	CLKBP, CLKBN,	时钟路径 (B)

功能框图

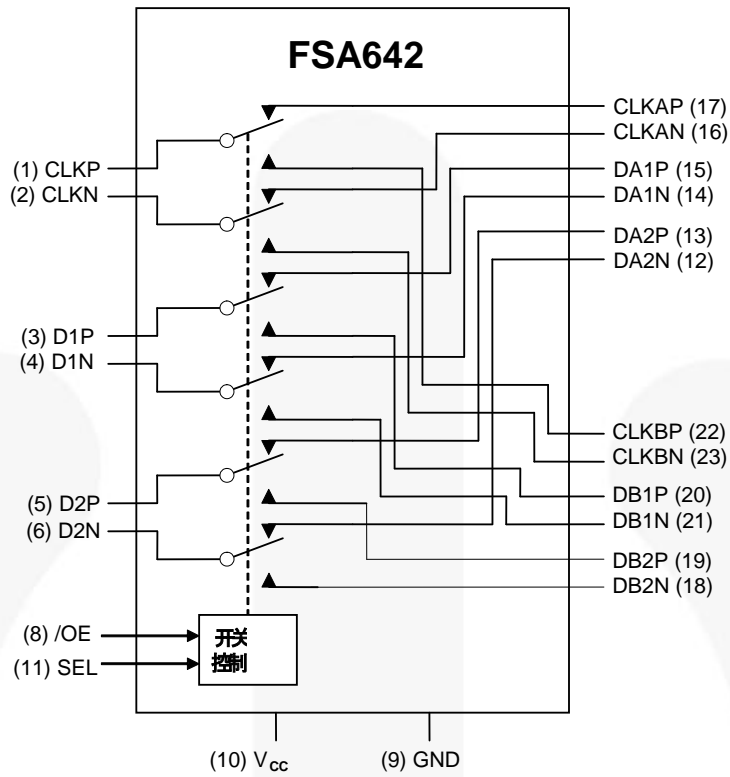


图 3. 功能框图

真值表

SEL	/OE	功能
无关	高	未连接
低	低	D1, D2, CLK=DA1, DA2, CLKA
高	低	D1, D2, CLK=DB1, DB2, CLKB

绝对最大额定值

应力超过绝对最大额定值, 可能会损坏设备。

在超出推荐的工作条件的情况下, 该器件可能无法正常运行或操作, 且不建议让器件在这些条件下长期工作。此外, 过度暴露在高于推荐的工作条件下, 会影响器件的可靠性。绝对最大额定值仅是额定应力值。

符号	参数	最小值	最大值	单位
V_{CC}	电源电压	-0.50	+5.25	V
V_{CTRL}	DC 输入电压 (SEL, /OE) ⁽¹⁾	-0.5	V_{CC}	V
V_{SW}	直流开关 I/O 电压 ⁽¹⁾	-0.5	$V_{CC} + 0.3$	V
I_{IK}	直流输入二极管电流	-50		mA
I_{OUT}	直流输出电流		50	mA
T_{STG}	存储温度	-65	+150	°C
ESD	人体模型, JEDEC: JESD22-A114	全部引脚	6.5	kV
		输入/输出至地	8.0	
		电源至地	16.0	
	充电器件模型, JEDEC: JESD22-C101	2.5		

注意:

- 当测量输入与输出二极管电流额定值时, 该输入与输出可能超出负额定值。

推荐工作条件

推荐的操作条件表定义了器件的真实工作条件。指定推荐的工作条件, 以确保设备的最佳性能达到数据表中的规格。飞兆半导体建议不要超过推荐工作条件, 也不能按照绝对最大额定值进行设计。

符号	参数	最小值	最大值	单位
V_{CC}	电源电压	2.65	4.30	V
V_{CTRL}	控制输入电压 (SEL, /OE) ⁽²⁾	0	V_{CC}	V
V_{SW}	开关 I/O 电压	-0.5	$V_{CC}-1$	V
T_A	工作温度	-40	+85	°C

注意:

- 控制输入必须保持高电平或低电平, 不允许浮空。

直流电气特性

若无其他说明, 所有典型值都在 $T_A=25^\circ\text{C}$ 下测得。

符号	参数	工作条件	V_{CC} (V)	$T_A=-40$ 至 $+85^\circ\text{C}$			单位
				最小值	典型值	最大值	
V_{IK}	箝位二极管电压	$I_{IN}=-18\text{mA}$	2.775			-1.2	V
I_{IN}	控制脚输入漏电流	$V_{SW}=0$ to 4.3V	4.3	-1		1	μA
V_{IH}	输入电压高电平	$V_{IN}=0$ 至 V_{CC}	2.650 至 2.775	1.3			V
			4.3	1.7			
V_{IL}	输入电压低电平	$V_{IN}=0$ 至 V_{CC}	2.650 至 2.775			0.5	V
I_{OZ}	关断漏电流	A, B=0+0.3V to $V_{CC}-0.3$	4.3	-2		2	μA
I_{CC}	静态电源电流	$V_{CTRL}=0$ or V_{CC} , $I_{OUT}=0$	4.3			1.0	μA
I_{CCT}	每个控制电压和 V_{CC} 的 I_{CC} 电流增量	$V_{CTRL}=1.8\text{V}$	2.775			1.5	μA

直流电气特性, 低速模式

若无其他说明, 所有典型值都在 $T_A=25^\circ\text{C}$ 下测得。

符号	参数	工作条件	V_{CC} (V)	$T_A=-40$ 至 $+85^\circ\text{C}$			单位
				最小值	典型值	最大值	
R_{ON}	LS 开关导通电阻 ⁽³⁾	$V_{SW}=1.2\text{V}$, $I_{ON}=-10\text{mA}$, 图 4	2.65		10	14	Ω
ΔR_{ON}	LS Delta R_{ON} ⁽⁴⁾	$V_{SW}=1.2\text{V}$, $I_{ON}=-10\text{mA}$ (内部成对)	2.65		0.65		Ω

说明:

- 在指定通过电流下, 由A/B 和 CLK/Dn引脚之间的电压降测得。
- 由产品特性保证。

直流电气特性, 高速模式

若无其他说明, 所有典型值都 $T_A=25^\circ\text{C}$ 下测得。

符号	参数	工作条件	V_{CC} (V)	$T_A=-40$ 至 $+85^\circ\text{C}$			单位
				最小值	典型值	最大值	
R_{ON}	HS 开关导通电阻 ⁽⁵⁾	$V_{SW}=0.4\text{V}$, $I_{ON}=-10\text{mA}$, 图 4	2.65		7.0	9.5	Ω
ΔR_{ON}	HS Delta R_{ON} ⁽⁶⁾	$V_{SW}=0.4\text{V}$, $I_{ON}=-10\text{mA}$ (内部成对)	2.65		0.65		Ω

说明:

- 在指定通过电流下, 由A/B 和 Dn引脚之间的电压降测得。
- 由产品特性保证。

交流电气特性

所有值的测量条件为 $R_L=50\Omega$ 和 $R_S=50\Omega$ ，典型值为 $V_{CC}=2.775V$ ， $T_A=25^\circ C$ ，除非另有说明。

符号	参数	工作条件	V_{CC} (V)	$T_A=-40^\circ C$ 至 $+85^\circ C$			单位
				最小值	典型值	最大值	
O_{IRR}	关断隔离 ⁽⁷⁾	$f=100MHz$, $R_I=50\Omega$ 图 14	2.775		-35		dB
Xtalk	非相邻通道串扰 ⁽⁷⁾	$f=100MHz$, $R_I=50\Omega$ 图 15	2.775		-55		dB
BW	-3db 带宽 ⁽⁷⁾	$C_L=0pF$, $R_I=50\Omega$ 图 13	2.775		1.0		GHz
t_{ON}	开机时间SEL, /OE 至输出	$C_L=5pF$, $V_{SW}=1.2V$ 图 6, 图 7	2.650 至 2.775		20	37	ns
t_{OFF}	关断时间SEL, /OE 至输出	$C_L=5pF$, $V_{SW}=1.2V$ 图 6, 图 7	2.650 至 2.775		15	27	ns
t_{PD}	传输延迟 ⁽⁷⁾	$C_L=5pF$ 图 6, 图 8	2.775		0.25		ns
t_{BBM}	“先开后合”时间	$C_L=5pF$, $V_{SW1}=V_{SW2}=1.2V$ 图 12	2.650 至 2.775	3	5	8	ns

注意:

7. 由产品特性保证。

交流电气特性，高速模式

若无其他说明，所有典型值都在 $V_{CC}=2.775V$ ， $T_A=25^\circ C$ 下测得。

符号	参数	工作条件	$T_A=-40^\circ C$ 至 $+85^\circ C$			单位
			最小值	典型值	最大值	
$t_{SK(Part_Part)}$	多器件通道间相位差 ^(8,9)	$V_{SW}=0.2Vdiff_{PP}$, $C_L=5pF$		40	80	ps
$t_{SK(Ch1_Ch1)}$	单器件通道间相位差 ⁽⁸⁾	$V_{SW}=0.2Vdiff_{PP}$, $C_L=5pF$, 图 9		15	30	ps
$t_{SK(脉冲)}$	同一差分通道内的反向转换相位差 ⁽⁸⁾	$V_{SW}=0.2Vdiff_{PP}$, $C_L=5pF$		10	20	ps

说明:

8. 由产品特性保证。

9. 假设所有器件应用相同的 V_{CC} 和温度。

电容值

符号	参数	工作条件	$T_A=-40^\circ C$ 至 $+85^\circ C$			单位
			最小值	典型值	最大值	
C_{IN}	控制引脚输入电容 ⁽¹⁰⁾	$V_{CC}=0V$		1.5		pF
C_{ON}	Dn/CLK- 导通电容 ⁽¹⁰⁾	$V_{CC}=2.775V$, /OE=0V, $f=1MHz$, at $25^\circ C$ 图 11	6.0	7.0	9.0	
C_{OFF}	Dn/CLK- 关断电容 ⁽¹⁰⁾	$V_{CC}=2.775V$, /OE=2.775V, $f=1MHz$ 图 10		2.5		

注意:

10. 由产品特性保证。

测试框图

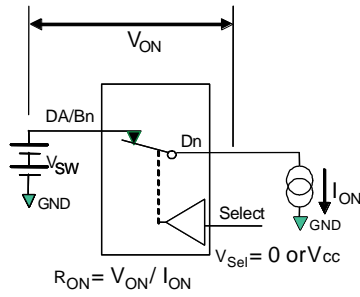
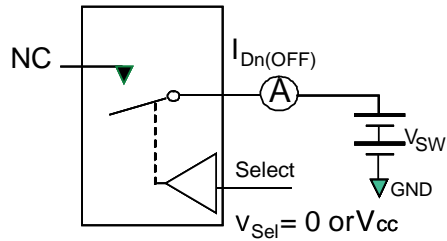
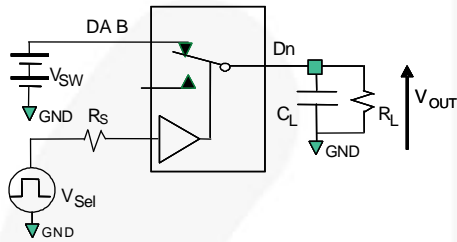


图 4. 导通电阻



**Each switch port is tested separately

图 5. 关断漏电流



R_L , R_S , and C_L are functions of application environment (see AC Tables for specific values). C_L includes test fixture and stray capacitance.

图 6. 交流测试电路负载

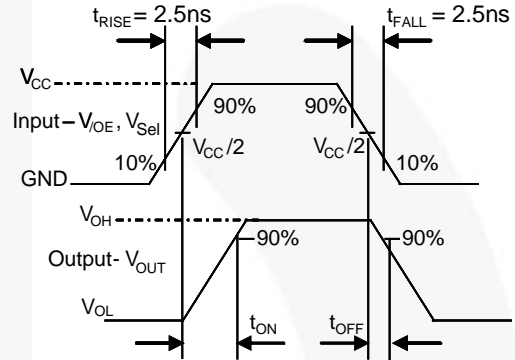


图 7. 开通/关断波形

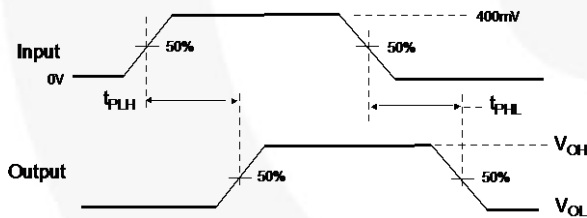


图 8. 传输延迟 ($t_{rTf} = 500ps$)

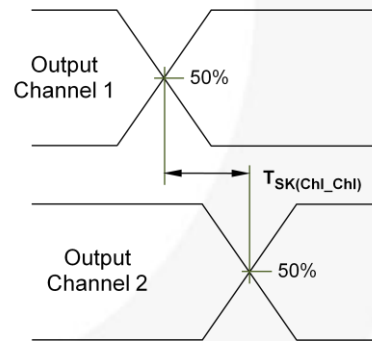


图 9. 通道间相位差

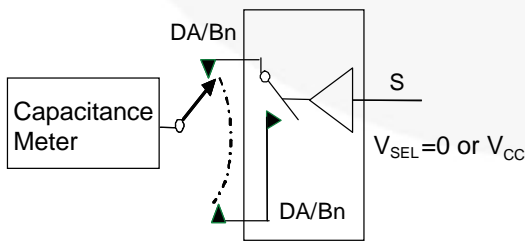


图 10. 通道关断电容

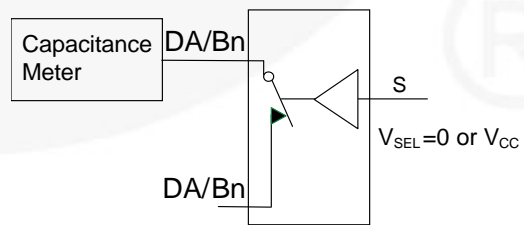


图 11. 通道导通电容

测试框图 (续)

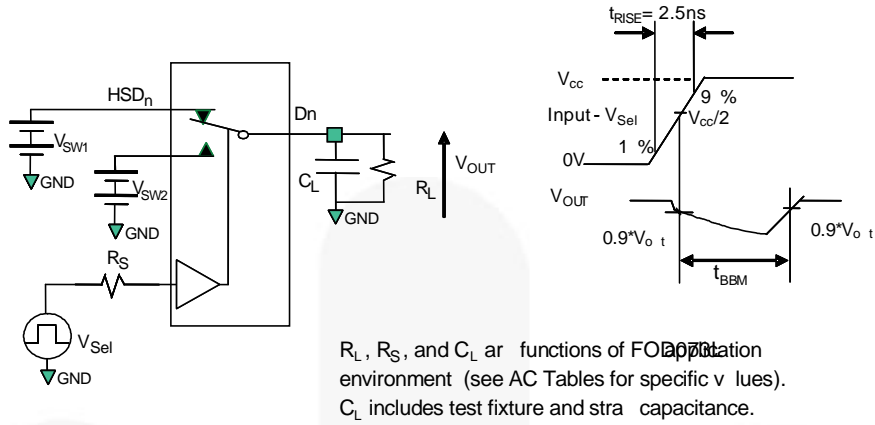


图 12. 先开后合间隔时序

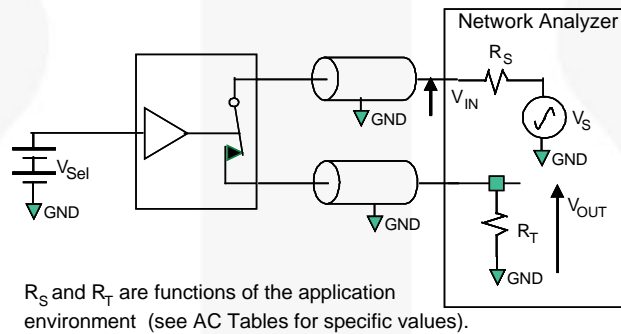


图 13. 带宽

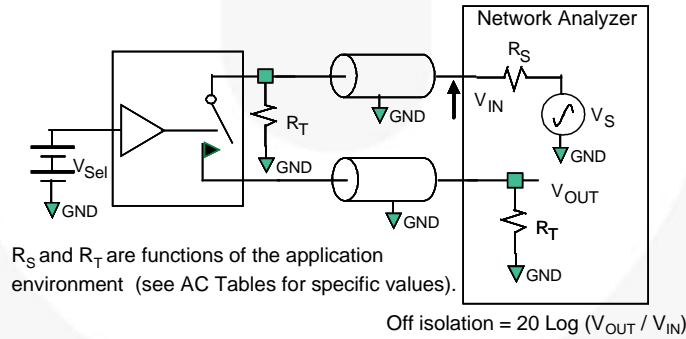


图 14. 通道的关断隔离

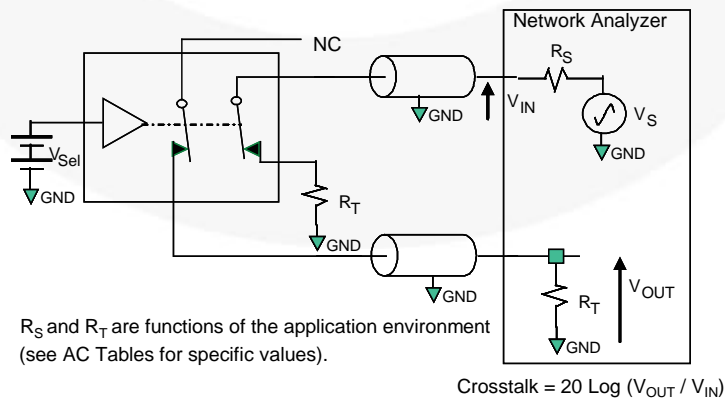
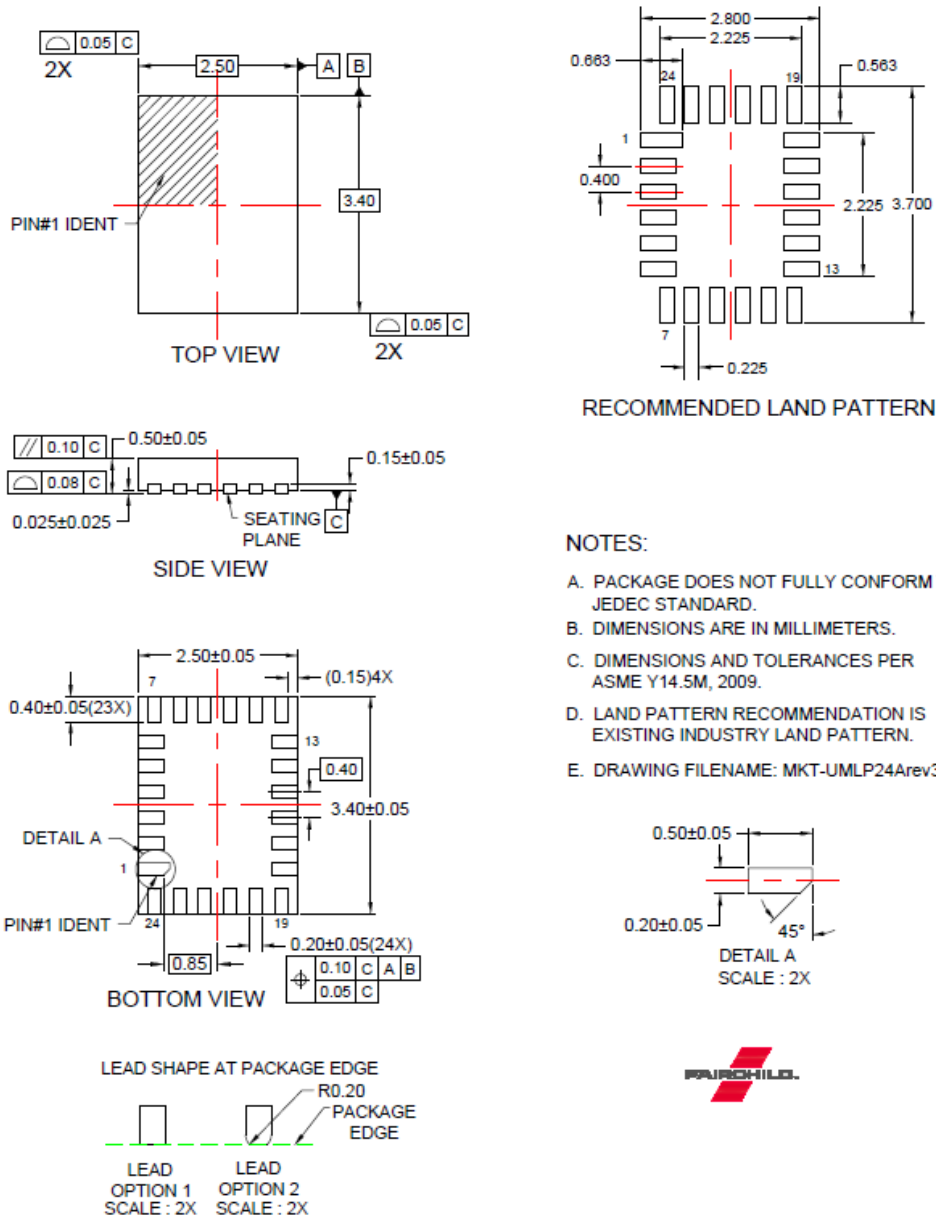


图 15. 非相邻通道间串扰

物理尺寸测试



- NOTES:
- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
 - D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
 - E. DRAWING FILENAME: MKT-UMLP24Arev3.



图 16. 24-引脚, UMLP

Product-Specific Dimensions

Description	Nominal Values (mm)
Overall Height	0.500
Pkg Standoff	0.026
Lead Thickness	0.152
Lead Width (24x)	0.200

Description	Nominal Values (mm)
Lead Length (23x)	0.4
Lead Length, Pin 1 (1x)	0.5
Lead Pitch	0.4
Body Length (X)	3.4
Body Width (Y)	2.5

2.5x3.4 UMLP24L Packing - Embossed Tape FSA642UMX

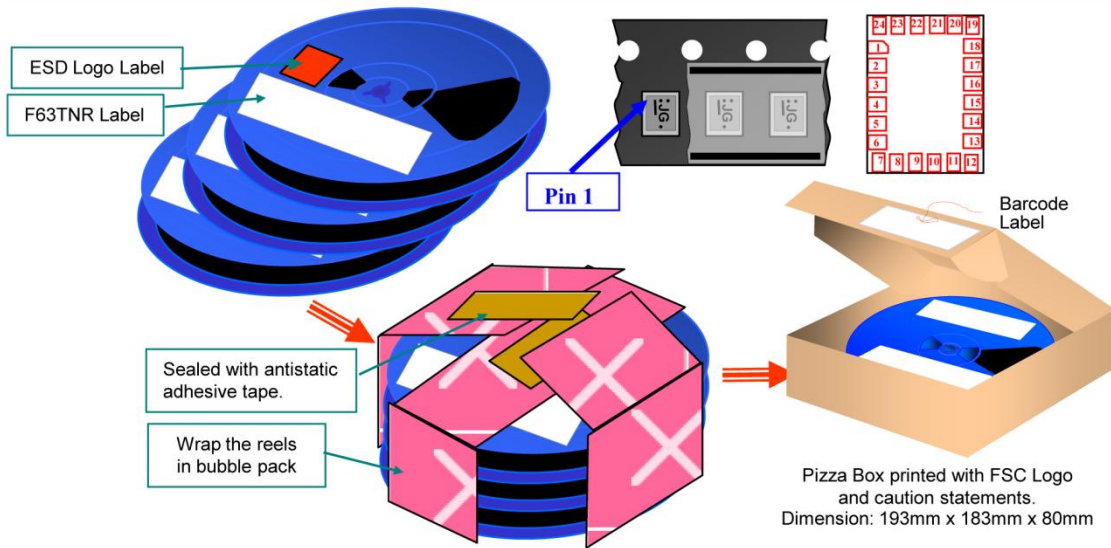


Packing Description:

UMLP 24 pins products are classified under Moisture Sensitive Level 1.

The carrier tape is made from dissipative polystyrene or polycarbonate resin. The cover tape is a multilayer film primarily composed of polyester film, adhesive layer, heat activated sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 5000 units per 178 mm diameter reel. Up to three reels are packed in each intermediate box. The reels is made of polystyrene plastic (anti-static coated or intrinsic).

These full reels are individually barcode labeled and placed inside a pizza box made of recyclable corrugated brown paper with a Fairchild logo printing. The reel is packed single reel in the pizza box. And these pizza boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.



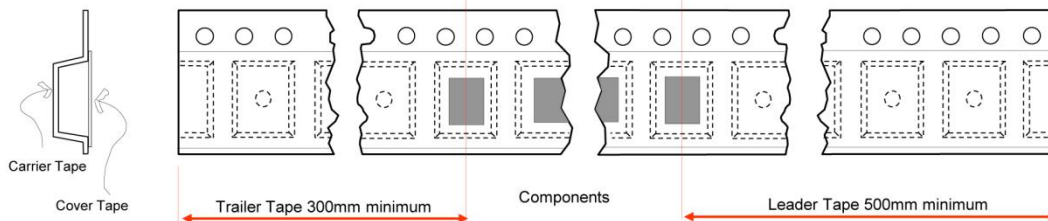
ESD Logo Label sample



Sample of F63TNR Label

LOT: PMH01008888	QTY: 5000
FSID: FSA642UMX	SPEC:
D/C1: P1215NA QTY1:	SPEC REV: 2 nd Level Interconnect
D/C2: QTY2:	1. Category G3
Green Component	2. Maximum safe temperature 260 deg C
RoHS COMPLIANT	3. MSL 1
	FAIRCHILD SEMICONDUCTOR (F63TNR)6.0

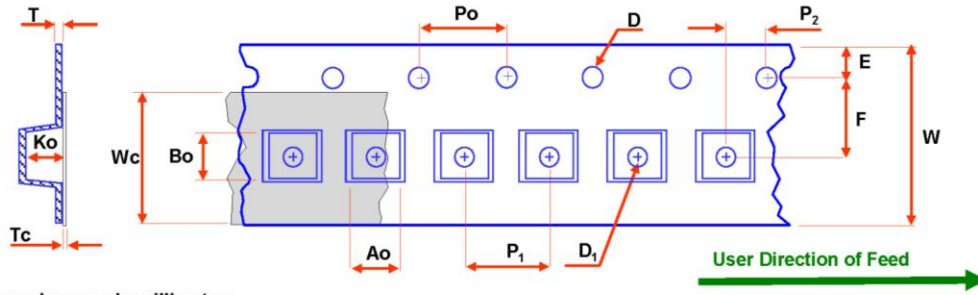
Tape Leader and Trailer Configuration



Rev 1 170810

图 17. Tape and Reel Packing Specification, page 1

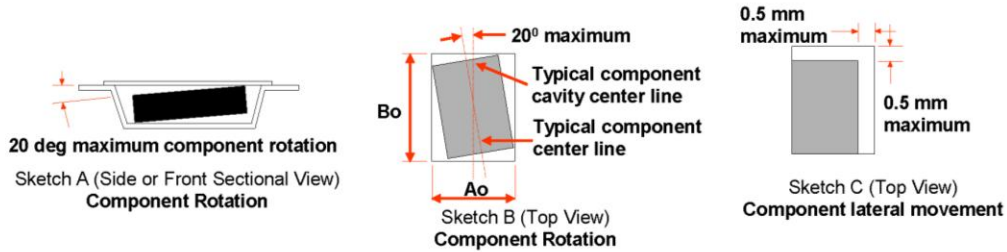
UMLP Embossed Tape Dimension



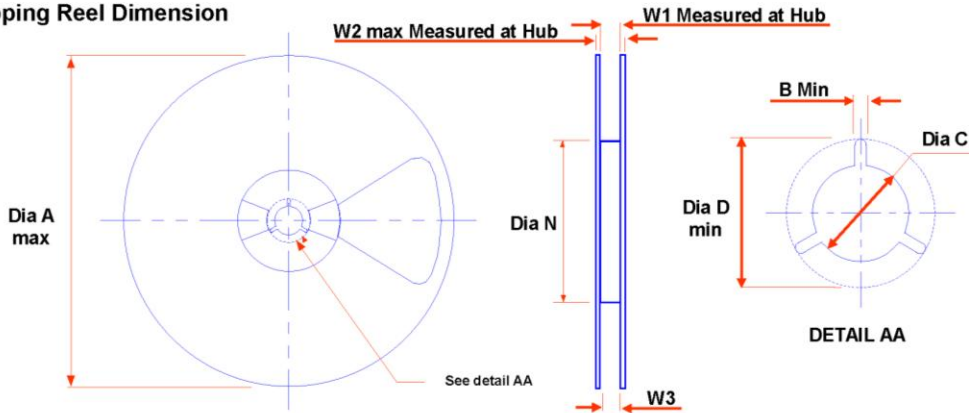
Dimensions are in millimeters

Package	Ao	Bo	D	D ₁	E	F	Ko	P ₁	Po	P ₂	T	Tc	W	Wc
UMLP24A	2.70 +/-0.05	3.60 +/-0.05	1.50 +/-0.10	0.6 +/-0.05	1.75 +/-0.1	3.5 +/-0.05	0.70 +/-0.05	4 TYP	4 TYP	2.0 +/-0/05	0.254 TYP	0.06 +/-0.005	8 +/-0.3	5.5 TYP

Notes: Ao, Bo, and Ko dimensions are determined with respect to the EIA /Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Shipping Reel Dimension



Dimensions are in millimeters

Tape Width	Dia A max	Dim B min	Dia C +5/-2	Dia D min	Dim N min	Dim W1 +2/-0	Dim W2 max	Dim W3 (LSL - USL)
8	178	1.5	13	20.2	55	8.4	14.4	7.9~10.9

图 18. Tape and Reel Packing Specification, page 2



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