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FPF2C110BI07AS2

F2, Boost and Inverter module with Press-fit

General Description

Fairchild's Boost and H-Bridge module is designed for a power stage that needs more compact design. And the Press-fit technology provides simple and reliable mounting. This module is optimized for the application such as solar inverter where a high efficiency and robust design are needed.

Electrical Features

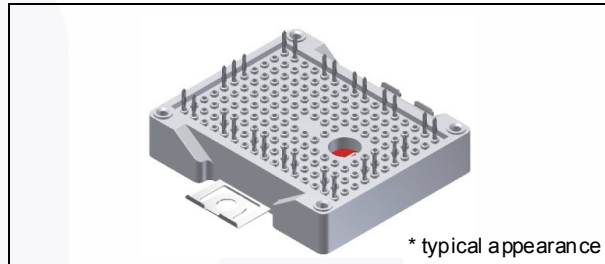
- Boost Stage
 - Dual Boost Topology
 - SiC Boost Diode
 - Low $R_{DS(ON)}$ Boost Switch
 - Low V_F and High Voltage Bypass Diode
- Inverter Stage
 - H-bridge Topology
 - High Speed IGBT and Fast Recovery FWD
- Integrated DC-capacitor for Boost and Inverter
- Temperature Sensor

Mechanical Features

- Compact size : F2 Package
- Press-fit Contact Technology
- Al_2O_3 Substrate with Low Thermal Resistance

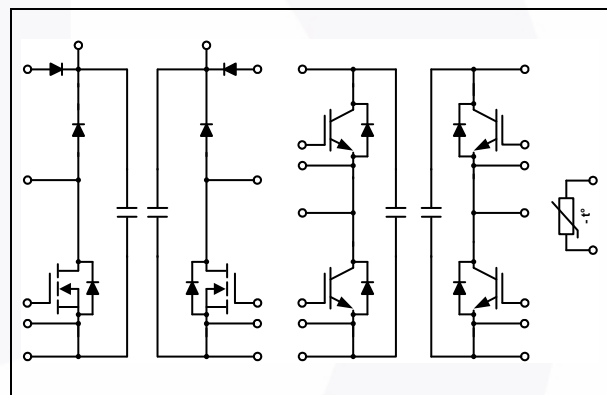
Applications

- Solar Inverter



* typical appearance

Package Code: F2



Internal Circuit Diagram

Package Marking and Ordering Information

Device	Device Marking	Package	Packing Type	Quantity / Tray
FPF2C110BI07AS2	FPF2C110BI07AS2	F2	Tray	14

FPF2C110BI07AS2 F2, Boost and Inverter module with Press-fit

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Description	Condition	Rating	Units
Bypass Diode (DA1, DA2)				
V_{RRM}	Peak Repetitive Reverse Voltage		1000	V
I_F	Continuous Forward Current	$T_C = 80^\circ\text{C}, T_{Jmax} = 175^\circ\text{C}$	50	A
I_{FSM}	Non-repetitive Peak Surge Current	60 Hz Single Half-Sine Wave	350	A
I^2t	Surge Current Integral Value		510	A^2s
P_D	Maximum Power Dissipation	$T_{Jmax} = 175^\circ\text{C}$	300	W
T_J	Operating Junction Temperature		- 40 to + 150	$^\circ\text{C}$
Boost Diode (DB1, DB2)				
V_{RRM}	Peak Repetitive Reverse Voltage		650	V
I_F	Continuous Forward Current	$T_C = 80^\circ\text{C}, T_{Jmax} = 175^\circ\text{C}$	10	A
I_{FSM}	Non-repetitive Peak Surge Current	60 Hz Single Half-Sine Wave	40	A
I^2t	Surge Current Integral Value		6.6	A^2s
P_D	Maximum Power Dissipation	$T_{Jmax} = 175^\circ\text{C}$	90	W
T_J	Operating Junction Temperature		- 40 to + 150	$^\circ\text{C}$
Boost MOSFET (M1, M2)				
V_{DSS}	Drain-Source Voltage		650	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current	$T_C = 25^\circ\text{C}, T_{Jmax} = 150^\circ\text{C}$	25	A
		$T_C = 80^\circ\text{C}, T_{Jmax} = 150^\circ\text{C}$	19	A
I_{DM}	Pulsed Drain Current	limited by T_{Jmax}	50	A
P_D	Maximum Power Dissipation	$T_{Jmax} = 150^\circ\text{C}$	199	W
T_J	Operating Junction Temperature		- 40 to + 150	$^\circ\text{C}$
H-bridge IGBT (QA, QB, QC, QD)				
V_{CES}	Collector-Emitter Voltage		650	V
V_{GES}	Gate-Emitter Voltage		± 20	V
I_C	Collector Current	$T_C = 80^\circ\text{C}, T_{Jmax} = 175^\circ\text{C}$	40	A
I_{CM}	Pulsed Collector Current	limited by T_{Jmax}	80	A
P_D	Maximum Power Dissipation	$T_{Jmax} = 175^\circ\text{C}$	158	W
T_J	Operating Junction Temperature		- 40 to + 150	$^\circ\text{C}$
H-bridge FWD (QAD, QBD, QCD, QDD)				
V_{RRM}	Peak Repetitive Reverse Voltage		650	V
I_F	Diode Forward Current	$T_C = 80^\circ\text{C}, T_{Jmax} = 175^\circ\text{C}$	30	A
I_{FM}	Pulsed Maximum Forward Currents	limited by T_{Jmax}	60	A
P_D	Maximum Power Dissipation	$T_{Jmax} = 175^\circ\text{C}$	109	W
T_J	Operating Junction Temperature		- 40 to + 150	$^\circ\text{C}$
DC Link Capacitor				
V_{MAX}	Maximum DC Voltage		1000	V
T_{OP}	Operating Temperature		- 55 to + 125	$^\circ\text{C}$

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Description	Condition	Rating	Units
Module				
T_{STG}	Storage Temperature		- 40 to + 125	$^\circ\text{C}$
V_{ISO}	Isolation Voltage	AC 1 min.	2500	V
Iso_Material	Internal Isolation Material		Al_2O_3	-
T_{MOUNT}	Mounting Torque ₍₁₎		2.4	N•m
Creepage	Terminal to Heat Sink		11.5	mm
	Terminal to Terminal		6.3	mm
Clearance	Terminal to Heat Sink		10.0	mm
	Terminal to Terminal		5.0	mm

Notes:

1. Recommendable value : 2.0 ~ 2.4 Nm (M4)

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted. **Parantheses value is based on the discrete.**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
Bypass Diode (DA1, DA2)							
V_F	Diode Forward Voltage	$I_F = 50\text{ A}$	-	1.37	1.7	V	
		$I_F = 50\text{ A}, T_C = 125^\circ\text{C}$	-	1.3	-	V	
I_R	Reverse Leakage Current	$V_R = 1000\text{ V}$	-	-	250	μA	
$R_{\theta JC}$	Thermal Resistance of Junction to Case	per Diode	-	-	0.49	$^\circ\text{C/W}$	
$R_{\theta CH}$	Thermal Resistance of Case to Heat sink	per Chip, $\lambda_{PCM} = 3.4\text{ W/mK}$	-	0.56	-	$^\circ\text{C/W}$	
Boost Diode (DB1, DB2)							
V_F	Diode Forward Voltage	$I_F = 10\text{ A}$	-	1.42	1.58	V	
		$I_F = 10\text{ A}, T_C = 125^\circ\text{C}$	-	1.61	-	V	
I_R	Reverse Leakage Current	$V_R = 650\text{ V}$	-	-	250	μA	
I_{rr}	Reverse Recovery Current	$V_R = 300\text{ V}, I_F = 10\text{ A},$ $di/dt = 1560\text{ A/us},$ $T_C = 25^\circ\text{C}$	-	6	-	A	
Q_C	Total Capacitive Charge		-	60	-	nC	
E_{rec}	Reverse Recovery Energy		-	7.5	-	μJ	
I_{rr}	Reverse Recovery Current	$V_R = 300\text{ V}, I_F = 10\text{ A},$ $di/dt = 1560\text{ A/us},$ $T_C = 125^\circ\text{C}$	-	6	-	A	
Q_C	Total Capacitive Charge		-	61	-	nC	
E_{rec}	Reverse Recovery Energy		-	7.5	-	μJ	
$R_{\theta JC}$	Thermal Resistance of Junction to Case	per Chip	-	-	1.63	$^\circ\text{C/W}$	
$R_{\theta CH}$	Thermal Resistance of Case to Heat sink	per Chip, $\lambda_{PCM} = 3.4\text{ W/mK}$	-	0.42	-	$^\circ\text{C/W}$	
Boost MOSFET (M1, M2)							
Off Characteristics							
V_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	650	-	-	V	
I_{DSS}	Drain Cut-off Current	$V_{DS} = V_{DSS}, V_{GS} = 0\text{ V}$	-	-	250	μA	
I_{GSS}	Gate-Source Leakage Current	$V_{GS} = V_{GSS}, V_{DS} = 0\text{ V}$	-	-	± 1	μA	
On Characteristics							
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0	3.9	5.0	V	
$R_{DS(on)}$	Static Drain-Source On Resistance	$I_D = 17.5\text{ A}, V_{GS} = 10\text{ V}$	-	110	137	$\text{m}\Omega$	
V_{SD}	Drain-Source Diode Forward Voltage	$I_{SD} = 17.5\text{ A}, V_{GS} = 0\text{ V}$	-	1.07	1.37	V	
		$I_{SD} = 17.5\text{ A}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	0.93	-	V	
R_{LEAD}	Lead Resistance of Pin to Chip	per Chip	-	3.2	-	$\text{m}\Omega$	
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	$V_{CC} = 300\text{ V}$ $I_D = 17.5\text{ A}$ $V_{GS} = 10\text{ V}$ $R_G = 4.7\ \Omega$ Inductive Load $T_C = 25^\circ\text{C}$	-	27	-	ns	
t_r	Rise Time		-	5.0	-	ns	
$t_{d(off)}$	Turn-Off Delay Time		-	3.0	-	ns	
t_f	Fall Time		-	5.5	-	ns	
E_{ON}	Turn-On Switching Loss per Pulse		-	33	-	μJ	
E_{OFF}	Turn-Off Switching Loss per Pulse		-	20	-	μJ	
$t_{d(on)}$	Turn-On Delay Time		$V_{CC} = 300\text{ V}$ $I_D = 17.5\text{ A}$ $V_{GS} = 10\text{ V}$ $R_G = 4.7\ \Omega$ Inductive Load $T_C = 125^\circ\text{C}$	-	26	-	ns
t_r	Rise Time		-	5.3	-	ns	
$t_{d(off)}$	Turn-Off Delay Time		-	87	-	ns	
t_f	Fall Time		-	6.0	-	ns	
E_{ON}	Turn-On Switching Loss per Pulse	-	39	-	μJ		
E_{OFF}	Turn-Off Switching Loss per Pulse	-	21	-	μJ		
Q_g	Total Gate Charge	$V_{CC} = 300\text{ V}, I_{SD} = 17.5\text{ A}, V_{GS} = 10\text{ V}$	-	84	-	nC	
$R_{\theta JC}$	Thermal Resistance of Junction to Case	per Chip	-	-	0.63	$^\circ\text{C/W}$	
$R_{\theta CH}$	Thermal Resistance of Case to Heat sink	per Chip, $\lambda_{PCM} = 3.4\text{ W/mK}$	-	0.49	-	$^\circ\text{C/W}$	

Electrical Characteristics $T_C = 25\text{ }^\circ\text{C}$ unless otherwise noted. **Parantheses value is based on the discrete.**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
H-Bridge IGBT (QA, QB, QC, QD)							
Off Characteristics							
BV_{CES}	Collector-Emitter Breakdown Voltage	$V_{GE} = 0\text{ V}, I_C = 1\text{ mA}$	650	-	-	V	
I_{CES}	Collector Cut-off Current	$V_{CE} = V_{CES}, V_{GE} = 0\text{ V}$	-	-	250	μA	
I_{GES}	Gate-Emitter Leakage Current	$V_{GE} = V_{GES}, V_{CE} = 0\text{ V}$	-	-	± 2	μA	
On Characteristics							
$V_{GE(th)}$	Gate-Emitter Threshold Voltage	$V_{GE} = V_{CE}, I_C = 40\text{ mA}$	3.0	5.2	6.1	V	
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 40\text{ A}, V_{GE} = 15\text{ V}$	-	1.6	2.3	V	
		$I_C = 40\text{ A}, V_{GE} = 15\text{ V}, T_C = 125\text{ }^\circ\text{C}$	-	1.8	-	V	
R_{LEAD}	Lead Resistance of Pin to Chip	per Chip	-	3.5	-	$\text{m}\Omega$	
Switching Characteristics (QB-QAD / QD-QCD)							
$t_{d(on)}$	Turn-On Delay Time	$V_{CC} = 300\text{ V}$ $I_C = 40\text{ A}$ $V_{GE} = 15\text{ V}$ $R_G = 15\text{ }\Omega$ Inductive Load $T_C = 25\text{ }^\circ\text{C}$	-	26	-	ns	
t_r	Rise Time		-	22	-	ns	
$t_{d(off)}$	Turn-Off Delay Time		-	125	-	ns	
t_f	Fall Time		-	14	-	ns	
E_{ON}	Turn-On Switching Loss per Pulse		-	0.45	-	mJ	
E_{OFF}	Turn-Off Switching Loss per Pulse		-	0.27	-	mJ	
$t_{d(on)}$	Turn-On Delay Time		$V_{CC} = 300\text{ V}$ $I_C = 40\text{ A}$ $V_{GE} = 15\text{ V}$ $R_G = 15\text{ }\Omega$ Inductive Load $T_C = 125\text{ }^\circ\text{C}$	-	24	-	ns
t_r	Rise Time			-	25	-	ns
$t_{d(off)}$	Turn-Off Delay Time			-	139	-	ns
t_f	Fall Time			-	13	-	ns
E_{ON}	Turn-On Switching Loss per Pulse	-		0.74	-	mJ	
E_{OFF}	Turn-Off Switching Loss per Pulse	-		0.35	-	mJ	
Q_g	Total Gate Charge	$V_{CC} = 300\text{ V}, I_C = 40\text{ A}, V_{GE} = 15\text{ V}$	-	60	-	nC	
$R_{\theta JC}$	Thermal Resistance of Junction to Case	per Chip	-	-	0.95	$^\circ\text{C/W}$	
$R_{\theta CH}$	Thermal Resistance of Case to Heat sink	per Chip, $\lambda_{PCM} = 3.4\text{ W/mK}$	-	0.64	-	$^\circ\text{C/W}$	
H-bridge FWD (QAD, QBD, QCD, QDD)							
V_F	Diode Forward Voltage	$I_F = 30\text{ A}$	-	2.45	3.2	V	
		$I_F = 30\text{ A}, T_C = 125\text{ }^\circ\text{C}$	-	2.15	-	V	
I_R	Reverse Leakage Current	$V_R = 650\text{ V}$	-	-	250	μA	
I_{rr}	Reverse Recovery Current	$V_R = 300\text{ V}, I_F = 30\text{ A},$ $di/dt = 1570\text{ A/us},$ $T_C = 25\text{ }^\circ\text{C}$	-	20.1	-	A	
t_{rr}	Reverse Recovery Time		-	30	-	ns	
E_{rec}	Reverse Recovery Energy		-	27	-	μJ	
I_{rr}	Reverse Recovery Current	$V_R = 300\text{ V}, I_F = 30\text{ A},$ $di/dt = 1135\text{ A/us},$ $T_C = 125\text{ }^\circ\text{C}$	-	23.1	-	A	
t_{rr}	Reverse Recovery Time		-	52	-	ns	
E_{rec}	Reverse Recovery Energy		-	73	-	μJ	
$R_{\theta JC}$	Thermal Resistance of Junction to Case	per Chip	-	-	1.38	$^\circ\text{C/W}$	
$R_{\theta CH}$	Thermal Resistance of Case to Heat sink	per Chip, $\lambda_{PCM} = 3.4\text{ W/mK}$	-	0.45	-	$^\circ\text{C/W}$	
DC link Capacitor							
C value	Capacitance Value		-	47	-	nF	
NTC (Thermistor)							
R_{NTC}	Rated Resistance	$T_C = 25\text{ }^\circ\text{C}$	-	22	-	$\text{k}\Omega$	
		$T_C = 100\text{ }^\circ\text{C}$	-	1.486	-	$\text{k}\Omega$	
	Tolerance	$T_C = 25\text{ }^\circ\text{C}$	-5	-	+5	%	
P_D	Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	-	-	20	mW	
B_{Value}	B-Constance	$B_{25/50}, \text{tol.}$	-	3950	-	K	
		$B_{25/100}$	-	3998	-	K	

Typical Performance Characteristics

Fig 1. Forward Voltage Drop
- Bypass Diode

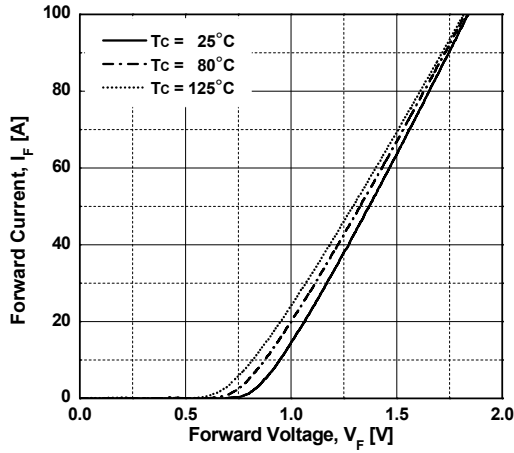


Fig 2. Transient Thermal Impedance
- Bypass Diode

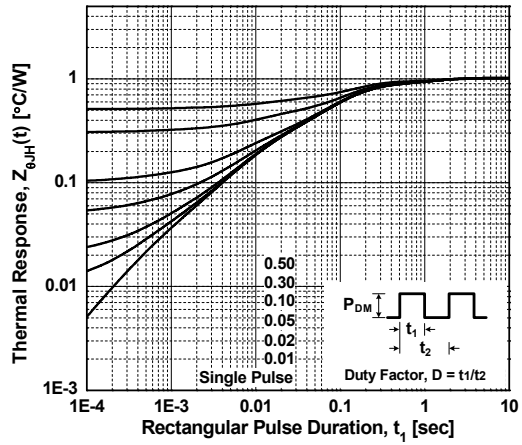


Fig 3. Forward Voltage Drop
- Boost Diode

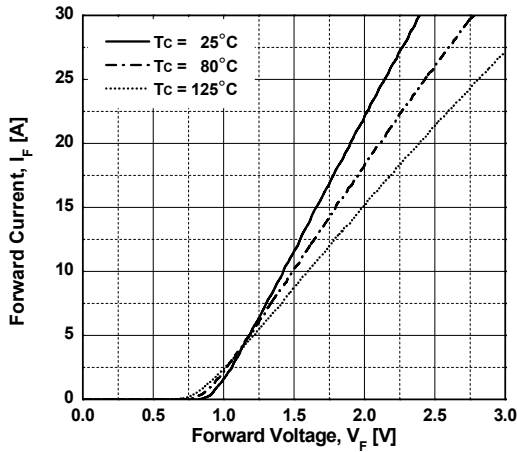


Fig 4. Transient Thermal Impedance
- Boost Diode

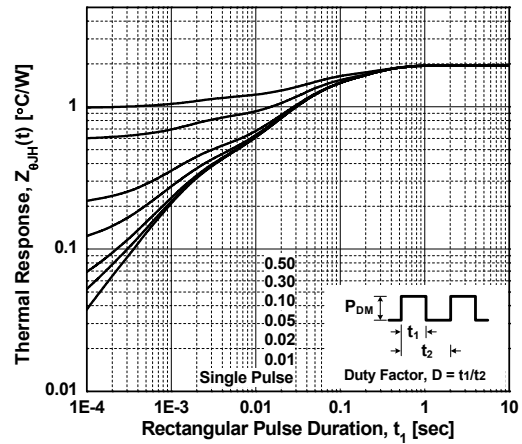


Fig 5. On-Region Characteristics
- Boost MOSFET

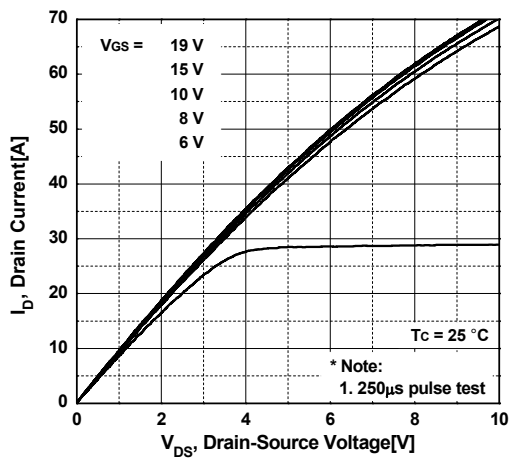
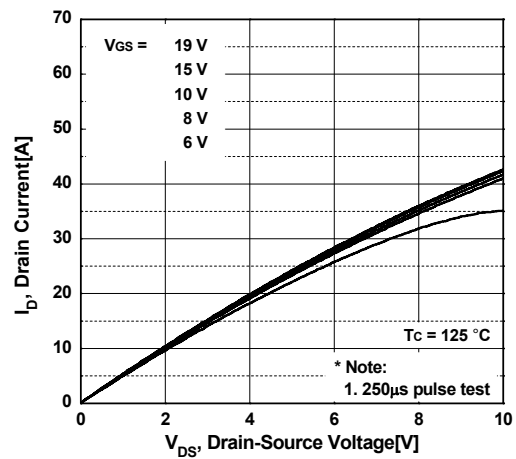


Fig 6. On-Region Characteristics
- Boost MOSFET



Typical Performance Characteristics

Fig 7. On-Resistance Variation vs. Temperature - Boost MOSFET

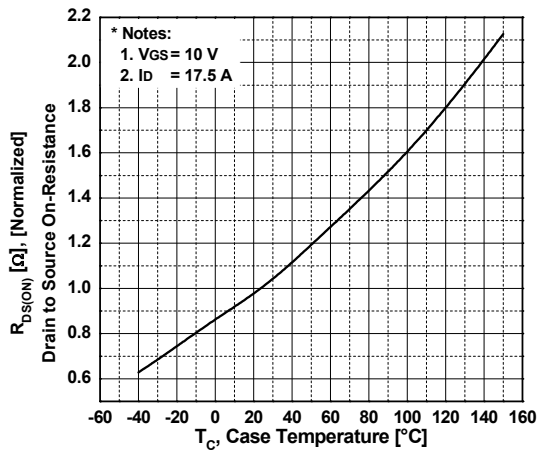


Fig 8. Switching Loss vs. Gate Resistor Values - Boost MOSFET

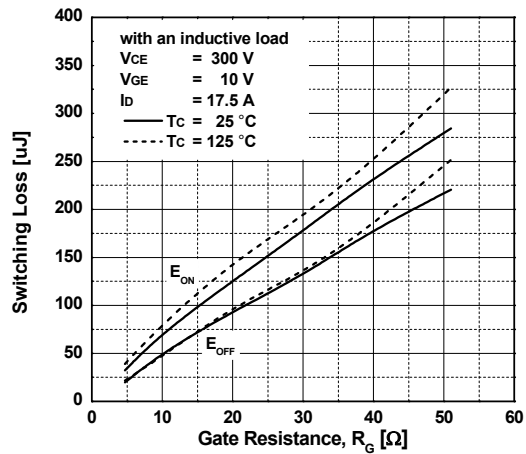


Fig 9. Switching Loss vs. Drain Current - Boost MOSFET

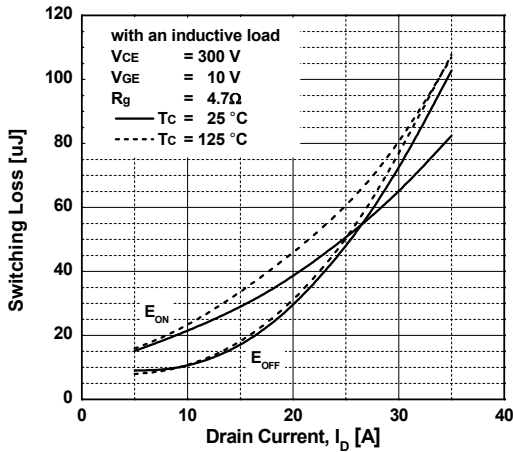


Fig 10. Body Diode Forward Voltage Variation vs. Source Current and Temperature - Boost MOSFET

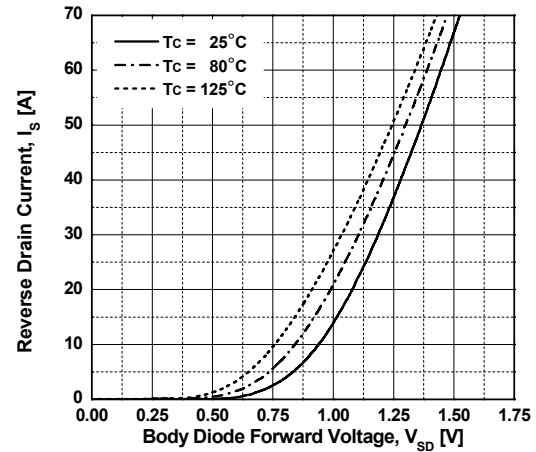


Fig 11. Transient Thermal Impedance - Boost MOSFET

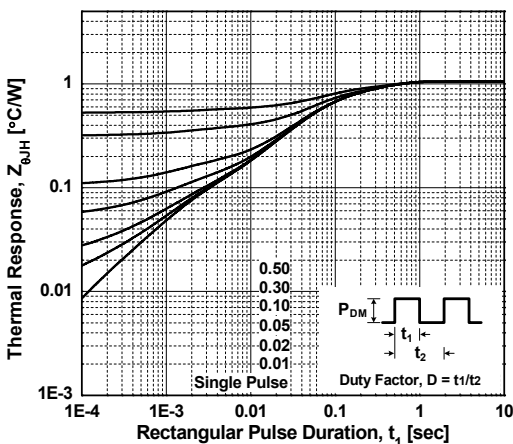
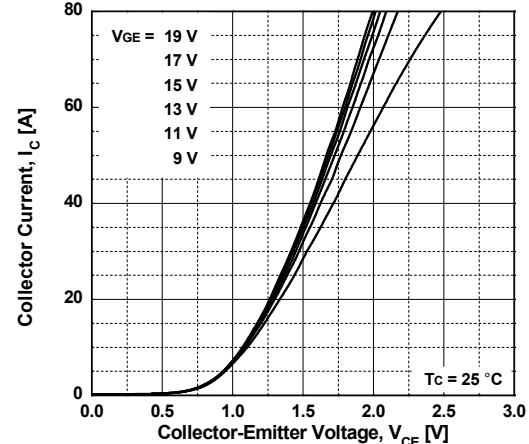


Fig 12. Output Characteristics - H-bridge IGBT



Typical Performance Characteristics

Fig 13. Output Characteristics
- H-bridge IGBT

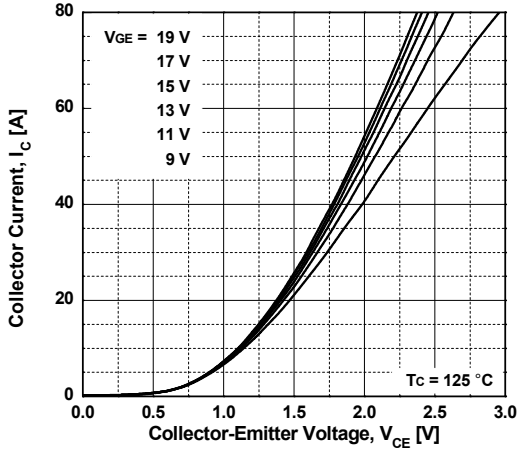


Fig 14. Saturation Voltage Characteristics
- H-bridge IGBT

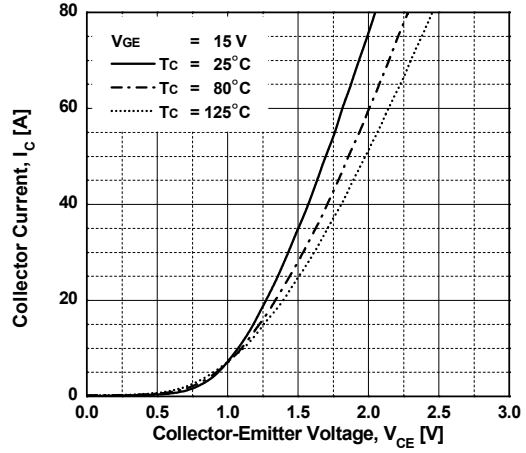


Fig 15. Switching Loss vs. Gate Resistor Values
- H-bridge IGBT

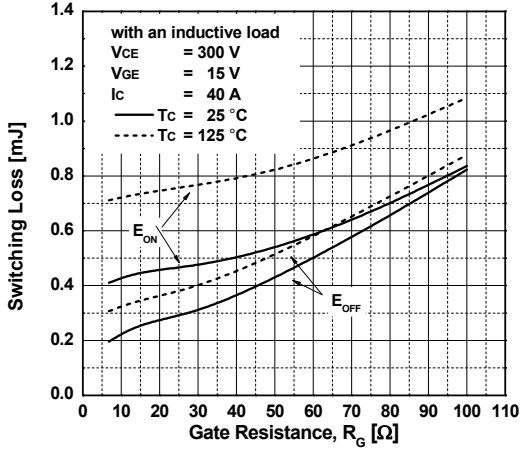


Fig 16. Switching Loss vs. Collector Current
- H-bridge IGBT

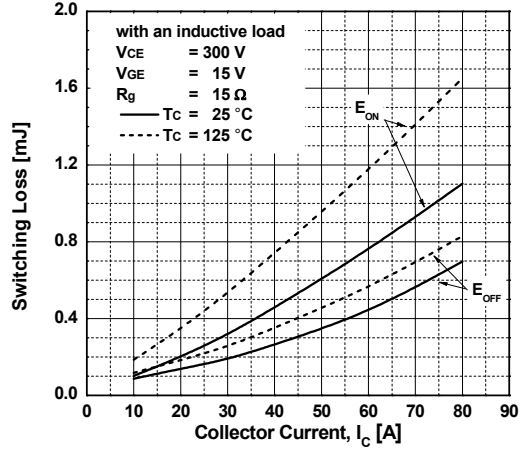


Fig 17. Transient Thermal Impedance
- H-bridge IGBT

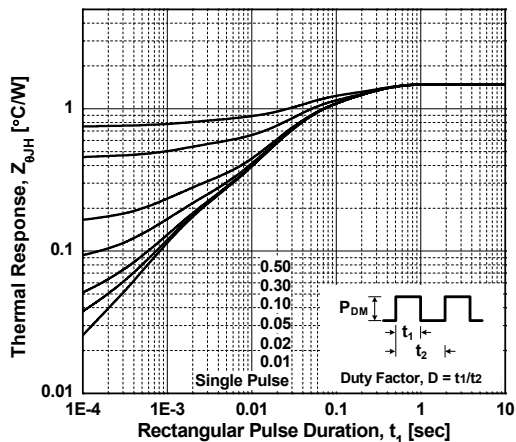
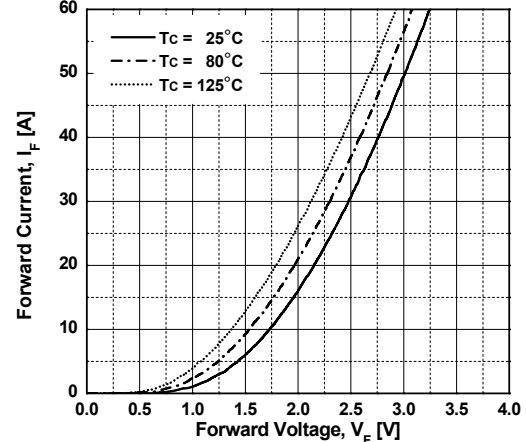


Fig 18. Forward Voltage Drop vs. Forward Current
- H-bridge FWD



Typical Performance Characteristics

Fig 19. Reverse Recovery Energy vs. Gate Resistor Values - H-bridge FWD

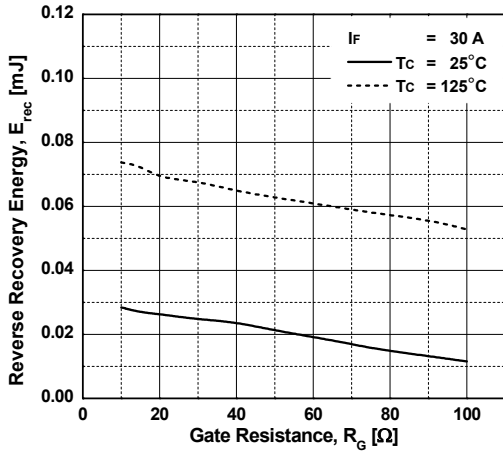


Fig 20. Reverse Recovery Energy vs. Forward Current - H-bridge FWD

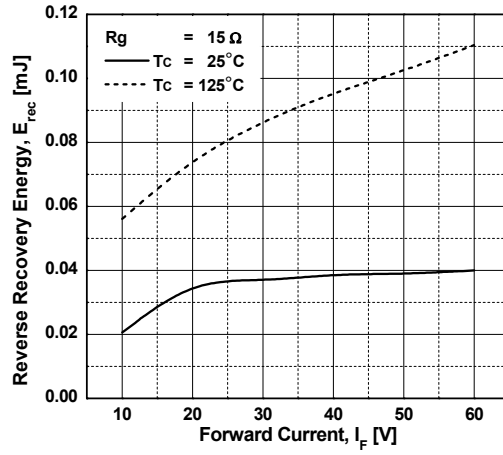
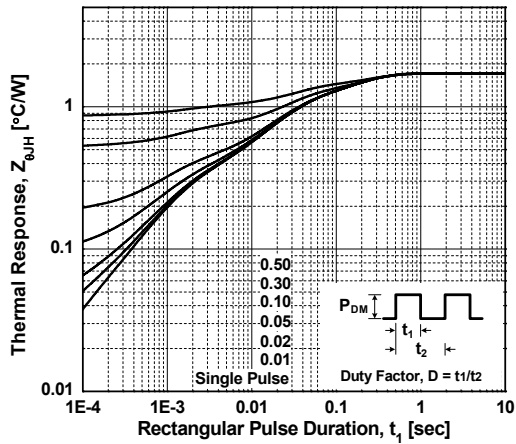
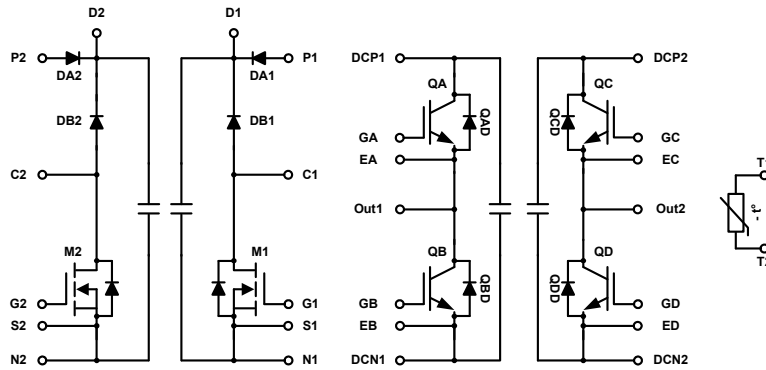


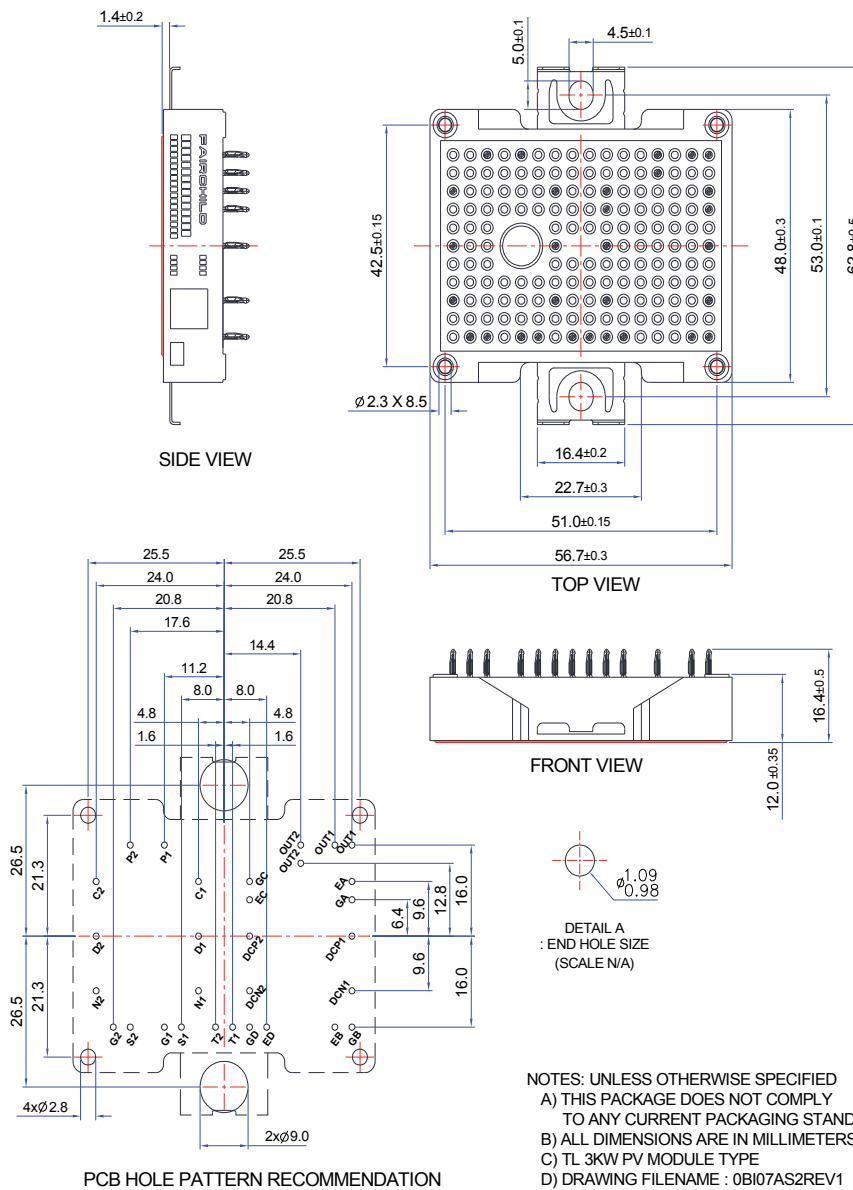
Fig 21. Transient Thermal Impedance - H-bridge FWD



Internal Circuit Diagram








Package Outlines [mm]





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