CRYSTAL OSCILLATOR

Low Profile / LOW-JITTER SPXO

SG - 210 S*D

- Frequency range : 50.000 MHz to 80.000 MHz
- Supply voltage : 1.8 V Typ. / 2.5 V Typ. / 3.3 V Typ.
- Current consumption : 7.0 mA Max.
  : (SDD 2.5 V No load condition 80 MHz)
- Function : Standby($\overline{ST}$)
- External dimensions : 2.5 × 2.0 × 0.8 t (mm) Typ.

Pb Free RoHS Compliant

Product Number (please contact us)
X1G0029x1xxxx00

Actual size

NEW

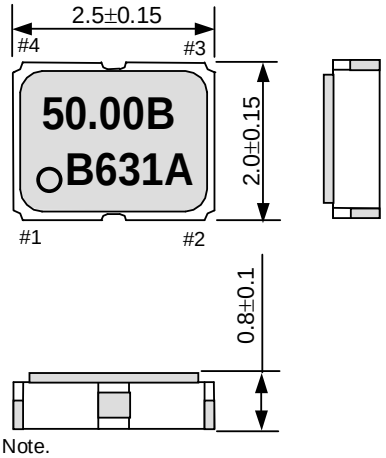
Specifications (characteristics)

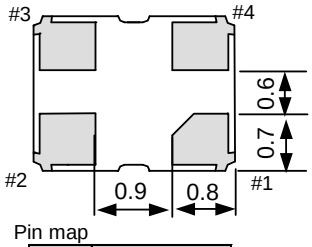
Item		Symbol	Specifications SG-210SED	SG-210SDD	SG-210SCD	Remarks
Output frequency range		f_0	50.000 MHz to 80.000 MHz			
Supply voltage		V_{CC}	1.8 V Typ. 1.6 V to 2.2 V	2.5 V Typ. 2.2 V to 3.0 V	3.3 V Typ. 2.7 V to 3.6 V	
Temperature range	Storage temperature	T_stg	-40 °C to +125 °C			Store as bare product after unpacking
	Operating temperature	T_use	-40 °C to +85 °C			
Frequency tolerance		f_tol	B: ±50 × 10^{-6}, C: ±100 × 10^{-6}			-20 °C to +70 °C
			L: ±50 × 10^{-6}, M: ±100 × 10^{-6}			-40 °C to +85 °C
Current consumption		I_{CC}	6.0 mA Max.	7.0 mA Max.	8.0 mA Max.	No load condition
Stand-by current		I_std	10.0 µA Max.			$\overline{ST}$ =GND
Symmetry		SYM	45 % to 55 %			50 % V_{CC} level,L_CMOS ≤ 30 pF
High output voltage		V_{OH}	V_{CC} -0.4 V Min.			I_{OH}=-8 mA(SCD,SDD), -4 mA(SED)
Low output voltage		V_{OL}	0.4 V Max.			I_{OL}= 8 mA(SCD,SDD), 4 mA(SED)
Output load condition (CMOS)		L_CMOS	30 pF Max.			
Output enable / disable input voltage		V_{IH}	70 % V_{CC} Min.			$\overline{ST}$ terminal
		V_{IL}	30 % V_{CC} Max.			
Rise time / Fall time		t_r / t_f	4 ns Max.			20 % V_{CC} to 80 % V_{CC} level, L_CMOS ≤ 30 pF
Start-up time		t_str	2 ms Max.			t=0 at 90 % V_{CC}
Jitter *1		t_{DJ}	0.5 ps Typ.			Deterministic Jitter
		t_{RJ}	3.0 ps Typ.			Random Jitter
		t_{RMS}	25 ps Typ.			Peak to Peak
Phase Jitter		t_{PJ}	1.0 ps Max.			Offset frequency: 12 kHz to 20 MHz
Frequency aging		f_aging	±3 × 10^{-6}/ year Max..			+25 °C, First year, V_{CC}= 1.8 V, 2.5 V, 3.3 V
			±10 × 10^{-6}/ 10 years Max.			+25 °C, 10 years, V_{CC}= 1.8 V, 2.5 V, 3.3 V

L_CMOS ≤ 15 pF

*1 Based on DTS-2075 Digital timing system made from WAVECREST with jitter analysis software VISI6.

External dimensions (Unit:mm)



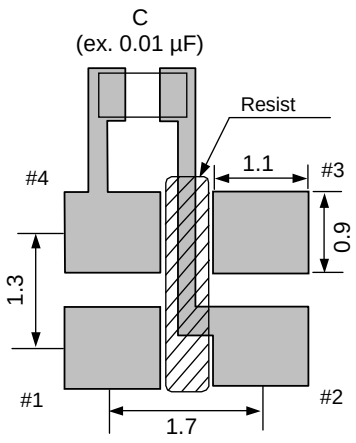


Pin map

Pin	Connection
1	$\overline{ST}$
2	GND
3	OUT
4	V_{CC}

Note.
$\overline{ST}$ pin = HIGH or "open" : Specified frequency output.
$\overline{ST}$ pin = LOW : Output is high impedance, oscillation stops.

Footprint (Recommended) (Unit:mm)



To maintain stable operation, provide by-pass capacitor with more than 0.1 µF at a location as near as possible to the power source terminal of the crystal products (between V_{CC} - GND).