HyperRAM™

DRAM Based Memory with HyperBus™ Interface

▶ Features:

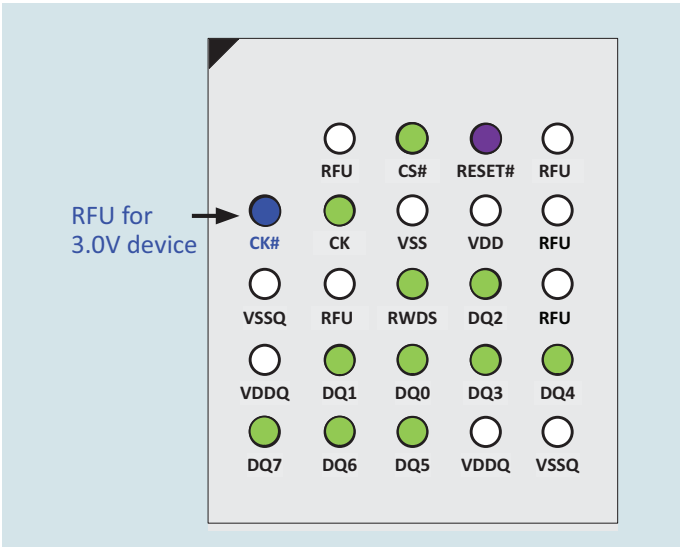
- Hidden Refresh operation
- Very Low Bus Signal Count :
  - 12 pins for 1.8V (with CK,CK#)
  - 11 pins for 3.0V (CK only)
- Max. Frequency :
  - 166MHz at VDD = 1.8V
  - 100MHz at VDD = 3.0V
- Low Power Consumption :
  - Burst Operation Current at 166MHz, 1.8V = 60mA (Max)
  - Standby Current @ 105°C, 1.8V = 300uA (Max)
  - Deep Power Down Current @ 105°C, 1.8V = 10uA (Max)

▶ Package:

- KGD/KTD
- 24-pin BGA

▶ HyperRAM™ Pin-Outs (In evaluation):

- 24-pin (5 x 5 ball array)
- PKG Body Size : 6 mm x 8 mm
- Ball Pitch : 1.0mm



▶ Densities:

- 64Mb (8Mb x 8) , 32Mb (4Mb x8),
- 128Mb (16Mb x8), 256Mb (32Mb x8)

▶ Availability:

- 64Mb
  - Production Now!
- 128Mb
  - Samples Available Now!
- 32Mb, 256Mb
  - Call Factory

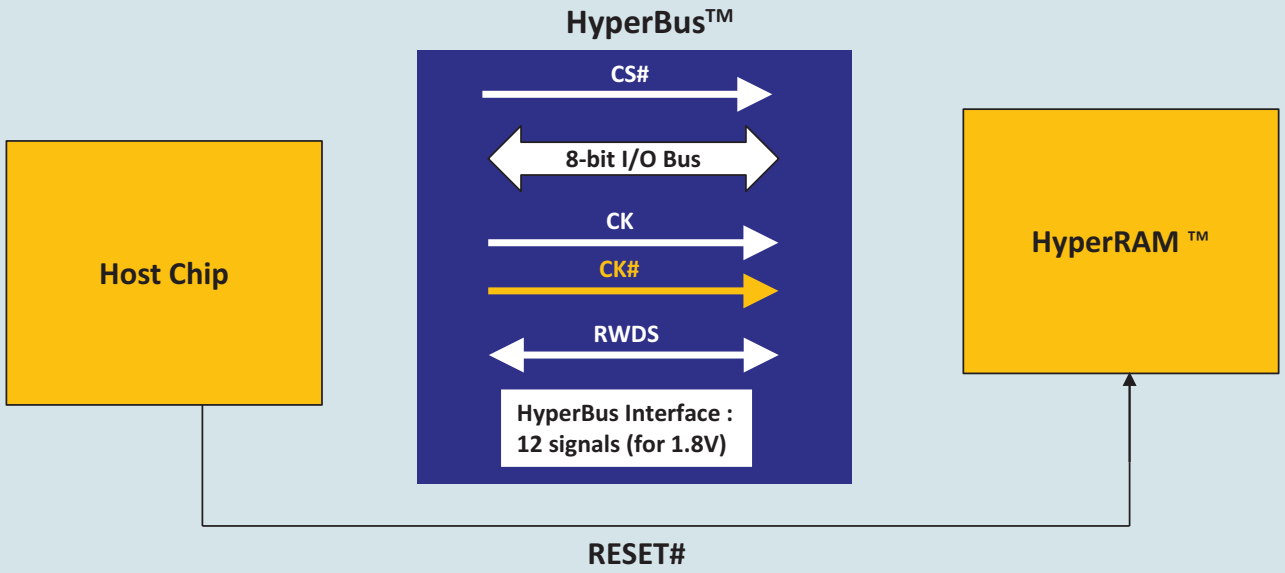
▶ Automotive Temperature Grades:

- Automotive, A1 (-40°C to 85°C)
- Automotive, A2 (-40°C to 105°C)

▶ Applications:

- Infotainment
- Advanced Driver Assistance Systems
- Smart Appliance
- Factory Automation
- Medical
- LED Projector
- D-SLR Camera
- Auto-Cluster

HyperRAM™ Interface



▶ Low Signal Pin Count for HyperBus™:

- 12 signals for 1.8V Device (with CK,CK#)
- 11 signals for 3.0V Device (with CK only)
- * RESET# is not included in the HyperBus™ signal.
- Differential Clock (CK,CK#) for 1.8V device & Single Ended Clock (CK only) for 3.0V device
- Up to 166MHz Double-Data-Rate (DDR) 8-bit I/O bus for high throughput : 333 MB/s bandwidth
- Read Write Data Strobe (RWDS) to:
  - Indicate Refresh Collision
  - Edge Aligned with Read Data for Read Operations
  - Byte mask for write operations
- Clocks (CK,CK#) are not required to be free-running