# PRM and VTM Parallel Operation

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## Introduction

This Application Note describes the steps needed to create a current sharing higher power array using two PRM-AL and VTM pairs in a parallel configuration. If the application requires more than two PRMs in parallel, please contact Applications Engineering for additional information.

## Connection Method

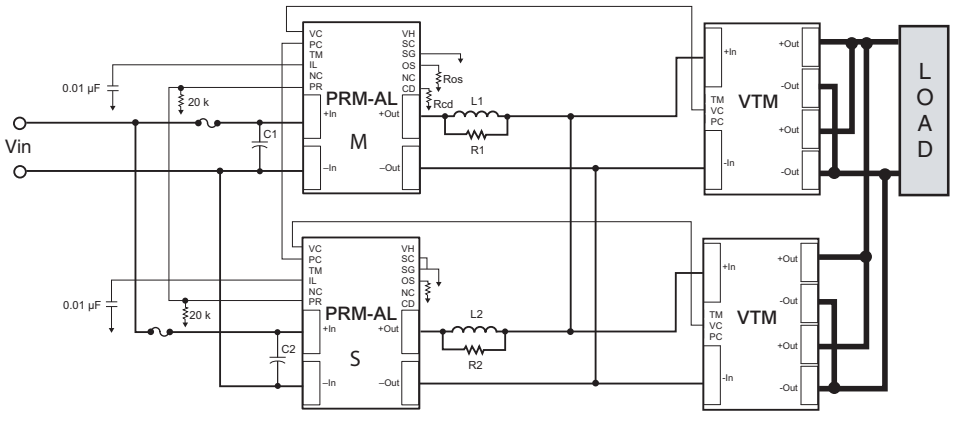
Placing two PRM-AL / VTM pairs in parallel to increase power and achieve current sharing is a relatively simple task:

1. Connect the + inputs of the PRMs together
2. Connect the – inputs of the PRMs together
3. Connect the + outputs of the VTMs together
4. Connect the – outputs of the VTMs together
5. Connect the PR pins of the PRMs together
6. Connect the PC pins of the PRMs together
7. Connect the SC pin to the SG pin of one PRM to configure it as a slave

The above steps are in addition to the general PRM / VTM interconnect and set-point configuration detailed in the PRM data sheet.

Schematically, this is shown in Figure 1.

*Figure 1*
*PRM / VTM interconnect schematic*




In this configuration there is no redundancy. Parallel operation for redundant applications, extreme dynamic loading, as well as higher order arrays and other power expanding techniques, are beyond the scope of this document and will be the subject of another Application Note.

## Precautions

Ensure there is no externally applied capacitance on the PR bus. It should be bypassed with a 10 kΩ equivalent impedance to Signal Ground (SG).

Under some loading or fault conditions, it may be possible for one pair to drive the factorized bus of the other pair due to the bi-directional nature of the VTMs. To prevent this "ORing" diodes should be employed on the inputs of the VTM to block reverse current flow. If the power dissipation of these diodes cannot be tolerated due to system constraints, placing the factorized bus of the pairs in parallel may be used as an alternative method as illustrated in the schematic.

A 2% minimum preload of total array capacity is required for proper operation.

## Reference

Traditional DC-DC converters regulate the output voltage to a set point by comparing a sample of the output voltage to an internal reference voltage, and adjusting either the switching frequency or pulse width to maintain regulation. These converters can operate as constant-current devices, or constant-power devices such that they will maintain voltage regulation up until either the current limit or power limit is reached. In the case of some constant-current devices, the voltage falls and current remains fixed when the limit has been exceeded.

When two voltage-regulated DC-DC converters are placed in a parallel configuration to increase power delivered, simply connecting the inputs together and the outputs together will not result in equal current share.

Each converter is sampling its output and comparing it to its reference to maintain the set-point voltage. One device will always have its voltage set point higher than another due to manufacturing variability and circuit impedance imbalance. With two devices operating in parallel as described, one will sense it has more voltage on its output and will sit "idle" because its regulation loop is satisfied.

The idle converter will not start to deliver current until the voltage on its output "droops" below its set point. Depending upon the circuit impedance, this may not occur until the converter that is delivering the current reaches its limit and its voltage falls. Eventually equilibrium will be reached; however, there will most likely not be a 50-50% current share. In this simple "droop-share" method, the sharing accuracy is best at full load and worst at light loads.

Purposely adding resistance and adjusting each converter to optimize the current-share accuracy can improve upon the droop-share method. This improvement, however, comes at the expense of having to tailor each configuration.

## Using VICs

V•I Chip topologies are unique and behave differently than the prior art. PRMs do not have the ability to source current once the current limit set point has been exceeded; they shut down and initiate a restart sequence. When configured in parallel, the possibility exists for one pair to come up, enter current limit, and shut down while the other pair is doing the same due to the inherent turn-on delays and asynchronous nature of the devices. This prevents them from being configured as traditional converters using the droop-share method. Connecting the PR pins and PC pins of the PRM overcomes this scenario and assures accurate current division between the pairs.

## PCB Construction

Please reference Application Note AN:005 "FPA Printed Circuit Board Layout Guidelines" for a detailed discussion on PCB layout.

## Test Vehicle

The array shown in Fig. 2 is constructed using the PRM-CB and VTM-CB customer evaluation boards. To order these boards, please go to:

vicorpower.com/evaluation_boards

The PRM customer boards have a 20 kΩ resistor from PR to SG so that if these are placed in parallel the equivalent bypass impedance is the desired 10 kΩ. If more than two PRM-CB boards are placed in parallel it will be necessary to change the 20 kΩ resistor to n•10 kΩ where "n" is the number of PRM-CB boards in the parallel array.

Each pair in this configuration has the ability to deliver 3 A at 36 V to the load, giving the array a 6 A rating. The nominal input to the array is 28 Vdc.

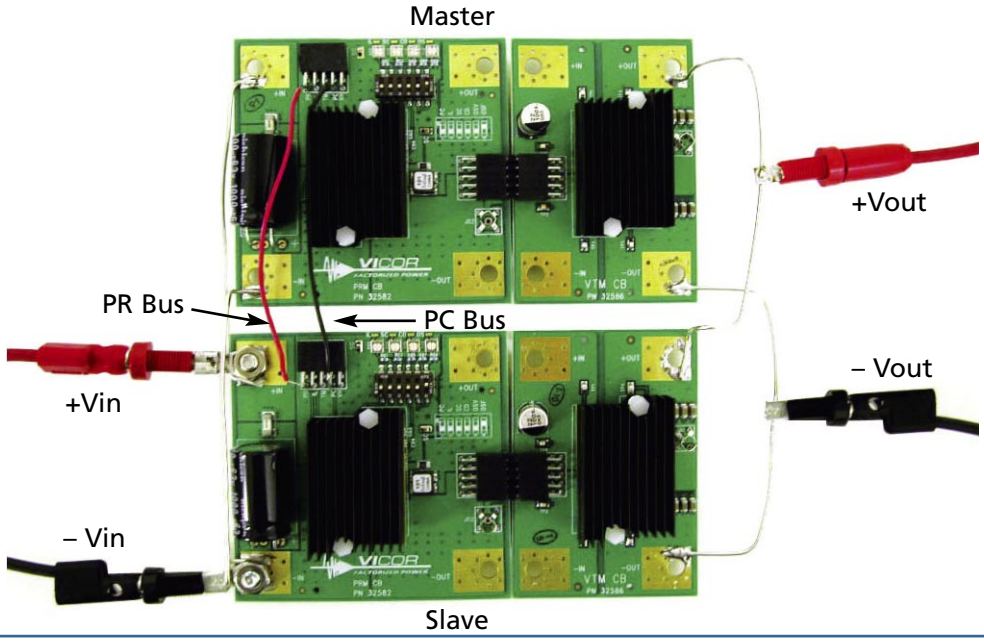
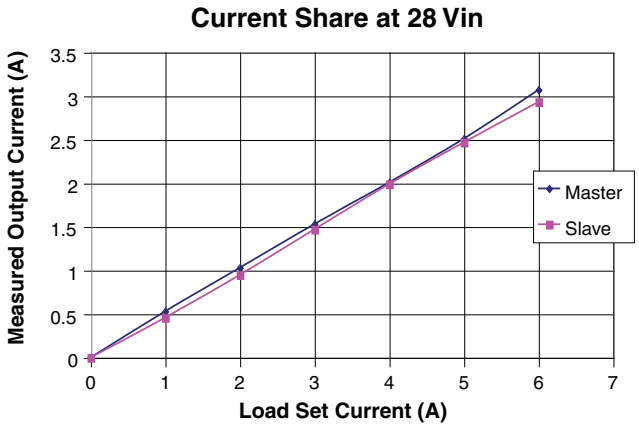



*Figure 2.*
*A pair of MP028F036M12AL-CB and MV036F360M003-CB boards are shown. The top pair is the master and the lower pair is the slave. The master was set for "Adaptive Loop" compensation.*

## Test Data

*Figure 3.*
*Current share at 28 Vin.*




The maximum output voltage deviation from no load to full load was 0.18 V or 0.49%. The measurement point for this was directly at the common connections to the load. The test data in Fig. 3 was taken with static load settings at 25°C, nominal line.

## Conclusion

Creating increased power capability by placing V•I Chips in parallel using the PR interface is a simple, straightforward task, ideal for most applications where high bandwidth / high slew rates are not required.