Innovative Power Device to Support Intermediate Bus Architecture Designs

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Abstract

For a majority of applications implemented today, the Intermediate Bus Architecture (IBA) has become the preferred power architecture. This power architecture has led to the development of the isolated, semi-regulated DC/DC converter known as the Intermediate Bus Converter (IBC). IBCs are an improvement to the standard regulated “Brick” DC/DC module, yet system requirements continue to evolve and are pushing the limits of these power devices. A new generation of IBC products, called Bus Converter Modules ™ (BCMs), has been developed to address these challenges.

1 Introduction

Since the development of the “brick” format DC/DC converter over 20 years ago, Distributed Power Architecture (DPA) designs have been the most common power architecture used for point of load regulation. Over the years, system requirements and increased competition have forced system designers to seek alternative solutions for their power devices in order to reduce cost and reduce physical board area. One of the latest power architectures developed to address these issues is the Intermediate Bus Architecture (IBA). IBA utilize one or more brick modules to provide the "upstream" isolation and create a lower “intermediate” bus voltage (typically 9.6V to 12V) that is then distributed to "downstream" non-isolated Point of Load (niPOL) regulators. The ability to replace many of the larger brick modules with smaller high efficiency niPOLs has led not only to lower component costs but also, in many cases improved overall system performance. Fig. 1 illustrates a typical Distributed Power Architecture and Intermediate Bus Architecture.

Early implementations of IBA used standard full, ½, and ¼ brick DC/DC converter modules. The main feature of an IBA is that it separates the DC/DC converter functions of isolation, transformation, and regulation and allocates them to two devices. In this configuration, the Intermediate bus voltage (the bus between the two devices) does not require tight regulation due to the fact that it will be post-regulated using niPOLs. The potential cost savings and efficiency gains achieved by designing a converter to be “loosely” or non-regulated directly led to the development of the Intermediate Bus Converter (IBC). Although IBCs are an improvement over the use of traditional "brick" converter modules power, size and efficiency demands have continued to escalate fueling the need for a new device adapted to these higher demands.

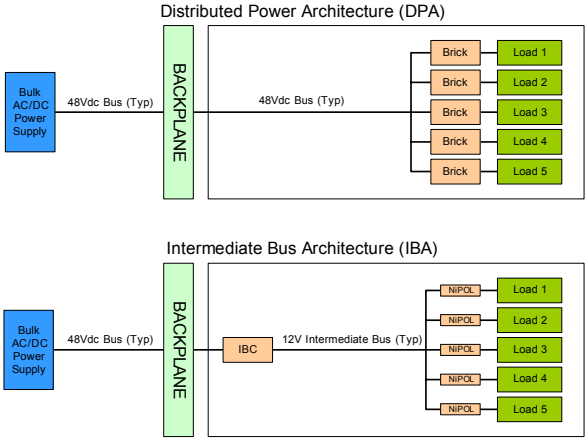

Fig. 1 DPA and IBA

To meet this challenge a power topology - known as the Sine Amplitude Converter (SAC) was developed. Bus Converter Modules (BCMs) employing SAC topology offer dramatic improvements in power density, noise reduction, and transient response over IBC products that are currently available. The BCM provides voltage transformation and isolation, and the niPOL converter provides the tight load regulation. High system efficiency is maintained because of the exceptionally high conversion efficiency of the BCM along with the reduced step down ratio required by the niPOL. Efficiency above 95% for the BCM is realized because the BCM does not regulate output voltage, it provides a fixed-ratio output. IBA systems use less board space than an isolated brick converter solution by eliminating multiple isolation barriers included in isolated converters.

2 Sine Amplitude Converter

A simplified schematic of a Sine Amplitude Converter is shown in Fig. 2. The power train is a low-charge (Q), high frequency, controlled oscillator with high spectral purity and common-mode symmetry - resulting in essentially noise-free operation. The control architecture locks the operating frequency to the power train resonant frequency, optimizing efficiency and minimizing

output impedance by effectively canceling reactive components. R_{OUT} (the output resistance of the BCM) can be as low as 0.8 milliohm from a single BCM. If that is not low enough, or if more power is required, BCMs can be paralleled with accurate current sharing. Quiet and powerful, the SAC-based BCM can be considered as a linear voltage / current converter with a flat output impedance up to about 1 MHz.

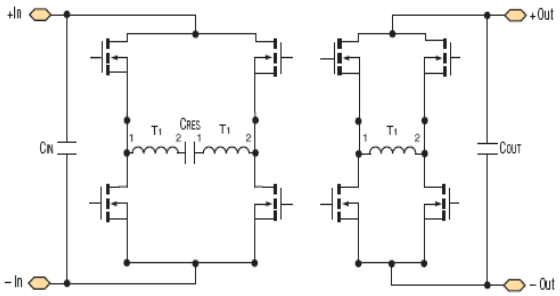

Fig. 2 Simplified schematic of the Sine Amplitude Converter

The secondary current in a BCM is basically a pure sinusoid. Selected BCM operating waveforms (Fig. 3) show the purity, low output impedance and fast response of a typical BCM. Please be aware the time scale in Figs. 4 and 5 is only 200 nanoseconds per division and that the waveform in Fig. 4 is with no external output capacitance across the load. The very low, non-inductive output impedance of the BCM allows an almost instantaneous response to the 100% step change in load current of Fig. 5. Because there is no internal regulation circuitry in a BCM, and none of the attendant loop delays or stability issues, no internal control action is required to respond to the change in load. The internal ASIC controller simply continues its function of controlling and synchronizing the operation of the switches to maintain operation at resonance.

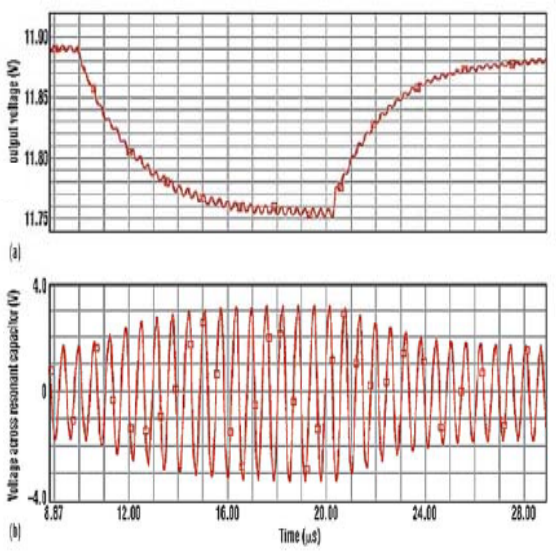

Fig. 3 Selected SAC BCM Waveforms

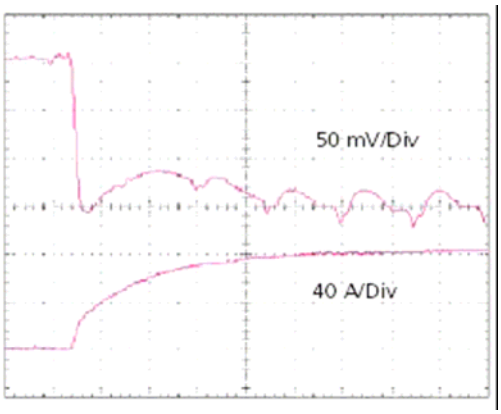

Fig. 4 BCM Dynamic Response - 0 – 80A Load step with NO output capacitance

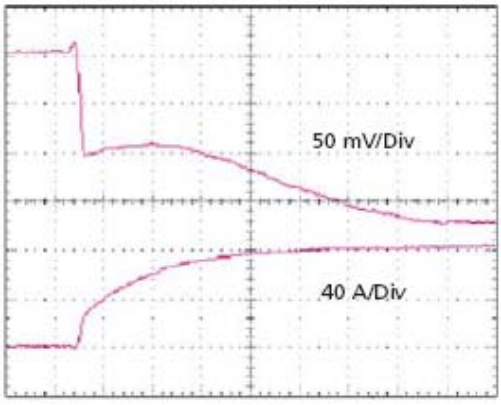

Fig. 5 BCM Dynamic Response - 0 – 80A Load step with 100µF output capacitance

3 Performance Comparison

The increase in performance over existing IBCs is directly related to the increased operating switching frequency and zero voltage/zero current switching process of the SAC topology. When compared to a typical 48V to 12V 300W ¼ brick IBC (Table 1), output power density increases from 13.2W/cm^3 to 63.6W/cm^3 and the required board area is reduced from 21.3 cm^2 to 7.2cm^2. In addition to being physically smaller than the current 1/8 brick IBC products available today, board space can be saved by using smaller input and output filtering components due to the higher switching frequency of the BCM. (Typical BCM switches at 3.4MHz versus IBCs that switch at 300kHz.) Another major advantage the SAC topology provides is capacitive multiplication and input source impedance division capability. This unique ability, exclusive to the SAC topology, provides additional cost and space saving advantages because it allows the system designer to reduce the number of differential capacitors required by the downstream niPOLs, while still maintaining the same system performance.

	Typical ¼ Brick IBC	**Typical BCM**
Input Voltage Range:	42-55Vdc	38-55Vdc
PRI to SEC Isolation:	2250Vdc	2250Vdc
Operating Efficiencies:	95% (typ. At full load)	95.6% (typ. At full load)
Switching Frequency:	300kHz (fixed)	3.4MHz (typ. 1.7MHz per phase)
Package size:	1.45" x 2.28" x 0.42" (36,8mm x 57,9mm x 10,7mm)	1.28" x 0.87" x 0.26" (32,5mm x 22,0mm x 6,6mm)
Typical Area Requirement for input Filter:	1.45" x 2.28" x 0.42" (36,8mm x 57,9mm x 10,7mm)	0.9843" x 0.4882" x 0.1773" (25,0mm x 12,4mm x 6,6mm)

Table 1 Comparing ¼ brick IBC to BCM

4 Capacitance Reduction

Faster transient response afforded by the SAC topology means that less energy storage is required for downstream devices. The BCM power train offers a unique capacitance multiplication feature. The effective output capacitance is 16x the input capacitance when a BCM with K of 1/4 is used. This means significantly less capacitance need be added downstream of the BCM. Since energy stored in a capacitor is:

$$E = \tfrac{1}{2} CV^2$$

a small amount of capacitance at the 48V input to the BCM has the same effect as the bulky capacitance typically added to the 12V input of the downstream niPOLs. This is also complemented by the lower input and output noise of SAC technology, resulting in a significant reduction in filtering.

To observe the effect of the BCM capacitance multiplication feature and dynamic performance, several niPOLs from different manufacturers were tested to compare the performance with their recommended capacitance versus the equivalent capacitance placed on the input of the BCM. Figs. 8 – 12 show typical results. Figs. 6 and 7 define the test configurations.

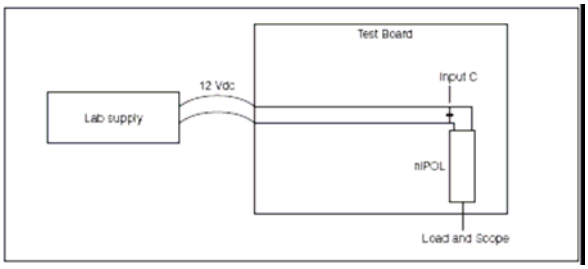

Fig. 6 Test set up 1 with niPOL and recommended input capacitance of 680µF.

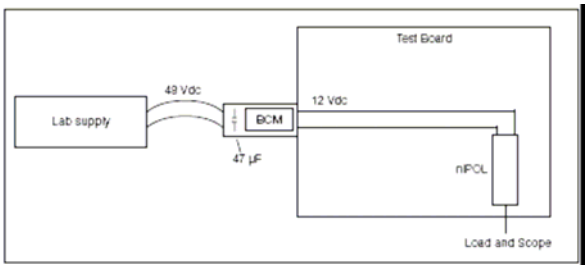

Fig. 7 Test set up 2 with BCM and 47µF of input capacitance.

Shown in the following figures are scope plots of the transient response and output ripple for a representative niPOL. The load step is from 10% to 90% of the rated current (1.5A to 13.5A) at a rate of 0.5A/µS. The output ripple measurement was taken with 330µF of output capacitance at full load (15A).

As can be observed from the figures, the transient response and output ripple of both systems are nearly identical. This demonstrates the manufacturer's recommended input capacitance for the niPOL can be replaced with significantly less capacitance at the BCM input without degradation of performance. Both set ups do have defined PCB trace impedance from the board edge to the niPOL. With the capacitance multiplication feature of the BCM, the 47µF of input capacitance is the equivalent of 752µF of output capacitance for a K of 1/4. In many applications, the PCB trace impedance to the niPOL can vary; therefore, it is necessary to evaluate the system with reduced capacitance. Greater trace impedance may require additional input capacitance at the input of the niPOL. The input capacitance of the niPOL can be replaced with the equivalent source impedance. This equivalent source impedance would consist of four parameters: the reduced input C, trace impedance, BCM output impedance, and BCM input capacitance reflected to the output.

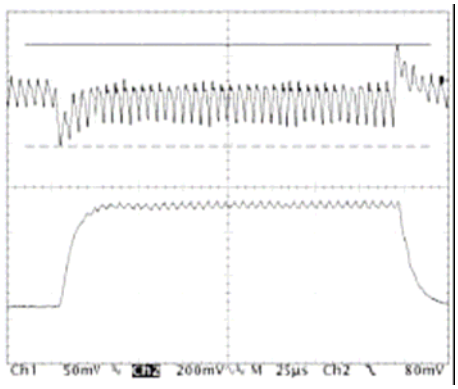

Fig. 8 Transient response in set up 1.Top waveform: niPOL output, Bottom waveform: load current.

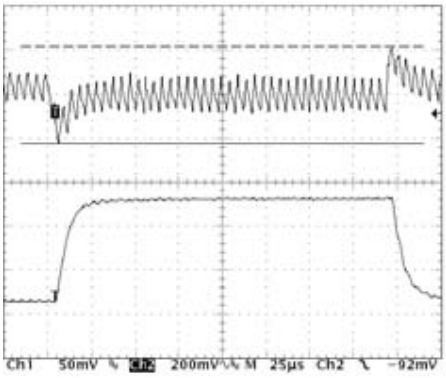

Fig. 9 Transient response in set up 2. Top waveform: niPOL output, Bottom waveform: load current.

5 Conclusion

Intermediate Bus Architecture incorporating Sine Amplitude Converter based BCMs and off-the-shelf niPOL converters can be an efficient and cost effective power solution. The high conversion frequencies and fast transient response of BCMs allow the system architect to take advantage of the capacitance multiplication feature. Any capacitance placed at the input to the BCM will be as effective as $1/K^2$ times this capacitance at the output of the BCM (input to the niPOLs) up to ~800 kHz. In some cases, it may be advantageous to add the input capacitance to the niPOL as well as capacitance on the input of the BCM so the combination of the two reflect the manufacturer's recommended capacitance. It is important to ensure that the output capacitance of the BCM does not exceed the maximum value listed on the BCM data sheet. Of course, as in any power system design with dynamic loads, layout and PCB trace impedances must be taken into consideration. Any trace inductance that is realized between the output of the BCM and the input of the niPOL will affect dynamic performance. It is especially important to keep the input impedance to the BCM as low as possible so it can respond quickly to changes in load current. The system architect needs to take into account the lowest BCM input voltage and the negative impedance of the niPOLs when determining the number of niPOLs a BCM can drive. This precaution is necessary to ensure that the BCM will not be in current limit during startup or low line conditions.

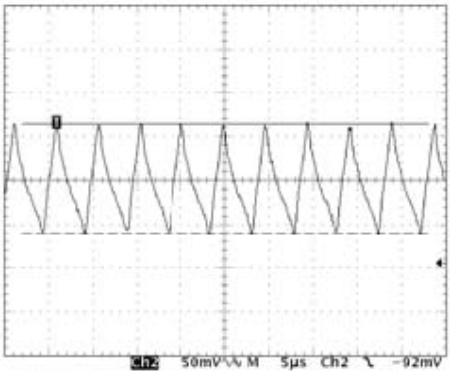

Fig. 10 Output ripple in set up 1with 330µF of niPOL output capacitance.

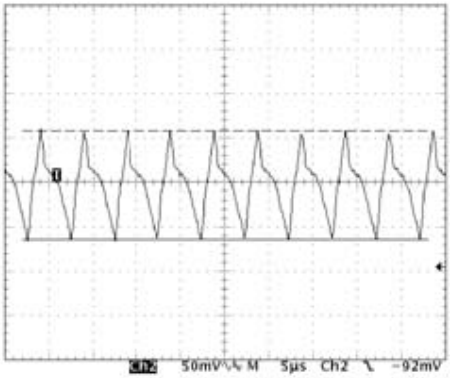

Fig. 11 Output ripple in set up 2 with 330µF of niPOL output capacitance.