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Optimized SiT15xx Drive Settings for 32 kHz Crystal Inputs of Low Power MCUs

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1 Introduction

Embedded microcontroller (MCU) based systems have historically relied on a low frequency 32.768 kHz quartz resonator driven oscillator for time keeping and failure recovery functions. TempFlat™ MEMS SiT153x oscillators and SiT155x temperature compensated oscillators (TCXOs) are a new generation of smaller footprint 32.768 devices that offer a cost effective, more reliable, improved frequency stability alternative to quartz-based 32.768 kHz oscillators.

This application note gives an overview of on-chip 32 kHz oscillator modes used in low power MCUs and the different drive settings supported by the SiT15xx families. The SiT15xx devices feature NanoDrive™, a factory programmable output voltage swing to optimize power and connectivity to existing oscillator sustaining circuits. This document lists valid combinations of SiT15xx output drive VOH/VOL settings and the associated part number for specific MCUs.
A list of SiT15xx drive settings optimized for each of the 32 kHz oscillator modes is provided for the following MCUs:

1. Energy Micro EFM32
2. Renesas Electronics RL78G13
3. STMicroelectronics STM32
4. Texas Instruments MSP430F2x
5. NXP LPC11xx
6. Freescale Kinetis L4x/L5x
7. Microchip PIC18

The programming details specific to each MCU are listed in individual Appendices at the end of this application note.

2 MCU 32 kHz Oscillator Operating Modes

Most energy efficient MCUs implement on-chip 32.768 kHz oscillators as a variant of a Pierce oscillator with either fixed or adjustable inverting gain stage as show in Figure 1.

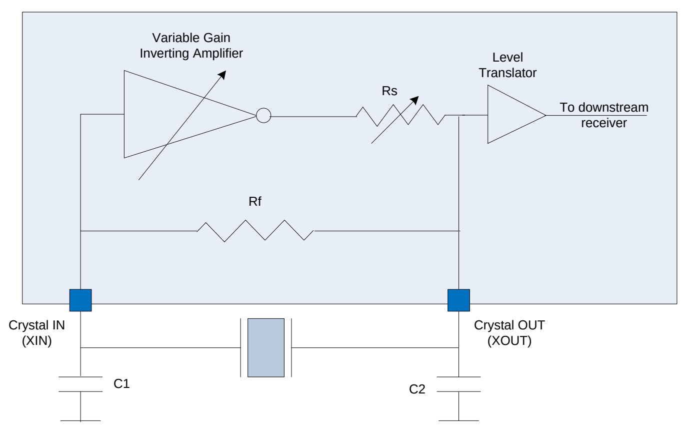
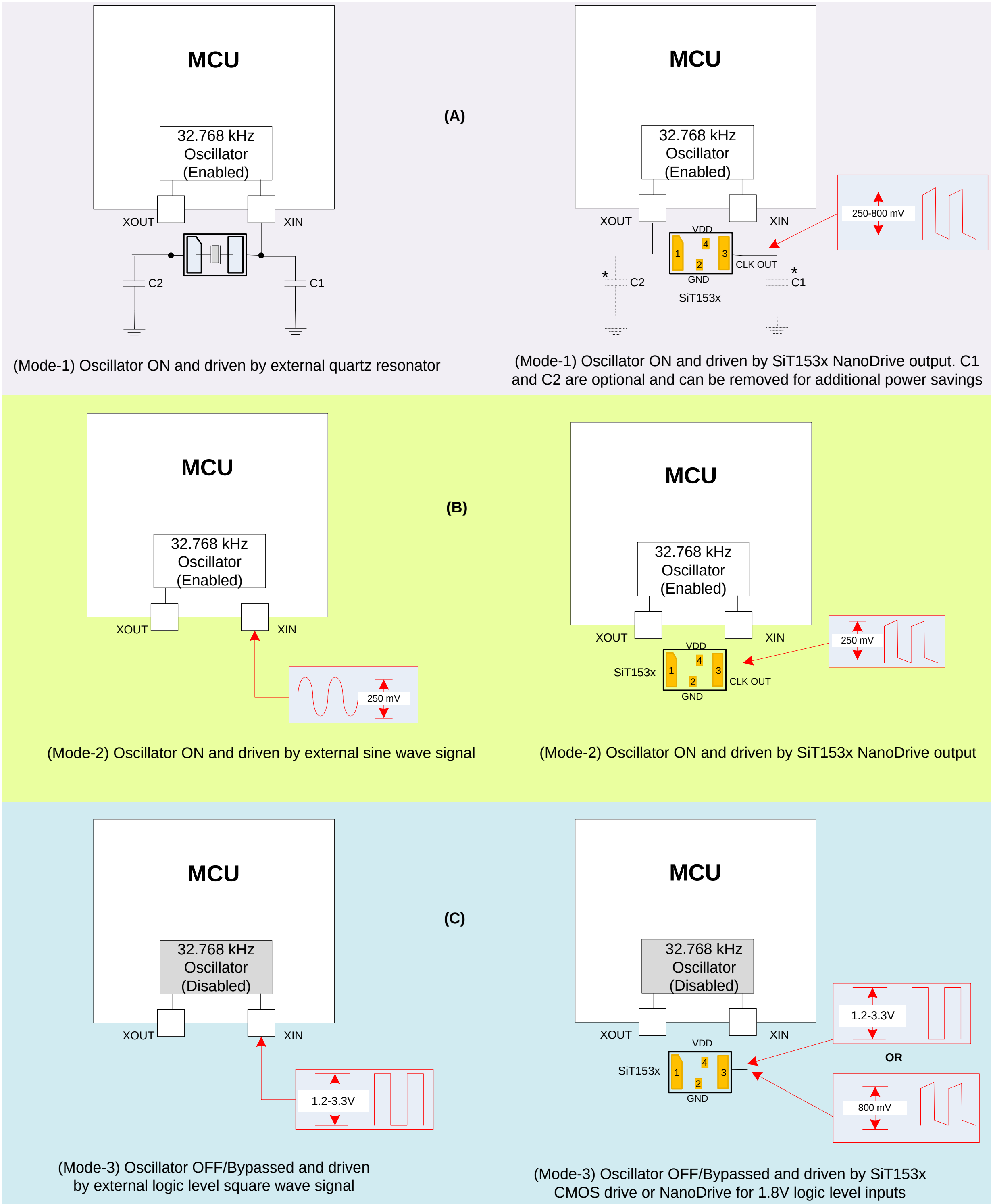


Figure 1: Typical 32.768 kHz oscillator block diagram shown with a crystal resonator.

This low frequency oscillator can be configured to operate in three distinct modes as shown in Figure 2.

1. Mode-1: Resonator only mode: drives a 32.768 kHz quartz resonator
2. Mode-2: Accept a sine wave input ≥200 mV_{pp} on XIN pin
3. Mode-3: Digital logic level clock input after bypassing or shutting off the on-chip oscillator. For oscillator inputs compatible to 1.8V logic levels, a smaller swing NanoDrive supported by the SiT15xx can be leveraged to save additional power.



* - C1 and C2 are optional and can be de-populated for additional power savings.

Figure 2: Operational modes of an MCU on-chip 32 kHz oscillator.

3 SiT15xx Output Drive Levels

The SiT15xx devices support two distinct output drive modes.

1. NanoDrive™ reduced swing, factory programmable
2. Rail-to-rail full-swing LVCMOS

3.1 NanoDrive Reduced Swing Mode

In NanoDrive mode, the SiT15xx output driver achieves various voltage swings and common-mode bias voltages similar to drive levels sustained by various implementations of a 32 kHz quartz crystal driven Pierce oscillator. Both DC coupled and AC coupled modes are supported.

DC coupled VOH/VOL drive levels shown in Table 1 are supported for 32 kHz oscillator circuits sensitive to DC bias and swing levels. The correct part number designator is shown inside each VOH/VOL combination in cell in Table 1. For example SiT15xxAI-H4-**D26**-32.768 will provide typical drive levels: VOH = 1.225V and VOL = 0.525V. The applicable oscillator operating modes for this setting is Mode-1 as illustrated in Figure 2.

Table 1: Matrix of Permitted DC Coupled VOH/VOL NanoDrive Levels

VOL\VOH	1.225	1.100	1.000	0.900	0.800	0.700	0.600
0.800	D28	D18	D08				
0.700	D27	D17	D07	D97			
0.525	D26	D16	D06	D96	D86		
0.500	D25	D15	D05	D95	D85	D75	
0.400		D14	D04	D94	D84	D74	D64
0.350		D13	D03	D93	D83	D73	D63

The supported AC coupled settings shown in Table 2 should be used with 32 kHz oscillator modes which are insensitive to DC bias levels, thus only the NanoDrive swing is relevant. The part number designator for each valid AC-swing level is shown below the valid swing option in Table 2. For example SiT15xxAI-H4-**AA4**-32.768 will provide a 400mV typical voltage swing. This AC coupled setting is most appropriate for oscillator Mode-2 as illustrated in Figure 2.

Table 2: Matrix of Permitted AC Coupled Swing Levels

Swing	0.800	0.700	0.600	0.500	0.400	0.300	0.250	0.200
Part# Output Code	AA8	AA7	AA6	AA5	AA4	AA3	AA2	AA1

The values listed in Tables 1 and 2 are typical numbers at 25°C and will exhibit a tolerance of +/- 55 mV across VDD and operating temperature range of -40 to 85°C.

Figure 3 shows a typical waveform output of a SiT15xx oscillator when programmed in NanoDrive mode: swing voltage, Vswing = 0.7 V, V_{OH} = 1.1V, V_{OL} = 0.4V in to a 15 pF load. The corresponding part number for a 2012 package 32.768 kHz device is SiT15xxAI-H4-**D14**-32.768.

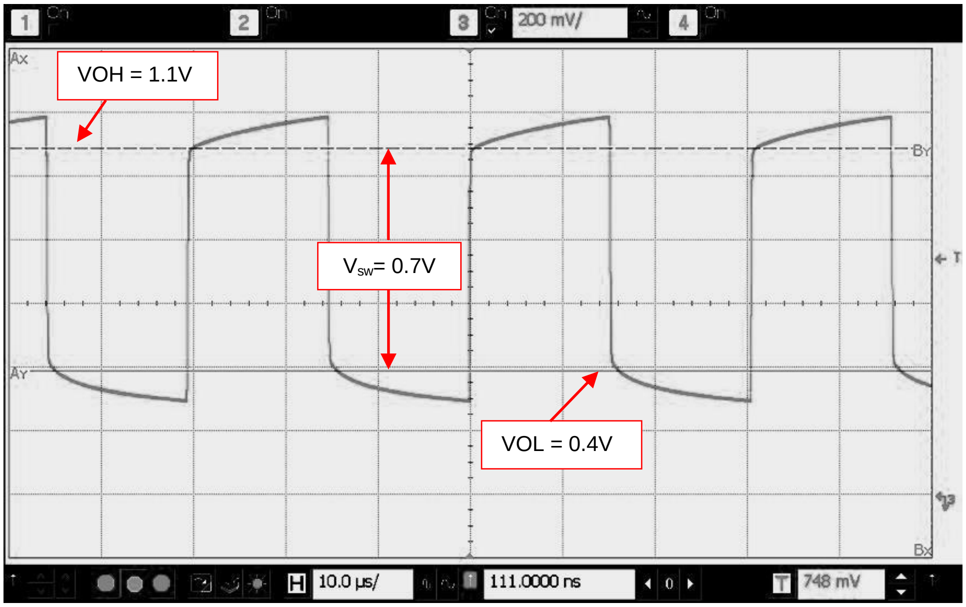


Figure 3: Scope capture of SiT15xxAI-H4-D14-32.768 output waveform in to a 15 pF load.

3.2 Full-Swing LVCMOS Drive

SiT15xx families can be programmed to generate full-swing LVCMOS levels. Figure 4 shows the waveform of SiT15xxAI-H4-DCC-32.768, 1.8V VDD at room temperature in to a 15 pF load.

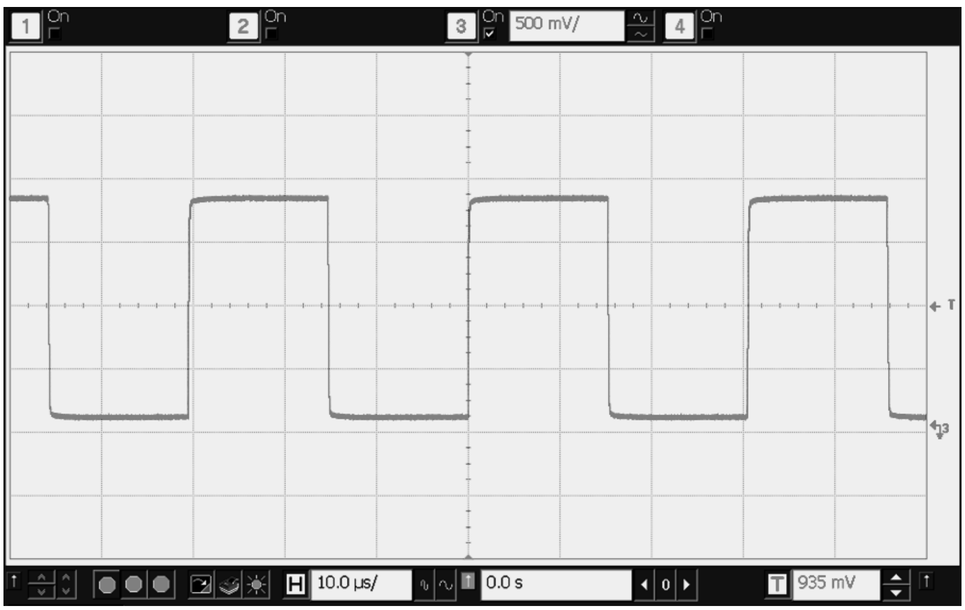


Figure 4: LVCMOS waveform of SiT15xxAI-H4-DCC-32.768 at 1.8V VDD in to 15 pf load.

LVCMOS level setting should be used if the NanoDrive settings do not achieve the expected results and best results, and lowest power, will be achieved when the on-chip oscillator has been bypassed or disabled as illustrated for oscillator Mode-3 in Figure 2.

4 Energy Micro EFM32

The EFM32 family of microcontrollers is based on the ARM Cortex-M0, M3 or M4 processor core targeted for low power operation. The EFM32 incorporates a low frequency crystal driven oscillator (LFXO) for clocking on-chip peripherals (including RTC) and potentially the CPU core. The LFXO can operate from a 32.768 kHz quartz crystal connected across the LFXTAL_N and LFXTAL_P pins or an external clock source on the LFXTAL_P pin.

By default the low frequency crystal oscillator (LFXO) is disabled. Table 3 lists the optimal settings of SiT15xx devices for each of the three operating modes of the LFXO oscillator.

Table 3: SiT15xx Configuration for the Three EFM32 LFXO Oscillator Modes

	Mode-1: LFXO Enabled	**Mode-2: LFXO Enabled with Sine Wave Input**	**Mode-3: LFXO Disabled**
LFXTAL_N, P connections	SiT15xx pin 3 → LFXTAL_N pin LFXTAL_P pin = NC	SiT15xx pin 3 → LFXTAL_N pin LFXTAL_P pin = NC	SiT15xx pin 3 → LFXTAL_P pin LFXTAL_N pin = NC
SiT15xx Output Drive Settings	NanoDrive: D74	NanoDrive: AA2	LVCMOS: DCC for MCU VDD ≥ 1.8V NanoDrive: D26 for MCU VDD = 1.8V (recommended for lowest power)

Appendix A provides details on how to enable, disable and program various operating modes of the EFM32 LFXO oscillator.

5 STMicroelectronics STM32

The STM32L152RBT6 is an ARM-based Cortex-M3 MCU. The internal RTC has a separate accurate low frequency (LSE) oscillator. The LSE oscillator has the advantage of providing a low power but highly accurate clock source for the real-time clock (RTC), peripheral clock/calendar or other timing functions. The oscillator incorporates OSC32_IN and OSC32_OUT pins for crystal connection. As an option, an external clock source can be routed directly to the OSC32_IN pin after bypassing the on-chip oscillator by settings the MCU registers. By default the LSE oscillator is switched off. Unlike the EFM32, the LSE oscillator supports two operating modes. Table 4 lists the optimal settings of SiT15xx for each of the two operating modes of the LSE oscillator.

Table 4: SiT15xx Configuration for the Two STM-32 LSE Oscillator Modes

	Mode-1: LSE Enabled	**Mode-2: LSE Enabled with Sine Wave Input**	**Mode-3: LSE Disabled**
OSC32_IN, OUT connections	SiT15xx pin-3 → OSC32_IN pin OSC_OUT pin = NC	Not Supported	SiT15xx pin 3 → OSC32_IN pin OSC_OUT pin = NC
SiT15xx Output Drive Settings	NanoDrive: D13	Not Applicable	LVCMOS: DCC for MCU VDD ≥1.8V NanoDrive: D26 for MCU VDD = 1.8V (recommended for lowest power)

Appendix B provides details on how to enable, disable and program various operating modes of the STM32 LSE oscillator.

6 Renesas Electronics RL78G13

The R5F100LE is a 16-bit MCU based on the RL78 core. The MCU includes a low frequency crystal oscillator (XT1) that can be used for clocking peripherals (including RTC) and the core if necessary. The XT1 clock oscillator has two pins for a crystal connection XT1 and XT2. The oscillation can be stopped by setting the XTSTOP bit (bit 6 of the clock operation status control register (CSC). An external CMOS level clock can also be supplied to the EXCLKS/XT2 pin.

Table 5 lists the optimal settings of SiT15xx for each of the three operating modes of the XT1 oscillator.

Table 5: SiT15xx Configuration for the Three XT1 Oscillator Modes

	Mode-1: LFXO Enabled	Mode-2: LFXO Enabled with Sine Wave Input	Mode-3: LFXO Disabled
XT1, XT2 Connection	SiT15xx pin 3 → XT1 pin XT2 pin = NC	Not Supported	SiT15xx pin 3 → XT2 pin XT1 pin = NC
SiT15xx Output Drive Settings	NanoDrive: D28	Not Applicable	LVCMOS: DCC for MCU VDD ≥ 1.8V NanoDrive: D26 for MCU VDD = 1.8V (recommended for lowest power)

Appendix C provides details on how to enable, disable and program various operating modes of the RL78G13 XT1 oscillator.

7 Texas Instruments MSP430F2x

MSP430 microcontrollers from Texas Instruments are based on a 16-bit RISC CPU. The architecture, combined with five different low-power modes is optimized to achieve extended battery life in portable applications. MSP430 MCUs include the basic clock module that supports low system cost and ultralow power consumption. The basic clock module includes low/high frequency oscillator that can be used with low-frequency watch crystals, resonators or external clock sources of 32768 Hz. The MCU has two XIN and XOUT pins for a crystal connection. Table 6 lists the optimal settings of SiT153x for each of the three operating modes of the XT1 oscillator.

Table 6: SiT153x Configuration for the Two LFXT Oscillator Modes

	Mode-1: LFXT Enabled	Mode-3: LFXT Disabled
XIN, XOUT connection	SiT153x pin 3 → XIN pin XOUT pin = NC	SiT153x pin 3 → XIN pin XOUT pin = NC
SiT153x Output Drive Settings	Not Applicable	LVCMOS: DCC

Appendix D provides details on how to enable, disable and program various operating modes of the MSP430 low frequency oscillator.

8 NXP LPC11xx

The LPC1100 MCUs are Cortex-M0 based MCUs running at speeds up to 50 MHz. The Cortex-M0 processor is an entry-level 32-bit ARM Cortex processor designed for a broad range of embedded applications. The MCU has several low power modes that enable to reach low power consumption with high performance in portable applications: Sleep Mode, Deep Sleep Mode, Power-Down Mode, and Deep Power-Down Mode.
The MCU incorporates the low power RTC oscillator providing 32768 Hz clock. Two pins RTCXIN and RTCXOUT are used for a connection of a 32768 Hz crystal. The RTC oscillator is always working despite the low power mode. The internal RTC oscillator cannot be bypassed. Table 7 lists the optimal settings of SiT153x for applicable operating mode of the XT1 oscillator.

Table 7: SiT153x Configuration for the RTC Oscillator Mode

	Mode-1: RTC Oscillator Enabled
RTCXIN, XOUT connection	SiT153x pin 3 → RTCXIN pin RTCXOUT pin = NC
SiT153x Output Drive Settings	NanoDrive: D13

Appendix E provides details on how to enable, disable and program various operating modes of the LPC1100 RTC oscillator.

9 Freescale Kinetis L4x/L5x

The Kinetis L series MCUs are based on ARM Cortex-M0+ processors. These processors feature low-power consumption in conjunction with high performance. The clock distribution system of the MCU includes Multipurpose Clock Generator (MCS), Crystal Oscillator (XOSC) and Real Time Clock (RTC) modules. A quartz crystal can be connected to the EXTAL32 and XTAL32 pins. If the XOSC is bypassed an external clock may be supplied to the EXTAL32 pin.

The XOSC incorporates tunable on-chip load capacitors, that are controlled by an user firmware. They exclude connecting external load capacitors to a crystal. Two oscillator modes of operation are available: high-gain and low-power configurations. The high gain configuration requires high voltage levels. Table below lists the optimal settings of the SiT153x for two operating modes of the XOSC oscillator.

Table 8: SiT15xx Configuration for the XOSC Oscillator Modes

	Mode-1: XOSC Enabled	**Mode-3: XOSC Bypassed**
XTAL32, EXTAL32 connection	SiT153x pin 3 → EXTAL32 pin XTAL32 pin = NC	SiT153x pin 3 → EXTAL32 pin XTAL32 pin = NC
SiT153x Output Drive Settings	NanoDrive: D28	LVCMOS: DCC

Appendix F provides details on how to enable, disable and program various operating modes of the KL04/05 oscillator.

10 Microchip PIC18

The PIC18 MCUs are low-power 8-bit devices that allow flexible clock customization and simple register access that enables designers to achieve low average power consumption in power-saving applications. The PIC18 devices include two oscillators. One is high-speed oscillator that operates in the MHz frequency range. The second oscillator operates in low-power low frequency using Timer1 and continues to operate while the core and other peripherals are in power-saving mode.

The secondary oscillator includes two T1OSI and T1OSO pins for connecting an external clock source. The table below shows two possible modes when using SiT153x devices as a clock source. To achieve the lowest power consumption SiTime recommends using the bypass mode (Mode-3). This eliminates additional current consumed by the on-chip secondary oscillator circuit.

Table 9: SiT15xx Configuration for the Secondary Oscillator Modes

	Mode-1: Secondary Oscillator Enabled	**Mode-3: Secondary Oscillator Bypassed**
T1OSI, T1OSO connection	SiT153x pin 3 → T1OSI pin T1OSO pin = NC	SiT153x pin 3 → T1OSO pin T1OSI pin = NC
SiT153x Output Drive Settings	NanoDrive: D13	LVCMOS: DCC

Appendix G provides details on how to enable, disable and program various operating modes of Secondary Oscillator.

11 Appendix A: Programming the EnergyMicro EFM32 LFXO

11.1 EFM32 Clock Management Unit

All on-chip oscillators are controlled by a Clock Management Unit (CMU). The CMU provides the capability to configure and turn on/off the clock on an individual basis to all peripheral modules. It is possible to connect an external clock source to LFXTAL_N pin of the LFXO. By configuring the LFXOMODE field in CMU_CTRL[12:11], the LFXO can be bypassed.

Table 10: CMU_CTRL - CMU Control Register

Offset	Bit Position																															
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset									0	0x0			0x3		0				1	0x0		0x3			0	0x1			0x3		0x0	
Access									RW	RW			RW		RW				RW	RW		RW			RW	RW			RW		RW	
Name									CLKOUTSEL1	CLKOUTSEL0			LFXOTMEOUT		LFXOBUFCUR				LFXOBOOST	LFXOMODE		HFXOTMEOUT		HFXOGLITCHDETEN		HFXOBUFCUR			HFXOBOOST		HFXOMODE	

Table 11: The LFXOMODE Field

Value	Mode	Description
0	XTAL	32.768 kHz crystal oscillator
1	BUFEXTCLK	An AC coupled buffer is coupled in series with LFXTAL_N pin, suitable for external sinus wave (32.768 kHz)
2	DIGEXTCLK	Digital external clock on LFXTAL_N pin. Oscillator is effectively bypassed.

To bypass the on-chip oscillator write '0x2' to the LFXOMODE[12:11] field.

The oscillator setting takes effect when 1 is written to LFXOEN in CMU_OSCENCMD.
The oscillator setting is reset to default when 1 is written to LFXODIS in CMU_OSCENCMD.

Table 12: CMU_OSCENCMD - Oscillator Enable/Disable Command Register

Offset	Bit Position																															
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																							0	0	0	0	0	0	0	0	1	1
Access																							W1	W1	W1	W1	W1	W1	W1	W1	W1	W1
Name																							LFXODIS	LFXOEN	LFRCODIS	LFRCOEN	AUXHFRCO DIS	AUXHFRCO EN	HFXODIS	HFXOEN	HFRCODIS	HFRCOEN

Table 13: OSCENCMD - The [31:3] Field Descriptions

Bit	Name	Reset	Access	Description
31:10	*Reserved*	*To ensure compatibility with future devices, always write bits to 0.*		
9	LFXODIS Disables the LFXO. LFXOEN has higher priority if written simultaneously.	0	W1	**LFXO Disable**
8	LFXOEN Enables the LFXO.	0	W1	**LFXO Enable**
7	LFRCODIS Disables the LFRCO. LFRCOEN has higher priority if written simultaneously.	0	W1	**LFRCO Disable**
6	LFRCOEN Enables the LFRCO.	0	W1	**LFRCO Enable**
5	AUXHFRCODIS Disables the AUXHFRCO. AUXHFRCOEN has higher priority if written simultaneously. Warning: Do not disable this clock during a flash erase/write operation.	0	W1	**AUXHFRCO Disable**
4	AUXHFRCOEN Enables the AUXHFRCO.	0	W1	**AUXHFRCO Enable**
3	HFXODIS Disables the HFXO. HFXOEN has higher priority if written simultaneously. Do not disable the HFRXO if this oscillator is selected as the source for HFCLK.	0	W1	**HFXO Disable**

Table 14: CMU_STATUS - Status Register

Offset	Bit Position																															
0x02C	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset																		0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
Access																		R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Name																		CALBSY	LFXOSEL	LFRCOSEL	HFXOSEL	HFRCOSEL	LFXORDY	LFXOENS	LFRCORDY	LFRCOENS	AUXHFRCO RDY	AUXHFRCO ENS	HFXORDY	HFXOENS	HFRCORDY	HFRCOENS

Table 15: CMU_STATUS - The [14:8] Field Descriptions

Bit	Name	Reset	Access	Description
31:15	*Reserved*	*To ensure compatibility with future devices, always write bits to 0.*		
14	CALBSY Calibration is on-going	0	R	**Calibration Busy**
13	LFXOSEL LFXO is selected as HFCLK clock source	0	R	**LFXO Selected**
12	LFRCOSEL LFRCO is selected as HFCLK clock source	0	R	**LFRCO Selected**
11	HFXOSEL HFXO is selected as HFCLK clock source	0	R	**HFXO Selected**
10	HFRCOSEL HFRCO is selected as HFCLK clock source	1	R	**HFRCO Selected**
9	LFXORDY LFXO is enabled and start-up time has exceeded	0	R	**LFXO Ready**
8	LFXOENS LFXO is enabled	0	R	**LFXO Enable Status**

11.2 Configuring the LFXO

Below is a code snippet of LFXO configuration from IAR Embedded Workbench IDE:

1. Enable the LFXO oscillator by setting the LFXOEN bit in the CMU_OSCENCMD[8]
2. Wait until the LFXORDY bit in the CMU_STATUS[9] is set. Applicable only for the XTAL mode, otherwise skip this step

```
CMU->CTRL &= ~(0x3 << 11);
CMU->CTRL   |= 0x00000000;    // (XTAL)32768 Hz crystal oscillator
//CMU->CTRL |= 0x00000800;    // (BUFEXTCLK)AC coupled
//CMU->CTRL |= 0x00001000;    // (DIGEXTCLK)an external clock source

// Lock CMU_CTRL
CMU->OSCENCMD = (0x1UL << 8);

/* Wait for clock to stabilize if requested
!!!Applicable only for crystal oscillator configuration!!! */
if (wait)
{
   while (!(CMU->STATUS & (0x1 << 9)));
}
```

The LFXO is able to operate from external clock sources with small signal amplitude (100mV and above). This mode (AC mode - BUFEXTCLK) can be set by configuring the LFXMODE field in the CMU_CTRL[12:11] register (see Table 10).

12 Appendix B: Programming the STMicroelectronics STM32 LSE Oscillator

12.1 Low-speed External Clock Oscillator

The low-speed external (LSE) crystal oscillator can be switched on/off by setting/clearing the LSEON bit in the RCC_CSR[8] register.

Table 16: Control/Status Register (RCC_CSR)

31	30	29	28	27	26	25	24
LPWR RSTF	WWDG RSTF	IWDG RSTF	SFT RSTF	POR RSTF	PIN RSTF	OBLRSF	RMVF
rw	rw	rw	rw	rw	rw	rw	rw

23	22	21	20	19	18	17	16
RTC RST	RTC EN	Reserved				RTCSEL [1:0]	
rw	rw					rw	rw

15	14	13	12	11	10	9	8
Reserved			LSECSSD	LSECSSON	LSE BYP	LSERDY	LSEON
			r	rw	rw	r	rw

7	6	5	4	3	2	1	0
Reserved						LSI RDY	LSION
						r	rw

The LSERDY flag in the RCC_CSR[9] register indicates whether the LSE crystal is stable or not. At startup the LSE crystal output clock signal is not released until this bit is set by hardware. An interrupt can be generated if enabled in the RCC_CIR[8] (Table 17

).

Table 17: Clock Interrupt Register (RCC_CIR)

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
CSSC	LSECS SC	MSI RDYC	PLL RDYC	HSE RDYC	HSI RDYC	LSE RDYC	LSI RDYC
W	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8
Res	LSECS SIE	MSI RDYIE	PLL RDYIE	HSE RDYIE	HSI RDYIE	LSE RDYIE	LSI RDYIE
	rw	rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
CSSF	LSE RDYF	MSI RDYF	PLL RDYF	HSE RDYF	HSI RDYF	LSE RDYF	LSI RDYF
r	r	r	r	r	r	r	r

12.2 External Clock Source (LSE bypass)

It is possible to connect an external clock source to OSC32_IN pin of the LSE oscillator. This feature is selected by setting the LSEBYP and LSEON bits in the RCC_CSR (Table 16). The external clock signal (square, sine or triangle) with ~50% duty cycle has to drive the OSC32_IN pin while the OSC32_OUT pin should be left unconnected (Hi-Z).

12.3 Clock Security System on LSE

The clock security system on the LSE oscillator can be activated by software writing the LSECSSON in the RCC_CSR register (Table 16). This bit can be disabled only by a hardware reset or RTC software reset, or after a failure detection on the LSE oscillator. LSECSSON must be written after LSE and LSI are enabled (LSEON and LSION enabled) and ready (LSERDY and LSIRDY set by hardware), and after the RTC clock has been selected by RTCSEL. The CSS on LSE is working in all modes: Run, Sleep, Stop and Standby.

If a failure is detected on the external 32 kHz oscillator, the LSE clock is no longer supplied to the RTC but no hardware action is made to the registers. In Standby mode a wakeup is generated. In other modes an interrupt can be sent to wake up. The software MUST then disable the LSECSSON bit, stop the defective 32 kHz oscillator (disabling LSEON), and can change the RTC clock source (no clock or LSI or HSE, with RTCSEL), or take any required action to secure the application.

12.4 Clock-out Capability

The microcontroller clock output (MCO) capability allows the clock to be output onto the external MCO pin (PA8) using a configurable prescaler (1, 2, 4, 8, or 16). The configuration registers of the corresponding GPIO port must be programmed in alternate function mode.

One of seven clock signals can be selected as the MCO clock:

- System clock (SYSCLK)
- Internal RC 16MHz (HSI) oscillator
- Internal 65 kHz to 4.2 MHz (MSI) oscillator
- External 1 to 24 MHz (HSE) oscillator
- PLL
- Internal low-power oscillator (LSI)
- Low-power 32.768 kHz external oscillator (LSE)

The selection is controlled by the MCOSEL[2:0] bits of the RCC_CFGR register (Table 18).

Table 18: Configuration Register (RCC_CFGR)

31	30	29	28	27	26	25	24
Res.	MCOPRE[2:0]			Res.	MCOSEL[2:0]		
	rw	rw	rw		rw	rw	rw
15	14	13	12	11	10	9	8
Reserved		PPRE2[2:0]			PPRE1[2:0]		
		rw	rw	rw	rw	rw	rw

23	22	21	20	19	18	17	16
PLLDIV[1:0]		PLLMUL[3:0]				Res.	PLL SRC
rw	rw	rw	rw	rw	rw		rw

15	14	13	12	11	10	9	8
Reserved		PPRE2[2:0]			PPRE1[2:0]		
		rw	rw	rw	rw	rw	rw

7	6	5	4	3	2	1	0
HPRE1[3:0]				SWS[1:0]		SW[1:0]	
rw	rw	rw	rw	rw	rw	rw	rw

Note: If the LSE or LSI is used as RTC clock source, the RTC continues to work in Stop and Standby low power modes, and can be used as wake-up source. However, when the HSE clock is used as RTC clock source, the RTC cannot be used in Stop and Standby low power modes.

12.5 Configuring LSE

1) Reset LSEON[8] and LSEBYP[10] bits in RCC_CSR before configuring the LSE.

IAR Embedded Workbench IDE example:

```
// #define RCC_LSE_OFF                      ((uint8_t)0x00)

/* Reset LSEON and LSEBYP bits before configuring the LSE --------*/
 *(__IO uint8_t *) CSR_BYTE2_ADDRESS = RCC_LSE_OFF;
```

2) Set the new LSE configuration. Set LSEBYP[10] bit if you need the bypass mode and set the LSEON bit. It can be performed simultaneously.

IAR Embedded Workbench IDE example:

```
// #define RCC_LSE_Bypass                   ((uint8_t)0x05)
// #define RCC_LSE_ON                       ((uint8_t)0x01)

/* Set the new LSE configuration ----------------------------------*/
 *(__IO uint8_t *) CSR_BYTE2_ADDRESS = RCC_LSE_ON;
// or *(__IO uint8_t *) CSR_BYTE2_ADDRESS = RCC_LSE_Bypass;
```

3) Wait untill the LSERDY[9] bit in RCC_CSR is ready. This is applicable when using an external crystal.

13 Appendix C: Programming the Renesas Electronics RL78G13 XT1 Oscillator

13.1 XT1 Oscillator

The XT1 oscillator is a circuit with low gain in order to achieve low-power consumption. There are AMPHS1[2], AMPHS0[1] fields in the CMC register (Table 21) that enables to choose optimal gain for a crystal.

Table 19: Oscillation Mode Fields

AMPHS1	AMPHS0	XT1 oscillator oscillation mode selection
0	0	Low power consumption oscillation (default)
0	1	Normal oscillation
1	0	Ultra-low power consumption oscillation
1	1	Setting prohibited

13.2 Configuration XT1

1) Set the XTSTOP bit in CSC[6] to disable the XT1 oscillator.
2) Change the oscillation mode (AMPHS1, AMPHS0) if required.
3) Set the oscillator mode by setting/clearing EXCLKS, OSCSELS fields in the CMC register (Table 21).
4) Clear the XTSTOP bit in CSC[6] (Table 20) to enable the XT1 oscillator.

Table 20: CSC Register

<table>
<tr><td>Symbol</td><td><7></td><td><6></td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td><0></td></tr>
<tr><td>CSC</td><td>MSTOP</td><td>XTSTOP</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>HIOSTOP</td></tr>
<tr><td rowspan="14"></td><td colspan="8"></td></tr>
<tr><td rowspan="2">MSTOP</td><td colspan="7">High-speed system clock operation control</td></tr>
<tr><td colspan="2">X1 oscillation mode</td><td colspan="4">External clock input mode</td><td>Input port mode</td></tr>
<tr><td>0</td><td colspan="2">X1 oscillator operating</td><td colspan="4">External clock from EXCLK pin is valid</td><td rowspan="2">Input port</td></tr>
<tr><td>1</td><td colspan="2">X1 oscillator stopped</td><td colspan="4">External clock from EXCLK pin is invalid</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td rowspan="2">XTSTOP</td><td colspan="7">Subsystem clock operation control</td></tr>
<tr><td colspan="2">XT1 oscillation mode</td><td colspan="4">External clock input mode</td><td></td></tr>
<tr><td>0</td><td colspan="2">XT1 oscillator operating</td><td colspan="4">External clock from EXCLKS pin is valid</td><td rowspan="2">Input port</td></tr>
<tr><td>1</td><td colspan="2">XT1 oscillator stopped</td><td colspan="4">External clock from EXCLKS pin is invalid</td></tr>
<tr><td colspan="8"></td></tr>
<tr><td>HIOSTOP</td><td colspan="7">High-speed on-chip oscillator clock operation control</td></tr>
<tr><td>0</td><td colspan="7">High-speed on-chip oscillator operating</td></tr>
<tr><td>1</td><td colspan="7">High-speed on-chip oscillator stopped</td></tr>
</table>

Table 21: CMC Register

Symbol	7	6	5	4	3	2	1	0
CMC	EXCLK	OSCSEL	EXCLKS	OSCSELS	0	AMPHS1	AMPHS0	AMPH
	EXCLK	OSCSEL	High-speed system clock pin operation mode		X1/P121 pin		X2/EXCLK/P122 pin	
	0	0	Input port mode		Input port			
	0	1	X1 oscillation mode		Crystal/ceramic resonator connection			
	1	0	Input port mode		Input port			
	1	1	External clock input mode		Input port		External clock input	
	EXCLKS	OSCSELS	Subsystem clock pin operation mode		XT1/P123 pin		XT2/EXCLKS/P124 pin	
	0	0			Input port			
	0	1			Crystal resonator connection			
	1	0			Input port			
	1	1			Input port		External clock input	
	AMPHS1	AMPHS0	XT1 oscillator oscillation mode selection					
	0	0	Low power consumption oscillation (default)					
	0	1	Normal oscillation					
	1	0	Ultra-low power consumption oscillation					
	1	1	Setting prohibited					
	AMPH	Control of X1 clock oscillation frequency						
	0	1 MHz ≤ fx ≤ 10 MHz						
	1	10 MHz ≤ fx ≤ 20 MHz						

14 Appendix D: Programming the Texas Instruments MSP430 low frequency oscillator

14.1 The MSP430 LFXT Oscillator

The LFXT1 oscillator supports ultra-low current consumption using a 32768 Hz watch crystal in LF mode (XTS = 0) or a high frequency crystal in HF mode. A watch crystal connects with the XIN and XOUT pins without any other external components. The software-selectable XCAPx bits configure the internally provided load capacitance for the LFXT1 crystal in LF mode. This capacitance can be selected as 1 pF, 6 pF, 10 pF, or 12.5 pF typical. Additional external capacitors can be added if necessary. The LFXT1 oscillator is not implemented in the MSP430G22x0 device family.

The LFXT1 oscillator also supports high-speed crystals or resonators when in HF mode (XTS = 1, XCAPx = 00). The high-speed crystal or resonator connects to XIN and XOUT and requires external capacitors on both terminals. When LFXT1 is in HF mode, the LFXT1Sx bits select the range of operation. LFXT1 may be used with an external clock signal on the XIN pin in either LF or HF mode when LFXT1Sx = 11, OSCOFF = 0, and XCAPx = 00. When used with an external signal, the external frequency must meet the data sheet parameters for the chosen mode. When the input frequency is below the specified lower limit, the LFXT1OF bit may be set preventing the CPU from being clocked with LFXT1CLK.

Steps to configure the LFXT1 oscillator:

1) Set the mode in XTS and the divider value in DIVAx.
2) Choose mode by changing the LFXT1Sx bits in BCSCTL3.
3) Enable internal capacitors if needed. It is controlled by XCAPx in BCSCTL3.
4) Turn on the oscillator by clearing XT2OFF in BCSCTL1.

Table 22: BCSCTL1, Basic Clock System Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	XT2OFF	XTS	DIVAx		RSELx			
State	rw-(1)	rw-(0)	rw-(0)	rw-(0)	rw-0	rw-1	rw-1	rw-1
	XT2OFF	Bit 7	XT2 off. This bit turns off the XT2 oscillator 0 XT2 is on 1 XT2 if off					
	XTS	Bit 6	LFXT1 mode select 0 Low-frequency mode 1 High-frequency mode					
	DIVAx	Bits 5-4	Divider for ACLK 00 /1 01 /2 10 /4 11 /8					
	RSELx	Bits 3-0	Range select. Sixteen different frequency ranges are available. The lowest frequency range is selected by setting RSELx = 0. RSEL3 is ignored when DCOR = 1					

Table 23: BCSCTL3, Basic Clock System Control Register 3

Bit	7	6	5	4	3	2	1	0
Name	XT2Sx		LFXT1Sx		XCAPx		XT2OF	LFXT1OF
State	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1	r0	r-(1)
	XT2Sx	Bits 7-6	XT2 range select. These bits select the frequency range for XT2.					
			00	0.4- to 1-MHz crystal or resonator				
			01	1- to 3-MHz crystal or resonator				
			10	3- to 16-MHz crystal or resonator				
			11	Digital external 0.4- to 16-MHz clock source				
	LFXT1Sx	Bits 5-4	Low-frequency clock select and LFXT1 range select. These bits select between LFXT1 and VLO when XTS = 0, and select the frequency range for LFXT1 when XTS = 1.					
			When XTS = 0:		When XTS = 1:			
			00	32768-Hz crystal on LFXT1	00	0.4- to 1-MHz crystal		
			01	Reserved	01	1- to 3-MHz crystal		
			10	VLOCLK	10	3- to 16-MHz crystal		
			11	External clock source	11	0.4- to 16-MHz clock source		
	XCAPx	Bits 3-2	Oscillator capacitor selection. These bits select the effective capacitance seen by the LFXT1 crystal when XTS = 0. If XTS = 1 or if LFXT1Sx = 11 XCAPx should be 00.					
			00	~1 pF				
			01	~6 pF				
			10	~10 pF				
			11	~12.5 pF				
	XT2OF	Bit 1	XT2 oscillator fault					
			0	No fault condition present				
			1	Fault condition present				
	LFXT1OF	Bit 0	LFXT1 oscillator fault					
			0	No fault condition present				
			1	Fault condition present				

Below is the configuration code of a base clock module example from IAR Embedded Workbench IDE:

```
BCSCTL3 = 0x00;          // 32768-Hz crystal, 1pF internal capacitor
BCSCTL1 = 0x00;          // XT2 oscillator is on, Low-frequency mode
```

14.2 Clock-out Capability

The microcontroller can be easily configured to clock external on-board peripherals from one of its pins. For this you need configure the PxSEL and PxSEL2 function registers that are used to select the pin function. A pin has to be configured as an output by setting needed in PxDIR.

Below is code from IAR Embedded Workbench that configures it:

```
P2SEL = P2SEL | 0x01;                  // Select ACLK function for pin
P2DIR = P2DIR | 0x01;                  // Set direction of P2.0 to output
```

Table 24: PxSEL and PxSEL2

PxSEL2	PxSEL	Pin Function
0	0	I/O function is selected
0	1	Primary peripheral module function is selected
1	0	Reserved. See device-specific data sheet
1	1	Secondary peripheral module function is selected

14.3 Low-power Modes

The MSP430 devices have several low-power modes. Every LPMx low-power mode allows developers to create an application with balanced power consumption. The low-power modes are configured with the CPUOFF, OSCOFF, SCG0, and SCG1 bits in the status register. The advantage of including the CPUOFF, OSCOFF, SCG0, and SCG1 mode-control bits in the status register is that the present operating mode is saved onto the stack during an interrupt service routine.

The ACLK clock is working in LPM0-LPM3 modes. The LPM4 mode disables CPU and all clocks.

Table 25: Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved							V	SCG1	SCG0	OSCOFF	CPUOFF	GIE	N	Z	C

Table 26: Low Power Modes and ACLK Clock

SCG1	SCG0	OSCOFF	CPUOFF	Mode	ACLK
0	0	0	0	Active	Enabled
0	0	0	1	LPM0	Enabled
0	1	0	1	LPM1	Enabled
1	0	0	1	LPM2	Enabled
1	1	0	1	LPM3	Enabled
1	1	1	1	LPM4	Disabled

15 Appendix E: Programming the NXP LPC1100 RTC Oscillator

15.1 Configuring the RTC Oscillator

The system clock block generates all clocks for the chip. The system block incorporates the low frequency RTC 32k oscillator. It provides a clock for the RTC block that resides in a separate always-on voltage domain with battery back-up. The RTC oscillator is also located in the always-on voltage domain. These circuits are always working independently of low-power modes. The RTC oscillator is easily controlled by RTCOSCCTRL.

Table 27: RTC Oscillator 32 kHz Output Control RTCOSCCTRL

Bit	Symbol	Value	Description	Reset Value
0	RTCOSCEN		Enable the RTC 32 kHz output.	1
		0	Disabled. 32 kHz output disabled.	
		1	Enabled. 32 kHz output enabled.	
31:1	-		Reserved	-

There is no possibility to bypass the RTC oscillator. The external clock should be applied to the RTCXIN pin.

15.2 Clock Output Capability

The LPC1100 devices feature a clock output function that routes the IRS oscillator, the system oscillator, the watchdog oscillator, or the main clock to an output pin. You can configure the MCU to get 32768 Hz clock from an I/O pin for on-board peripherals. To distribute 32k clock to the CLKOUT pin you need set the RTC clock for the main clock domain. There are several steps to do this:

Below is the code example from LPCXpresso IDE that configures the clock-out feature for LPC11U68:

```
// 1) Enable a clock for the GPIO clock domain
LPC_SYSCTL->SYSAHBCLKCTRL |= (1 << 6);

// 2) Set PLL input as a clock source of the main clock domain
LPC_SYSCTL->MAINCLKSEL = 0x1;

// 3) Configure the PIO0_1 as the CLKOUT pin
pIOCON->PIO0[1] = 0x1;

// 4) Set the main clock as a clock source for CLKOUT
LPC_SYSCTL->CLKOUTSEL = (uint32_t) 0x3;

// 5) Set divider to /1 for CLKOUT
LPC_SYSCTL->CLKOUTDIV = 1;
```

```
// 6) Set the RTC oscillator clock source as the clock source for the PLL
LPC_SYSCTL->SYSPLLCLKSEL = 0x3;

// 7) updated clock source for PLL
LPC_SYSCTL->SYSPLLCLKUEN = 0;
LPC_SYSCTL->SYSPLLCLKUEN = 1;

// update clock source for the main clock domain
LPC_SYSCTL->MAINCLKUEN = 0;
LPC_SYSCTL->MAINCLKUEN = 1;

// update clock source for CLKOUT
LPC_SYSCTL->CLKOUTUEN = 0;
LPC_SYSCTL->CLKOUTUEN = 0x1;
```

Table 28: System Clock Control SYSAHBCLKCTRL

Bit	Symbol	Value	Description	Reset Value
0	SYS		This bit is read-only and always reads as 1. It configures the always-on clock for the AHB, APB bridges the Cortex-M0 core clocks, SYSCON, reset control, SRAM0, and the PMU. Writes to this bit are ignored.	1
		0	Disable	
		1	Enable	
1	ROM		Enables clock for ROM.	1
		0	Disable	
		1	Enable	
2	RAM0		Enables clock for Main SRAM0.	1
		0	Disable	
		1	Enable	
3	FLASHREG		Enables clock for flash register interface.	1
		0	Disable	
		1	Enable	
4	FLASHARRAY		Enables clock for flash access.	1
		0	Disable	
		1	Enable	
5	I2C0		Enables clock for I2C.	0
		0	Disable	
		1	Enable	
6	GPIO		Enables clock for GPIO port registers.	1
		0	Disable	
		1	Enable	
7	CT16B0		Enables clock for 16-bit counter/timer 0.	0
		0	Disable	
		1	Enable	
8	CT16B1		Enables clock for 16-bit counter/timer 1.	0
		0	Disable	
		1	Enable	
9	CT32B0		Enables clock for 32-bit counter/timer 0.	0
		0	Disable	
		1	Enable	
10	CT32B1		Enables clock for 32-bit counter/timer 1.	0
		0	Disable	
		1	Enable	

Bit	Symbol	Value	Description	Reset Value
11	SSP0		Enables clock for SSP0.	1
		0	Disable	
		1	Enable	
12	USART0		Enables clock for USART0.	0
		0	Disable	
		1	Enable	
13	ADC		Enables clock for ADC.	0
		0	Disable	
		1	Enable	
14	USB		Enables clock to the USB register interface.	1
		0	Disable	
		1	Enable	
15	WWDT		Enables clock for WWDT.	0
		0	Disable	
		1	Enable	
16	IOCON		Enables clock for I/O configuration block.	0
		0	Disable	
		1	Enable	
17	-		Reserved	0
18	SSP1		Enables clock for SSP1.	0
		0	Disable	
		1	Enable	
19	PINT		Enables clock to GPIO Pin interrupt register interface.	0
		0	Disable	
		1	Enable	
20	USART1		Enables clock to USART1 register interface.	0
		0	Disable	
		1	Enable	
21	USART2		Enables clock to USART2 register interface.	0
		0	Disable	
		1	Enable	
22	USART3_4		Enables clock to USART3 and USART4 register interfaces.	0
		0	Disable	
		1	Enable	
23	GROUP0INT		Enables clock to GPIO GROUP0 interrupt register interface.	0
		0	Disable	
		1	Enable	

Bit	Symbol	Value	Description	Reset Value
24	GROUP1INT		Enables clock to GPIO GROUP1 interrupt register interface.	0
		0	Disable	
		1	Enable	
25	I2C1		Enables clock for I2C1.	0
		0	Disable	
		1	Enable	
26	RAM1		Enables clock for SRAM1 located at 0x2000 0000 to 0x2000 0800.	0
		0	Disable	
		1	Enable	
27	USBSRAM		Enables USB SRAM/SRAM2 block located at 0x2000 4000 to 0x2000 4800.	1
		0	Disable	
		1	Enable	
28	CRC		Enables clock for CRC.	0
		0	Disable	
		1	Enable	
29	DMA		Enables clock for DMA.	0
		0	Disable	
		1	Enable	
30	RTC		Enables clock for RTC register interface.	0
		0	Disable	
		1	Enable	
31	SCT0_1		Enables clock for SCT0 and SCT1.	0
		0	Disable	
		1	Enable	

Table 29: Main Clock Source Select MAINCLKSEL

Bit	Symbol	Value	Description	Reset Value
1:0	SEL		Clock source for main clock	0
		0x0	IRC Oscillator	
		0x1	PLL input	
		0x2	Watchdog oscillator	
		0x3	PLL output	
31:2	-		Reserved	-

Table 30: Digital Pin Control Register IOCON (PIO0_1)

Bit	Symbol	Value	Description	Reset Value
2:0	FUNC		Selects pin function.	0
		0x0	PIO0_1	
		0x1	CLKOUT	
		0x2	CT32B0_MAT2	
		0x3	USB_FTOGGLE	
		0x4..0x7	-	
4:3	MODE		Selects function mode (on-chip pull-up/pull-down resistor control).	0x2
		0x0	Inactive (no pull-down/pull-up resistor enabled).	
		0x1	Pull-down resistor enabled.	
		0x2	Pull-up resistor enabled.	
		0x3	Repeater mode.	
5	HYS		Hysteresis.	0
		0	Disable	
		1	Enable	
6	INV		Invert input	0
		0	Input not inverted (HIGH on pin reads as 1)	
		1	Input inverted (HIGH on pin reads as 0)	
9:7	-	-	Reserved	0
10	OD		Open-drain mode	0
		0	Disable	
		1	Enable. Open-drain mode enabled	
12:11	S_MODE		Digital filter sample mode.	0
		0x0	Bypass input filter.	
		0x1	1 clock cycle.	
		0x2	2 clock cycles.	
		0x3	3 clock cycles.	
15:13	CLKDIV		Select peripheral clock divider for input filter sampling clock IOCONCLKDIV. Value 0x7 is reserved.	0
		0x0	IOCONCLKDIV0. Use IOCON clock divider 0.	
		0x1	IOCONCLKDIV1. Use IOCON clock divider 1.	
		0x2	IOCONCLKDIV2. Use IOCON clock divider 2.	
		0x3	IOCONCLKDIV3. Use IOCON clock divider 3.	
		0x4	IOCONCLKDIV4. Use IOCON clock divider 4.	
		0x5	IOCONCLKDIV5. Use IOCON clock divider 5.	
		0x6	IOCONCLKDIV6. Use IOCON clock divider 6.	
31:16	-	-	Reserved	0

Table 31: CLKOUT Clock Source Select CLKOUTSEL

Bit	Symbol	Value	Description	Reset Value
1:0	SEL		CLKOUT clock source	0
		0x0	IRC oscillator	
		0x1	Crystal oscillator (SYSOSC)	
		0x2	Watchdog oscillator	
		0x3	Main clock	
31:2	-		Reserved	0

Table 32: CLKOUT Clock Divider CLKOUTDIV

Bit	Symbol	Value	Description	Reset Value
7:0	DIV		CLKOUT clock divider values	0
		0	Disable CLKOUT clock divider.	
		1	Divide by 1.	
		to 255	Divide by 255.	
31:8	-		Reserved	0

Table 33: System PLL Clock Source Select SYSPLLCLKSEL

Bit	Symbol	Value	Description	Reset Value
1:0	SEL		System PLL clock source	0
		0x0	IRC	
		0x1	System oscillator. Crystal Oscillator.	
		0x2	Reserved	
		0x3	32 kHz clock. Select this option when the 32 kHz clock is the clock source for the main clock and select the pll input in the MAINCLKSEL register. Do not use the 32 kHz clock with the PLL.	
31:2	-		Reserved	0

Table 34: System PLL Clock Source Update Enable Register SYSPLLCLKUEN

Bit	Symbol	Value	Description	Reset Value
0	ENA		Enable system PLL clock source update	1
		0	No change	
		1	Update clock source	
31:1	-	-	Reserved	-

Table 35: Main Clock Source Update Enable Register MAINCLKUEN

Bit	Symbol	Value	Description	Reset Value
0	ENA		Enable main clock source update	1
		0	No change	
		1	Update clock source	
31:1	-	-	Reserved	-

Table 36: CLKOUT Clock Source Update Enable Register CLKOUTUEN

Bit	Symbol	Value	Description	Reset Value
0	ENA		Enable CLKOUT clock source update	1
		0	No change	
		1	Update clock source	
31:1	-	-	Reserved	-

16 Appendix F: Programming the Freescale Kinetis L4x and L5x System Oscillator

16.1 Programming Model

The MCU incorporates two modules managing a clock distribution. The selection and multiplexing of system clock sources is controlled and programmed via the multipurpose clock generator (MCG) module. The setting of clock dividers and module clock gating for the system are programmed via the system integration module (SIM). The system oscillator, MCG and SIM registers control the multiplexers, dividers and clock gates.

NOTE. After OSC is enabled and starts generating clocks, the configurations such as low power and frequency range must not be changed.

The oscillator module has built-in load capacitors for a connected crystal. OSC0_CR controls low power modes operation and the load capacitors. If ERCLKEN and EREFSTEN in OSC0_CR are set, the OSC is in operation when the MCU enters Stop modes.

Table 37: OSC Control Register (OSCx_CR)

Bit	Symbol	Value	Description
7	ERCLKEN		External Reference Enable. Enables external reference clock (OSCERCLK).
		0	External reference clock is inactive.
		1	External reference clock is enabled.
6	Reserved		This read-only field is reserved and always has the value 0.
5	EREFSTEN		External Reference Stop Enable. Controls whether or not the external reference clock (OSCERCLK) remains enabled when MCU enters Stop mode.
		0	External reference clock is disabled in Stop mode.
		1	External reference clock stays enabled in Stop mode if ERCLKEN is set before entering Stop mode.
4	Reserved		This read-only field is reserved and always has the value 0.
3	SC2P		Oscillator 2 pF Capacitor Load Configure. Configures the oscillator load.
		0	Disable the selection.
		1	Add 2 pF capacitor to the oscillator load.
2	SC4P		Oscillator 4 pF Capacitor Load Configure. Configures the oscillator load.
		0	Disable the selection.
		1	Add 4 pF capacitor to the oscillator load.
1	SC8P		Oscillator 8 pF Capacitor Load Configure. Configures the oscillator load.
		0	Disable the selection.
		1	Add 8 pF capacitor to the oscillator load.
0	SC16P		Oscillator 16 pF Capacitor Load Configure. Configures the oscillator load.
		0	Disable the selection.
		1	Add 16 pF capacitor to the oscillator load.

The system oscillator supports 32 kHz oscillators as well as crystals with higher frequency (3 to 32 MHz). Three clocks are output from OSC module:

- OSCCLK for MCU system
- OSCERCLK for on-chip peripherals
- OSC32KCLK

RANGE0 bits in MGC_C2[5:4] define frequency range for the crystal oscillator. You have to clear RANGE0 bits to select the oscillator frequency range for 32 kHz operation.

The oscillator output clock (OSC_CLK_OUT) is gated off until the counter has detected 4096 cycles of its input clock (XTL_CLK). After 4096 cycles are completed, the counter passes XTL_CLK onto OSC_CLK_OUT. This counting time-out is used to guarantee output clock stability.

Table 38: MCG Control 2 Register (MCG_C2)

Bit	Symbol	Value	Description
7	LOCRE0		Loss of Clock Reset Enable. Determines whether an interrupt or a reset request is made following a loss of OSC0 external reference clock. The LOCRE0 only has an affect when CME0 is set.
		0	Interrupt request is generated on a loss of OSC0 external reference clock.
		1	Generate a reset request on a loss of OSC0 external reference clock.
6	Reserved		This read-only field is reserved and always has the value 0.
5-4	RANGE0		Frequency Range Select. Selects the frequency range for the crystal oscillator or external clock source. See the Oscillator (OSC) chapter for more details and the device data sheet for the frequency ranges used.
		00	Encoding 0 — Low frequency range selected for the crystal oscillator.
		11	Encoding 1 — High frequency range selected for the crystal oscillator.
		1x	Encoding 2 — Very high frequency range selected for the crystal oscillator.
3	HGO0		High Gain Oscillator Select. Controls the crystal oscillator mode of operation. See the Oscillator (OSC) chapter for more details.
		0	Configure crystal oscillator for low-power operation.
		1	Configure crystal oscillator for high-gain operation.
2	EREFS0		External Reference Select. Selects the source for the external reference clock. See the Oscillator (OSC) chapter for more details.
		0	External reference clock requested.
		1	Oscillator requested.
1	LP		Low Power Select. Controls whether the FLL is disabled in BLPI and BLPE modes. In FBE mode, setting this bit to 1 will transition the MCG into BLPE mode; in FBI mode, setting this bit to 1 will transition the MCG into BLPI mode. In any other MCG mode, LP bit has no affect.
		0	FLL is not disabled in bypass modes.
		1	FLL is disabled in bypass modes (lower power)
0	IRCS		Internal Reference Clock Select. Selects between the fast or slow internal reference clock source.
		0	Slow internal reference clock selected.
		1	Fast internal reference clock selected.

Table 39: MCG Status Register (MCG_S)

Bit	Symbol	Value	Description
7-5	Reserved		Reserved. This field is reserved. This read-only field is reserved and always has the value 0.
		0	Interrupt request is generated on a loss of OSC0 external reference clock.
		1	Generate a reset request on a loss of OSC0 external reference clock.
4	IREFST		Internal Reference Status This bit indicates the current source for the FLL reference clock. The IREFST bit does not update immediately after a write to the IREFS bit due to internal synchronization between clock domains.
		0	Source of FLL reference clock is the external reference clock.
		1	Source of FLL reference clock is the internal reference clock.
3-2	CLKST		Clock Mode Status. These bits indicate the current clock mode. The CLKST bits do not update immediately after a write to the CLKS bits due to internal synchronization between clock domains.
		00	Encoding 0 — Output of the FLL is selected (reset default).
		01	Encoding 1 — Internal reference clock is selected.
		10	Encoding 2 — External reference clock is selected.
		11	Reserved.
1	OSCINIT0		OSC Initialization. This bit, which resets to 0, is set to 1 after the initialization cycles of the crystal oscillator clock have completed. After being set, the bit is cleared to 0 if the OSC is subsequently disabled. See the OSC module's detailed description for more information.
0	IRCST		Internal Reference Clock Status. The IRCST bit indicates the current source for the internal reference clock select clock (IRCSCLK). The IRCST bit does not update immediately after a write to the IRCS bit due to internal synchronization between clock domains. The IRCST bit will only be updated if the internal reference clock is enabled, either by the MCG being in a mode that uses the IRC or by setting the C1[IRCLKEN] bit.
		0	Source of internal reference clock is the slow clock (32 kHz IRC).
		1	Source of internal reference clock is the fast clock (4 MHz IRC).

Table 40: System Options Register 2 (SIM_SOPT2)

Bit	Symbol	Value	Description
31-28	Reserved		This field is reserved. This read-only field is reserved and always has the value 0.
27-26	UART0SRC		UART0 clock source select. Selects the clock source for the UART0 transmit and receive clock.
		00	Clock disabled
		01	MCGFLLCLK clock
		10	OSCERCLK clock
		11	MCGIRCLK clock
25-24	TPMSRC		TPM clock source select. Selects the clock source for the TPM counter clock
		00	Clock disabled
		01	MCGFLLCLK clock
		10	OSCERCLK clock
		11	MCGIRCLK clock
23-8	Reserved		This field is reserved. This read-only field is reserved and always has the value 0.
7-5	CLKOUTSEL		CLKOUT select. Selects the clock to output on the CLKOUT pin.
		000	Reserved.
		001	Reserved.
		010	Bus clock.
		011	LPO clock (1 kHz)
		100	MCGIRCLK
		101	Reserved.
		110	OSCERCLK
		111	Reserved.
4	RTCCLKOUTSEL		RTC clock out select. Selects either the RTC 1 Hz clock or the OSC clock to be output on the RTC_CLKOUT pin.
		0	RTC 1 Hz clock is output on the RTC_CLKOUT pin.
		1	OSCERCLK clock is output on the RTC_CLKOUT pin.
3-0	Reserved		This field is reserved. This read-only field is reserved and always has the value 0.

Table 41: MCG Control 4 Register (MCG_C4)

<table>
<tr><th>Bit</th><th>Symbol</th><th>Value</th><th colspan="5">Description</th></tr>
<tr><td rowspan="12">7</td><td rowspan="12">DMX32</td><td rowspan="10"></td><td colspan="5">DCO Maximum Frequency with 32.768 kHz Reference. The DMX32 bit controls whether the DCO frequency range is narrowed to its maximum frequency with a 32.768 kHz reference. The following table identifies settings for the DCO frequency range.

NOTE: The system clocks derived from this source should not exceed their specified maximums.</td></tr>
<tr><td>DRST_DRS</td><td>DMX32</td><td>Reference Range</td><td>FLL Factor</td><td>DCO Range</td></tr>
<tr><td rowspan="2">00</td><td>0</td><td>31.25–39.0625 kHz</td><td>640</td><td>20–25 MHz</td></tr>
<tr><td>1</td><td>32.768 kHz</td><td>732</td><td>24 MHz</td></tr>
<tr><td rowspan="2">01</td><td>0</td><td>31.25–39.0625 kHz</td><td>1280</td><td>40–50 MHz</td></tr>
<tr><td>1</td><td>32.768 kHz</td><td>1464</td><td>48 MHz</td></tr>
<tr><td rowspan="2">10</td><td>0</td><td>31.25–39.0625 kHz</td><td>1920</td><td>60–75 MHz</td></tr>
<tr><td>1</td><td>32.768 kHz</td><td>2197</td><td>72 MHz</td></tr>
<tr><td rowspan="2">11</td><td>0</td><td>31.25–39.0625 kHz</td><td>2560</td><td>80–100 MHz</td></tr>
<tr><td>1</td><td>32.768 kHz</td><td>2929</td><td>96 MHz</td></tr>
<tr><td>0</td><td colspan="5">DCO has a default range of 25%.</td></tr>
<tr><td>1</td><td colspan="5">DCO is fine-tuned for maximum frequency with 32.768 kHz reference.</td></tr>
<tr><td rowspan="5">6-5</td><td rowspan="5">DRST_DRS</td><td></td><td colspan="5">DCO Range Select. The DRS bits select the frequency range for the FLL output, DCOOUT. When the LP bit is set, writes to the DRS bits are ignored. The DRST read field indicates the current frequency range for DCOOUT. The DRST field does not update immediately after a write to the DRS field due to internal synchronization between clock domains. See the DCO Frequency Range table for more details.</td></tr>
<tr><td>00</td><td colspan="5">Encoding 0 — Low range (reset default).</td></tr>
<tr><td>01</td><td colspan="5">Encoding 1 — Mid range.</td></tr>
<tr><td>10</td><td colspan="5">Encoding 2 — Mid-high range.</td></tr>
<tr><td>11</td><td colspan="5">Encoding 3 — High range.</td></tr>
<tr><td>4-1</td><td>FCTRIM</td><td></td><td colspan="5">Fast Internal Reference Clock Trim Setting FCTRIM controls the fast internal reference clock frequency by controlling the fast internal reference clock period. The FCTRIM bits are binary weighted, that is, bit 1 adjusts twice as much as bit 0. Increasing the binary value increases the period, and decreasing the value decreases the period. If an FCTRIM[3:0] value stored in nonvolatile memory is to be used, it is your responsibility to copy that value from the nonvolatile memory location to this register.</td></tr>
<tr><td>0</td><td>SCFTRIM</td><td></td><td colspan="5">Slow Internal Reference Clock Fine Trim. SCFTRIM controls the smallest adjustment of the slow internal reference clock frequency. Setting SCFTRIM increases the period and clearing SCFTRIM decreases the period by the smallest amount Possible.
If an SCFTRIM value stored in nonvolatile memory is to be used, it is your responsibility to copy that value from the nonvolatile memory location to this bit.</td></tr>
</table>

Below is the code example from CodeWarrior Development Studio showing configuration to be run with SiT1533AI-H4 in Mode-1.

```
// 1) Enable external reference clock (OSCERCLK) and disable all the
//    built-in load capacitors
OSC0_CR = 0xA0;

// 2) Configure MCG_C2. Set low frequency range for the crystal
//    oscillator, low power mode and select external reference
MCG_C2 &= ~(0x3C);

// 3) Select external reference
MCG_C2 |= 0x04;

// 4) Wait for oscillator initialization has completed
while((MCG_S & 0x2) != 0x2);
```

16.2 Clock Output Capability

The MCU has the RTC_CLKOUT pin that can be driven either with RTC 1 Hz or with the OSCERCLK on-chip clock source. Control for this option is through SIM_SOPT2[4] bit. SIM_SOPT2[7:5] bits control the clock source.

Below is the code example configuring the RTC_CLKOUT pin to be driven by a clock source:

```
// 1) Configure PTC13 pin as output
PORTB_PCR13 = (PORT_PCR_MUX(0x3));

// 2) Select clock source
SIM_SOPT2 |= (uint32_t) 0xD0;
```

17 Appendix G: Programming the PIC18 MCU Secondary Oscillator

The secondary oscillator is part of Timer1 and can be configured by customizing Timer1 registers. Timer1 can operate in three modes:

- Timer
- Synchronous Counter
- Asynchronous Counter

Timer1 requires clocking for operation. There are three clock sources:

- Internal Clock (system clock routed from high-speed oscillator or from internal RC oscillator)
- Secondary Oscillator (with a 32 kHz crystal connected)
- External Clock (from T1OSO pin)

When configuring the secondary oscillator, the user must provide a software time delay to ensure proper start-up. When Timer1 is enabled, the RC1/T1OSI and RC0/T1OSO/T13CKI pins become inputs. This means the values of TRISC are ignored and the pins are read as ‘0’.

PIC18 MCUs are simple devices to program. All Timer1 configurations can be accomplished in one register. Timer1 is controlled by T1CON (Timer1 Control Register). It also contains the Timer1 Oscillator Enable bit (T1OSCEN). Timer1 can be enabled or disabled by setting or clearing control bit TMR1ON (T1CON<0>).

Table 42: Timer1 Control Register (T1CON)

R/W-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	**T1RUN**	**T1CKPS1**	**T1CKPS0**	**T1OSCEN**	**T1SYNC**	**TMR1CS**	**TMR1ON**
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit 7	**RD16:**	16-Bit Read/Write Mode Enable bit					
	1	Enables register read/write of Timer1 in one 16-bit operation					
	0	Enables register read/write of Timer1 in two 8-bit operations					
Bit 6	**T1RUN:**	Timer1 System Clock Status bit					
	1	Device clock is derived from Timer1 oscillator					
	0	Device clock is derived from another source					
Bit 5-4	**T1CKPS<1:0>**	Timer1 Input Clock Prescale Select bits					
	11	1:8 Prescale value					
	10	1:4 Prescale value					
	01	1:2 Prescale value					
	00	1:1 Prescale value					
Bit 3	**T1OSCEN:**	Timer1 Oscillator Enable bit					
	1	Timer1 oscillator is enabled					
	0	Timer1 oscillator is shut off.					
Bit 2	**T1SYNC:**	Timer1 External Clock Input Synchronization Select bit					
	When TMR1CS = 1						
	1	Do not synchronize external clock input					
	0	Synchronize external clock input					
		Timer1 uses the internal clock when TMR1CS = 0 and this bit is ignored.					
Bit 1	**TMR1CS:**	Timer1 Clock Source Select bit					
	1	External clock from RC0/T1OSO/T13CKI pin (on the rising edge)					
	0	Internal clock (FOSC/4)					
Bit 0	**TMR1ON:**	Timer1 On bit					

	1	Enables Timer1
	0	Stops Timer1

Below are two code snippets for configuring the oscillator to operate in Mode-1 and Mode-3:

```
// Configure Secondary Oscillator in Mode-1
// enable Timer1 Oscillator
T1CON = 0x08;
// enabling Timer1 and switching to Secondary Oscillator clock
T1CON |= 0xC3;

// Configure Secondary Oscillator in Mode-3 (Bypass Mode)
// enabling Timer1 and switching to Secondary Oscillator clock
T1CON = 0xC3;
```

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