White Paper

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A Signal Integrity Comparison of 25 Gbps Backplane Systems Using Varying High-Density Connector Performance Levels

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Abstract

To address the ever-increasing need to widen network bandwidth, signal integrity (SI) engineers continue to push backplane link speeds toward 25 Gbps. When designing links, SI engineers often begin with a specific connector platform and then modify system variables such as trace length, dielectric materials, and equalization settings to achieve acceptable performance. This paper takes a different approach by setting various system and equalizer parameters to slightly aggressive values and then studying the effect of various connector performance levels. The result of the paper is a set of connector performance guidelines that can be referenced in order to design 25 Gbps backplane systems successfully.

Author Biography

Chad Morgan earned his degree in Electrical Engineering from the Pennsylvania State University, University Park, in 1995. For the past 13 years, he has worked in the Circuits & Design group of Tyco Electronics as a signal integrity engineer, specializing in the analysis & design of high-speed, high-density components. Currently, he is a Principal Engineer at Tyco Electronics, where he focuses on high-frequency measurement & characterization of components & materials, full-wave electromagnetic modeling of high-speed interconnects, and the simulation of digital systems. Mr. Morgan's responsibilities at Tyco Electronics include numerous research activities, and he has presented multiple papers at both DesignCon and the International Microwave Symposium. Recent publications include:

"Solutions for Causal Modeling and a Technique for Measuring Causal, Broadband Dielectric Properties", DesignCon08, Track 5-TA4.

"The Need for Impulse Response Models and an Accurate Method for Impulse Generation from Band-Limited S-Parameters", DesignCon08, Track 7-WA1.

"Transition to Surface-Mount: An Analysis of Signal Integrity Improvement versus Manufacturing Concerns in Multi-Gigabit Systems Using High-Density Connectors", DesignCon05 TecForum.

"Obtaining Accurate Device-Only S-Parameter Data to 15-20 GHz Using In-Fixture Measurement Techniques", DesignCon04, Track 7-TP1.

"The Impact of PWB Construction on High-Speed Signals", DesignCon99, Track H412.

Introduction

To address the ever-increasing need to widen network bandwidth, signal integrity (SI) engineers continue to push backplane link speeds toward 25 Gbps. Past simulation studies, presented at DesignCon and before IEEE and OIF committees, have often accepted a certain level of connector differential insertion loss and crosstalk and then optimized other system variables in order to successfully transmit high-speed signals across backplanes. Specifically, system trace lengths, dielectric materials, and tap settings for pre-emphasis and decision-feedback equalization (DFE) have been optimized to account for given connector imperfections.

This paper studies 25 Gbps signaling across backplane environments using a slightly different approach. In this paper, system criteria such as chip parasitics, trace lengths and widths, dielectric materials, and equalization settings are fixed at slightly aggressive settings while high-speed, high-density connector performance itself is varied. Different connector (and footprint) differential insertion loss and crosstalk levels are studied in the pre-defined systems to determine the connector performance required to allow successful 25 Gbps transmission across given backplanes.

Specific system settings for anticipated 25 Gbps backplane environments are determined via common industry specifications (such as IEEE 802.3ap, IEEE 802.3ba, OIF-CEI-11G-LR, and OIF-CEI-28G-SR) and knowledge of available PCB materials and construction technology. The system specifications chosen allow successful 25 Gbps transmission (with margin) when no connector differential insertion loss or crosstalk is included in the simulation. Note that both a short system (14.8”) and a long system (30.8”) are examined.

Given the short and long fixed systems, various levels of connector (and footprint) performance are then included in the channels. Specifically, this paper examines 3 generations of high-speed, high-density interconnection performance levels, where each subsequent generation represents an improvement in electrical performance. For each interconnect generation, connector-only performance metrics such as impedance, differential insertion loss, and total near/far-end crosstalk (NEXT/FEXT) are given. The effect of each interconnect’s performance on the final system eye pattern is then shown.

Note that all simulations reported in this presentation use random-pattern, binary NRZ signaling at 25 Gbps and include the effects of chip parasitics and jitter. Simulations are included for throughput-only and throughput with NEXT and FEXT. The end result of the paper is a set of connector (and footprint) performance guidelines that can be referenced when choosing the proper connector for successfully designing a 25 Gbps backplane link.

System Parameters and Simulation Setup

The goal in choosing base system parameters is to create lossy channels that allow 25 Gbps signals to transmit successfully with margin when no connector reflections or noise are present. The primary goal of the paper is then to examine how real connector (and footprint) imperfections affect the final 25 Gbps signal. For this study, the system parameters shown in Figure 1 are used. These values represent realistic backplane channel parameters that are slightly aggressive yet achievable in next generation 25 Gbps systems.

In this study, two system lengths are examined using highly reliable and validated models. The first system length of 14.8" consists of two 3" daughtercard traces, a 6" backplane trace, and two 1.4" 'perfect connection' models (lossy, reflectionless, and noiseless). The second system length of 30.8" consists of two 4" daughtercard traces, a 20" backplane trace, and two 1.4" 'perfect connection' models. The 1.4" length for the 'perfect connection' model comes from the addition of a 0.250" backplane footprint, a 1" connector, and a 0.150" daughtercard footprint. All differential pairs consist of 6 mil traces with 8 mil spacings in Nelco 4000-13SI (ε_r=3.5, tanδ=0.008). All differential pairs are routed on the backplane and daughtercard bottom layer so that signals travel all the way through the board in the connector footprints.

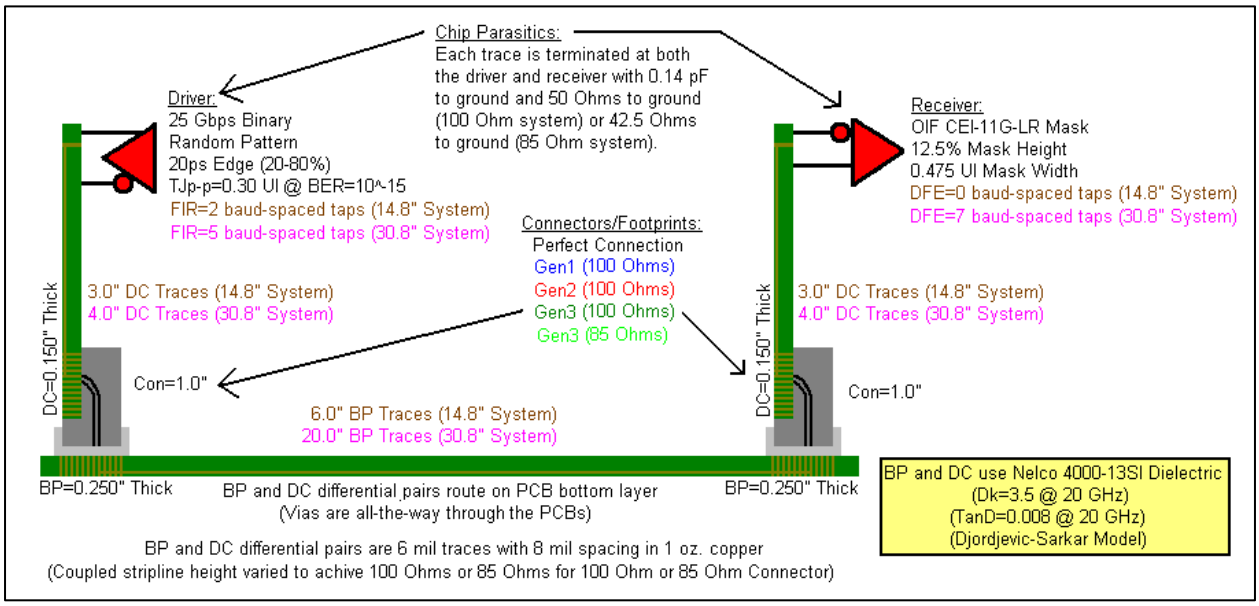


Figure 1: Backplane Channel Parameters

Chip parasitics are included within the channel models. The OIF CEI-11G-LR standard specifies that chip capacitance to ground must be low enough such that the return loss looking into a chip is below -8 dB at 75% of the baud rate. For 25 Gbps signals, this means that the return loss of the parallel chip capacitance and termination resistance must be less than -8 dB at 18.75 GHz. Simulations show that a value of 0.14 pF meets this criterion, so this value is used.

Ideal channels using 'perfect connection' models tune all differential pair stackup heights to achieve 100 Ω. When real Generation 1 (Gen1), Generation 2 (Gen2), and Generation 3 (Gen3) 100 Ω connector (and footprint) models replace the 'perfect connections', differential pairs and chip terminations remain at 100 Ω. However, when the Gen3 85 Ω connector (and footprint) model replaces the 'perfect connection', all differential pair stackup heights are lowered to achieve 85 Ω. In this scenario, chip terminations are also changed to 85 Ω. In other words, all backplane channels use 100 Ω differential pairs and chip terminations, except for the Gen3 85 Ω connector (and footprint), which uses 85 Ω differential pairs and chip terminations.

Besides the physical model permutations described above, time-domain system simulations then use carefully selected criteria. First, all signals use random-pattern, binary NRZ coding at 25 Gbps. These signals are jittered with DJ_{p-p} = 6 ps and RJ_{σ} = 0.378 ps such that the total peak-to-

peak jitter at a bit error rate (BER) of 10^{-15} is TJ_{p-p} = 12 ps or 0.30 UI. Eye pattern simulations are run in Stateye 4.2.3. 14.8" systems use 2-tap, baud-spaced FIR pre-emphasis while 30.8" systems use both 5-tap, baud-spaced FIR pre-emphasis and 7-tap, baud-spaced DFE equalization. Ultimately, received signals are judged against the OIF CEI-11G-LR receiver mask (12.5% height, 0.475 UI width).

'Perfect Connection' Channel Results

As already stated, the goal in selecting system parameters is to choose aggressive, yet realistic values that allow 25 Gbps signals to be transmitted across both a short (14.8") and a long (30.8") system when no connector (and footprint) reflections or noise are present. Figure 2 and Figure 3 below show the performance of both 'perfect connection' channels. These channels include loss and dispersion, but there is no noise in the system and the only reflections come from 0.14 pF chip parasitics. For the 14.8" system, only 2 baud-spaced pre-emphasis taps are required to transmit 25 Gbps data successfully with 19.3% margin. The 30.8" system, on the other hand, requires 5 baud-spaced pre-emphasis taps and 7 baud-spaced DFE taps to transmit 25 Gbps data successfully with 3.9% margin.

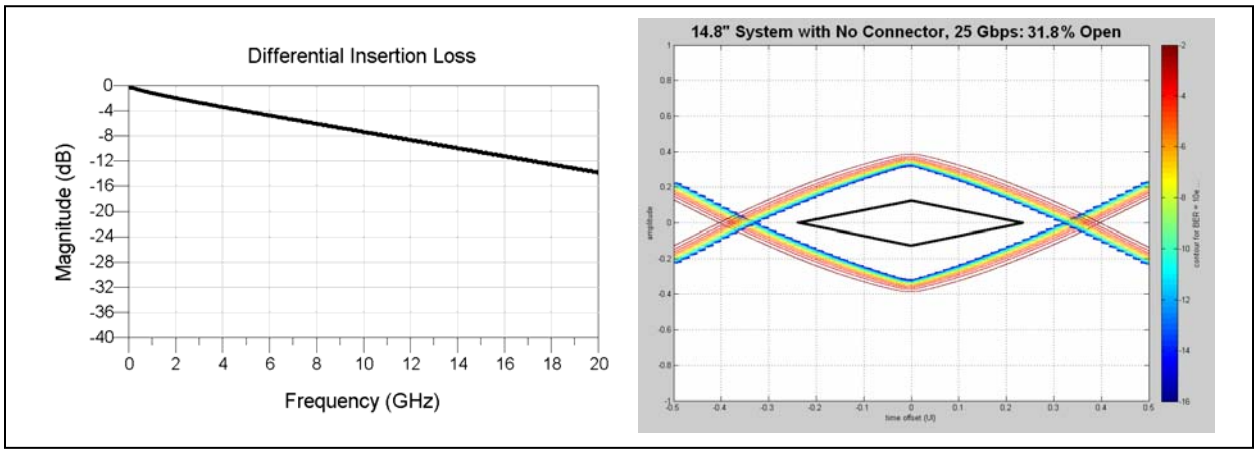


Figure 2: 14.8" 'Perfect Connection' Channel - Differential Insertion Loss & 25 Gbps Eye Pattern
(Pre-emphasis taps = 0.79375, -0.2625)

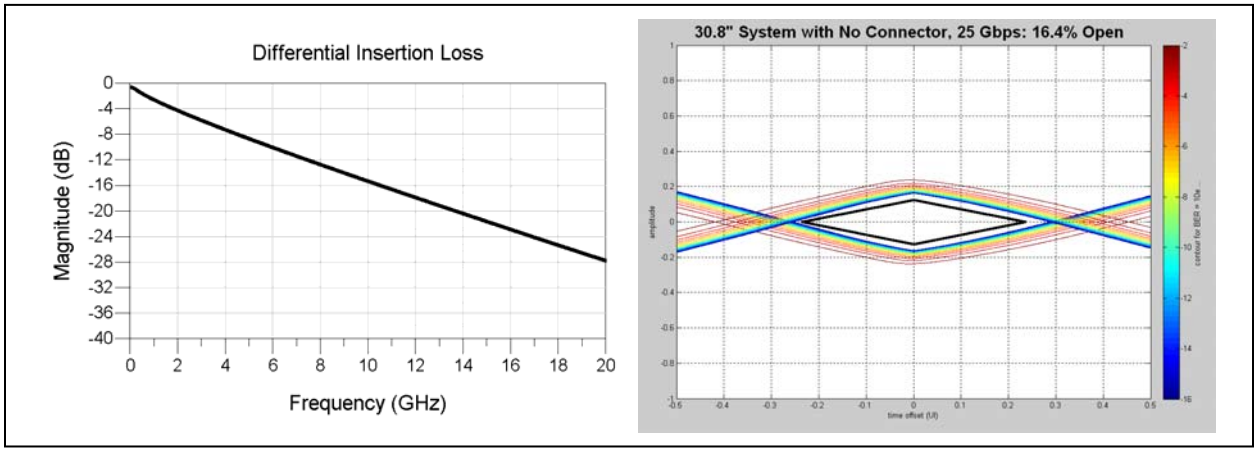


Figure 3: 30.8" 'Perfect Connection' Channel - Differential Insertion Loss & 25 Gbps Eye Pattern
(Pre-emphasis taps = -0.00203, -0.00866, 0.974723, -0.00377, -0.01082)
(DFE taps = 0.21424, 0.10114, 0.05682, 0.03663, 0.02511, 0.01797, 0.01371)

Real Connector Channel Results

Without including any real connectors (and footprints) in the 'perfect connection' channels, it is clear that successful 25 Gbps signal transmission is a challenge requiring tight jitter control, small chip parasitics, and aggressive equalization techniques for longer channels. Even so, it is clear that 25 Gbps transmission is possible. The next task is to introduce varying levels of connector (and footprint) technology into the channels to examine the impact on received data.

Connector Details

In this paper, three generations of presently existing high-speed, high-density connectors are introduced into the short and long channels to examine their impact on 25 Gbps data throughput. For each channel, a specified connector generation's electrical model replaces the ideal 1.4" 'perfect connection' model. It is important to note that *the connector model includes the 0.250" through-the-board backplane footprint, the 1" long connector differential pair, and the 0.150" through-the-board daughtercard footprint*. It is also important to note that *all three generations of connectors (and footprints) currently exist*. Each connector generation represents an advancement in connector technology with Gen3 performance being the best.

Connector Comparison Data

To quantify the performance of each connector generation, Figure 4 and Figure 5 show the time-domain and frequency-domain data. Note that the Gen1, Gen2, and Gen3 100 Ω connectors are simulated in a 100 Ω environment, but the Gen3, 85 Ω connector is simulated in an 85 Ω environment.

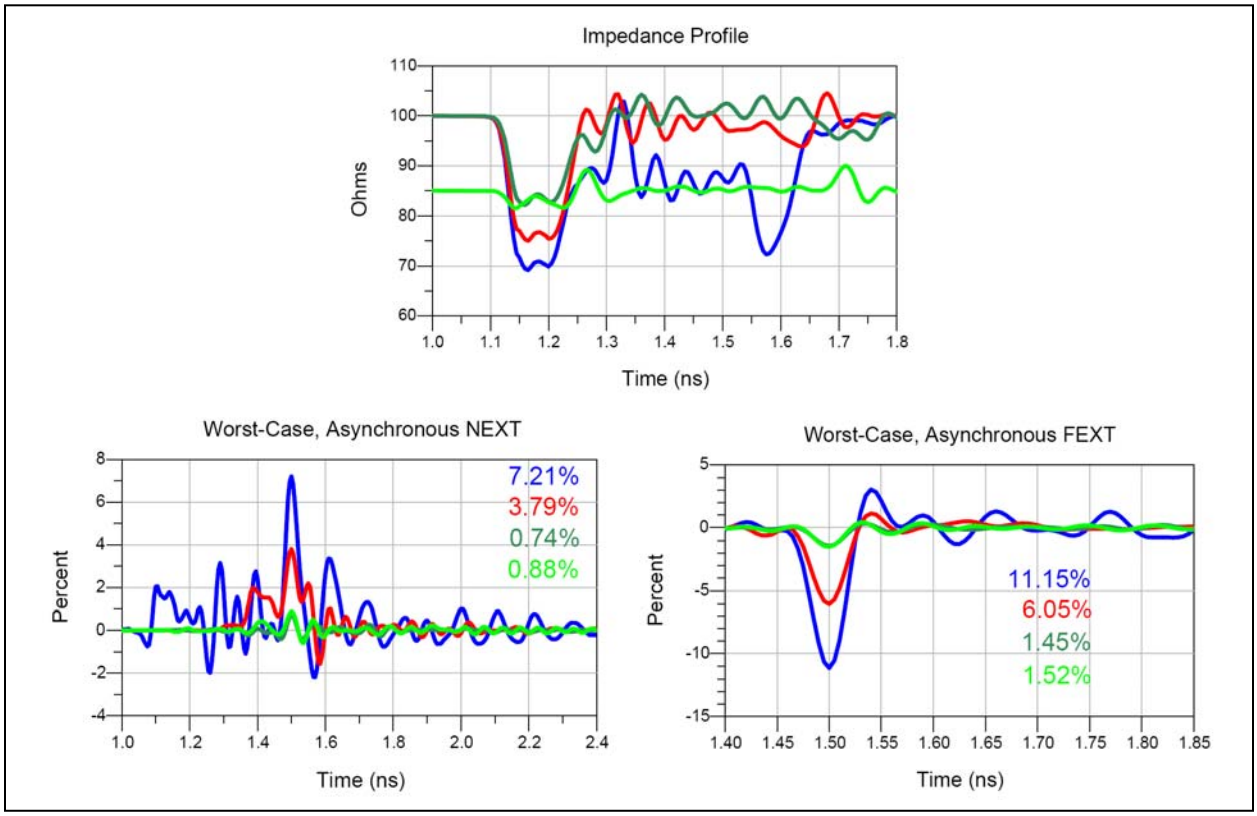


Figure 4: Backplane Footprint – Connector – Daughtercard Footprint Zo, NEXT, and FEXT TDR Comparison Data (20ps rise time, 20-80%) (Gen1 100 Ω=Blue, Gen2 100 Ω=Red, Gen3 100 Ω=Green, Gen3 85 Ω=Lime)

As should be clear from Figure 4, the Gen1 connector (with footprints) shows a worst-case backplane footprint impedance of 70 Ω and total worst-case asynchronous noise of NEXT = 7.21% and FEXT = 11.15% (20ps rise time, 20-80%). The Gen2 connector (with footprints) then shows a worst-case backplane footprint impedance of 75 Ω and total worst-case asynchronous noise of NEXT = 3.79% and FEXT = 6.05%. Finally, the Gen3 connector (with footprints) shows a worst-case backplane footprint impedance of 82 Ω and total worst-case asynchronous noise of NEXT < 0.88% and FEXT < 1.52%. Note that 'worst-case asynchronous' noise is calculated using all nearby aggressor pairs where the peak magnitude of each aggressor is time- and polarity-aligned before adding to achieve a worst-case value.

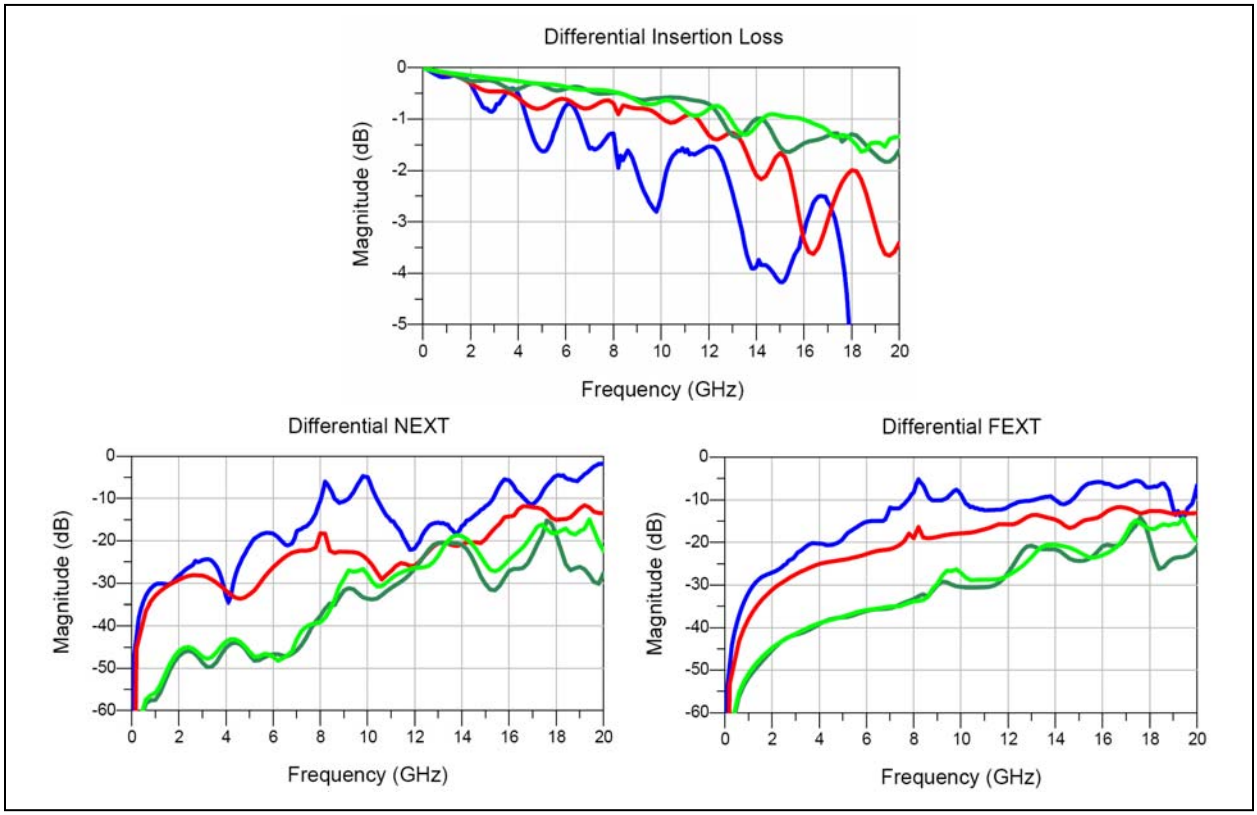


Figure 5: Backplane Footprint – Connector – Daughtercard Footprint SDD21, NEXT, and FEXT Comparison Data (Gen1 100 Ω=Blue, Gen2 100 Ω=Red, Gen3 100 Ω=Green, Gen3 85 Ω=Lime)

Figure 5 shows the frequency-domain behavior of each connector (and footprints). As expected, the Gen1 connector, having the largest impedance discontinuity, shows the poorest differential insertion loss performance. With subsequent generational improvements in impedance matching, the Gen2 and Gen3 connectors (and footprints) then show improving differential insertion loss. Note that the Gen3, 85 Ω connector shows the best throughput, since it shows the best impedance match in its simulated 85 Ω environment.

Figure 5 also shows substantial improvements in differential NEXT and FEXT from generation to generation of connectors. Note that these plots show total frequency-domain noise where all aggressor *magnitudes* are added. Although this worst-case frequency-domain noise is not possible at all frequencies, it provides a worst-case bound for noise plotting that is a more realistic metric than the root sum of squares (RSS) method, which underestimates total noise.

14.8" Channel Comparison Data

Given the four connectors (and footprints), the next step is to examine the effect of inserting each of them into the 14.8" system. Figure 6 shows the time-domain NEXT and FEXT of each 14.8" channel using a 20ps (20%-80%) TDR response. Figure 7 then shows the frequency-domain performance of each 14.8" channel.

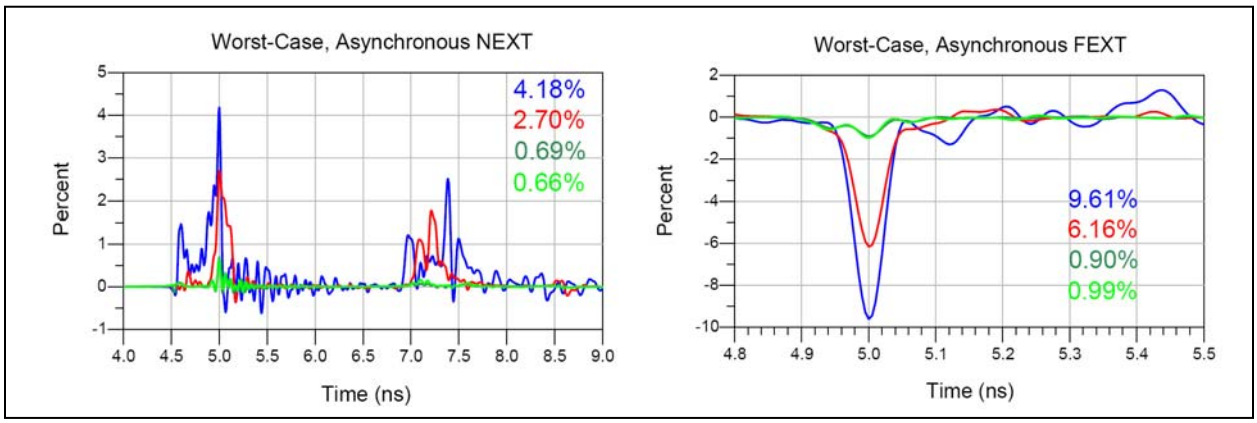


Figure 6: 14.8" System Comparison Data – TDR Stimulus (20ps rise time, 20-80%)
(Gen1 100 Ω=Blue, Gen2 100 Ω=Red, Gen3 100 Ω=Green, Gen3 85 Ω=Lime)

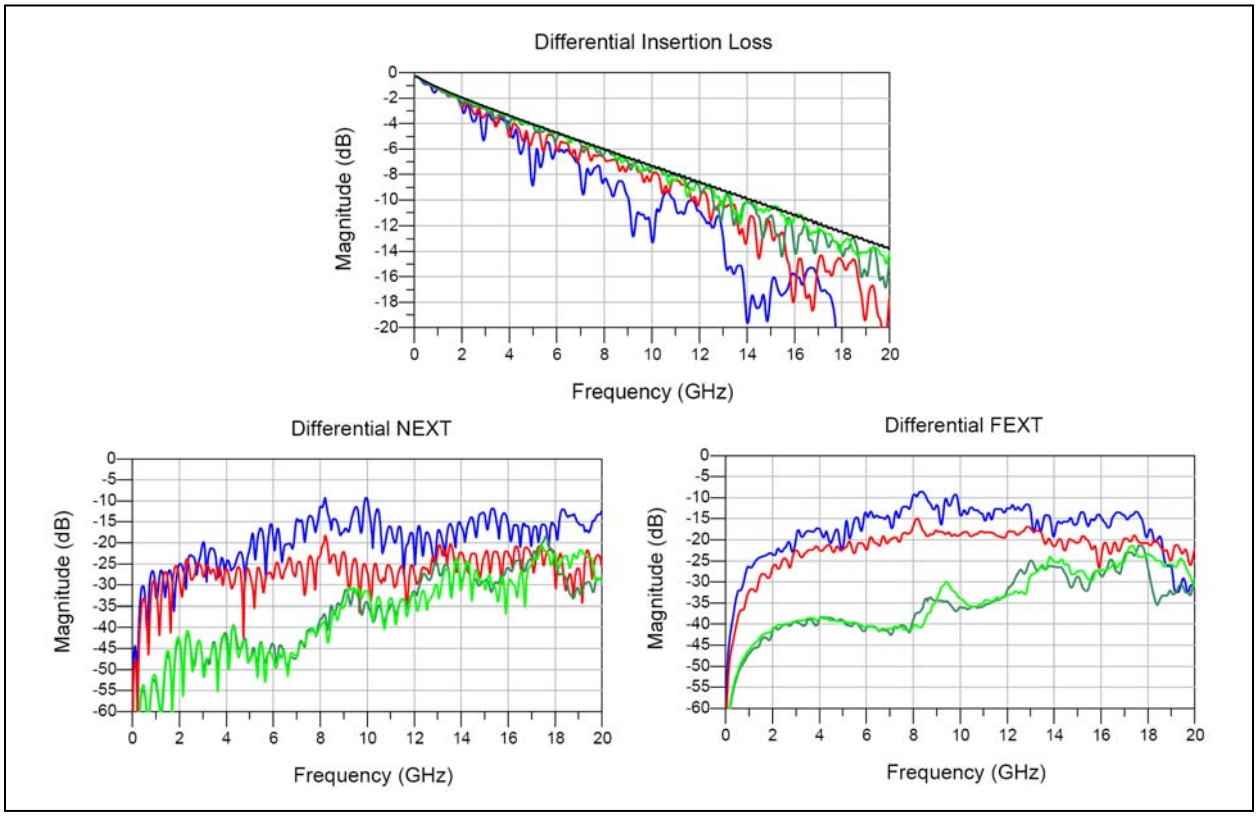


Figure 7: 14.8" System Comparison Data – S-parameters
(Gen1 100 Ω=Blue, Gen2 100 Ω=Red, Gen3 100 Ω=Green, Gen3 85 Ω=Lime)

As expected, Figure 6 shows damped NEXT due to the 3" of trace between the driver and the connector noise source. Also, although FEXT from two connectors in the system adds, Figure 6 shows a total FEXT that is damped due to the loss of the system traces. Figure 7 then shows frequency-domain performance with trace loss and connector-to-connector interaction effects.

Figure 8, shown below, highlights the effect of the four connector (and footprint) models on the 25 Gbps data throughput of the 14.8" channel that uses 2-tap pre-emphasis. Note that Figure 8 shows throughput-only data, without the effect of connector (and footprint) NEXT or FEXT.

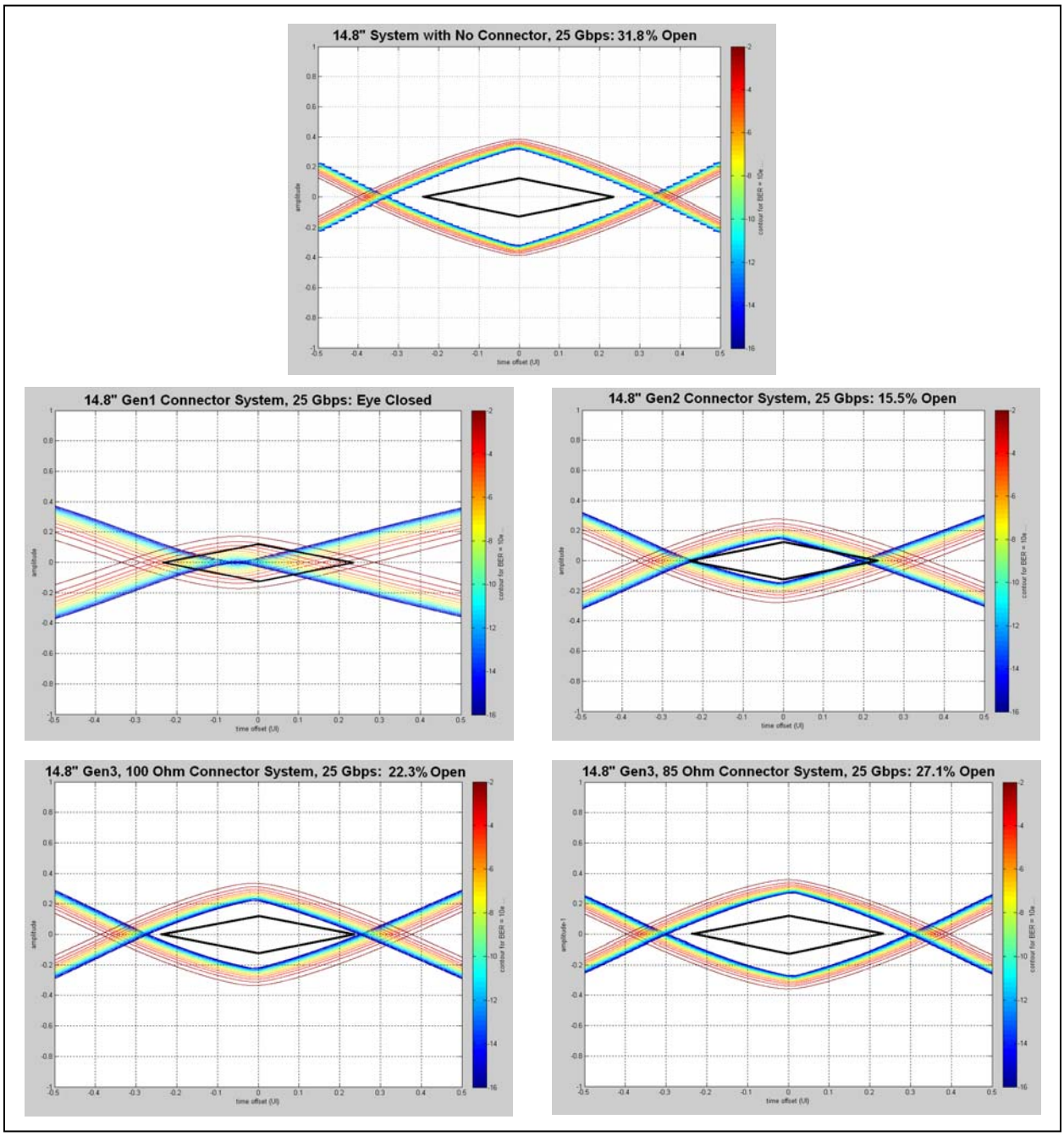


Figure 8: 14.8" System Comparison Data – 25 Gbps Eye Patterns (2-tap Pre-emphasis)

It is immediately clear in Figure 8 that the Gen1 connector (and footprints) do not perform well enough electrically to allow 25 Gbps data transmission. Even though the baseline system eye pattern is over 31% open, the impedance discontinuities of the Gen1 connector (and footprints) cause complete eye closure at 25 Gbps. Although the Gen2 connector improves the 25 Gbps eye pattern, it still fails the receiver mask at 25 Gbps. Ultimately, the Gen3, 100 Ω connector (in 100 Ω system) and the Gen3, 85 Ω connector (in 85 Ω system) both allow successful 25 Gbps transmission for a 14.8" system when no NEXT or FEXT is included.

The next step is to examine each connector (and footprint) channel performance when full NEXT is present or when full FEXT is present. To do this, Stateye 4.2.3 calculates noise addition both within the pulse response and between aggressors statistically. Further, all noise is calculated in a correlated manner, meaning that aggressor noise is time-aligned with the throughput pulse response. Although this statistical and correlated noise calculation is not absolute worst-case performance, it appears to be relatively representative of the effect of system noise. Further, assuming single-source clock triggering for driver chips, the noise correlation assumption should be fairly accurate. Note that Stateye 4.2.3 should equalize aggressor noise as it equalizes throughput signals, and it appears to do this sufficiently.

Table 1 shows all 14.8" 25 Gbps eye pattern simulation results. The first three rows of data give results for the eye patterns shown in Figure 8. The second three rows of data give eye pattern values when full NEXT is included, and the final three rows of data give eye pattern values when full FEXT is included. Note that all actual eye patterns are included in Appendix A.

	Base System	Gen1 System	Gen2 System	Gen3 System	Gen3 System
Throughput-Only:	100 Ω	100 Ω	100 Ω	100 Ω	85 Ω
Eye Opening:	31.8%	Closed	15.5%	22.3%	27.1%
P-P Jitter (10^-15):	0.36 UI	Closed	0.59 UI	0.48 UI	0.40 UI
Pass/Fail:	PASS	FAIL	FAIL	PASS	PASS
Throughput w/ NEXT:	Base 100	Gen1 100	Gen2 100	Gen3 100	Gen3 85
Eye Opening:	31.8%	Closed	8.5%	20.9%	25.6%
P-P Jitter (10^-15):	0.36 UI	Closed	0.69 UI	0.49 UI	0.42 UI
Pass/Fail:	PASS	FAIL	FAIL	PASS	PASS
Throughput w/ FEXT:	Base 100	Gen1 100	Gen2 100	Gen3 100	Gen3 85
Eye Opening:	31.8%	Closed	1.5%	20.9%	24.8%
P-P Jitter (10^-15):	0.36 UI	Closed	0.87 UI	0.49 UI	0.42 UI
Pass/Fail:	PASS	FAIL	FAIL	PASS	PASS

Table 1: 14.8" System 25 Gbps Eye Pattern Summary

It is clear from Table 1 that both Gen3 systems successfully transmit 25 Gbps signals, even in the presence of NEXT or FEXT. Of course, both the Gen1 and Gen2 systems had failed without the presence of noise, so the addition of noise doesn't change that.

It is interesting to note that the Gen3 eye patterns close with the introduction of NEXT by ~1.5%, even though the TDR plot of Figure 6 shows less than 0.7% total NEXT. Similarly, the introduction of FEXT in the Gen3 system causes up to 2.3% eye closure, even though the TDR plot of Figure 6 shows less than 1% total FEXT. There are two reasons for this increased eye closure. First, overall noise increases with increasing bit speed, as noise duration causes bit-to-bit noise growth. Second, although FIR pre-emphasis helps throughput, it also amplifies noise.

30.8" Channel Comparison Data

The next step is to examine the effect of inserting the four connectors (and footprints) into the 30.8" baseline system. Figure 9 shows the time-domain NEXT and FEXT of each 30.8" channel using a 20ps (20%-80%) TDR response. Figure 10 then shows the frequency-domain performance of each 30.8" channel.

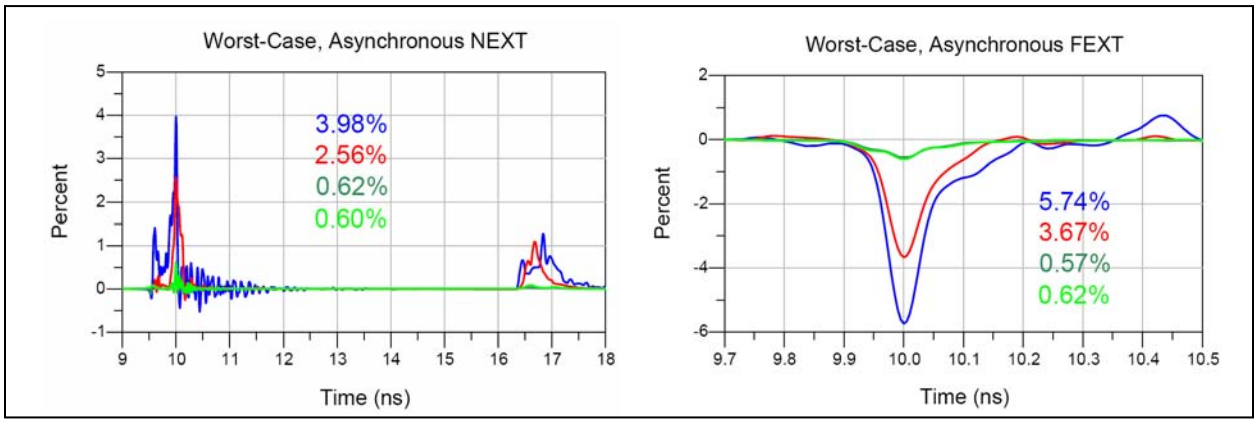


Figure 9: 30.8" System Comparison Data – TDR Stimulus (20ps rise time, 20-80%)
(Gen1 100 Ω=Blue, Gen2 100 Ω=Red, Gen3 100 Ω=Green, Gen3 85 Ω=Lime)

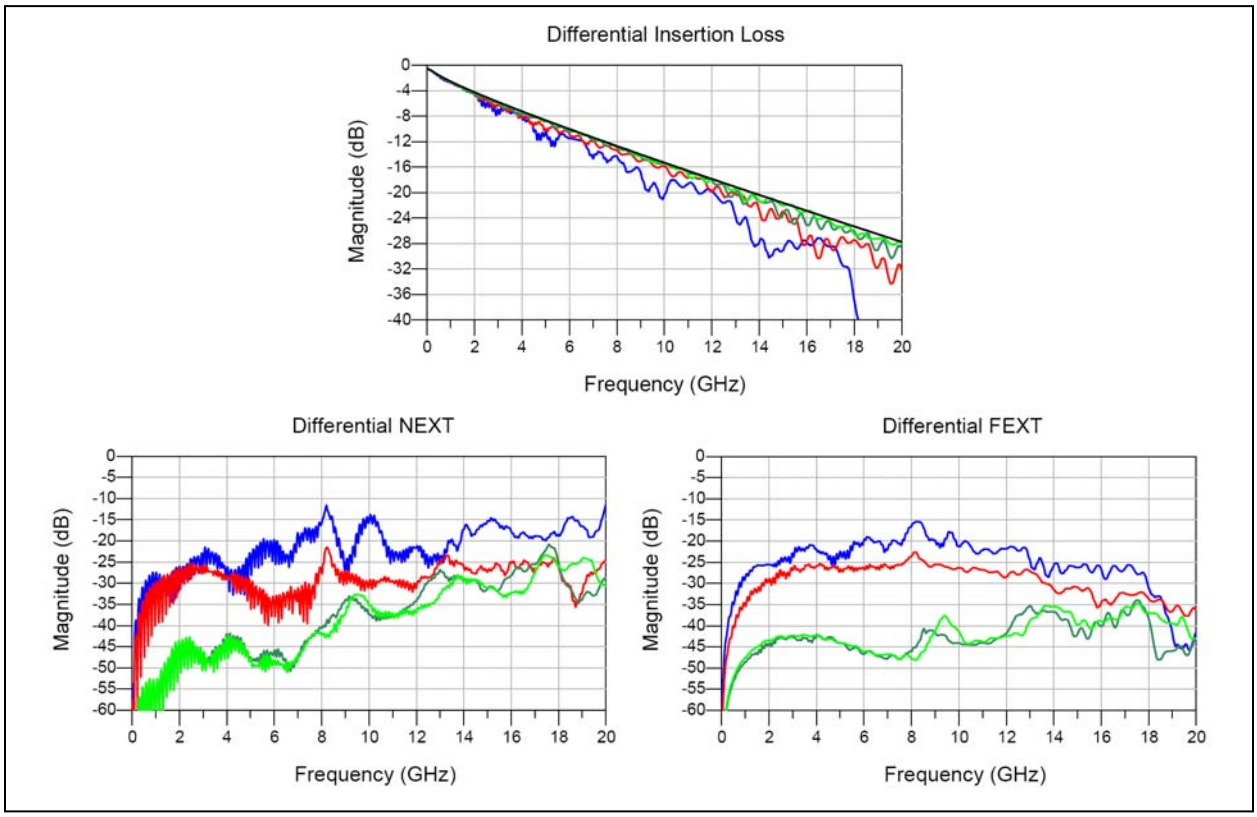


Figure 10: 30.8" System Comparison Data – S-parameters
(Gen1 100 Ω=Blue, Gen2 100 Ω=Red, Gen3 100 Ω=Green, Gen3 85 Ω=Lime)

As expected, Figure 9 shows damped NEXT due to the 4" of trace between the driver and the connector noise source. Also, although FEXT from two connectors in the system adds, Figure 9 shows a total FEXT that is damped due to the loss of the system traces. Figure 10 then shows frequency-domain performance with trace loss and connector-to-connector interaction effects.

Figure 11, shown below, highlights the effect of the four connector (and footprint) models on the 25 Gbps data throughput of the 30.8" channel that uses 5-tap pre-emphasis and 7-tap DFE equalization. The throughput-only data does not include the effects of NEXT or FEXT.

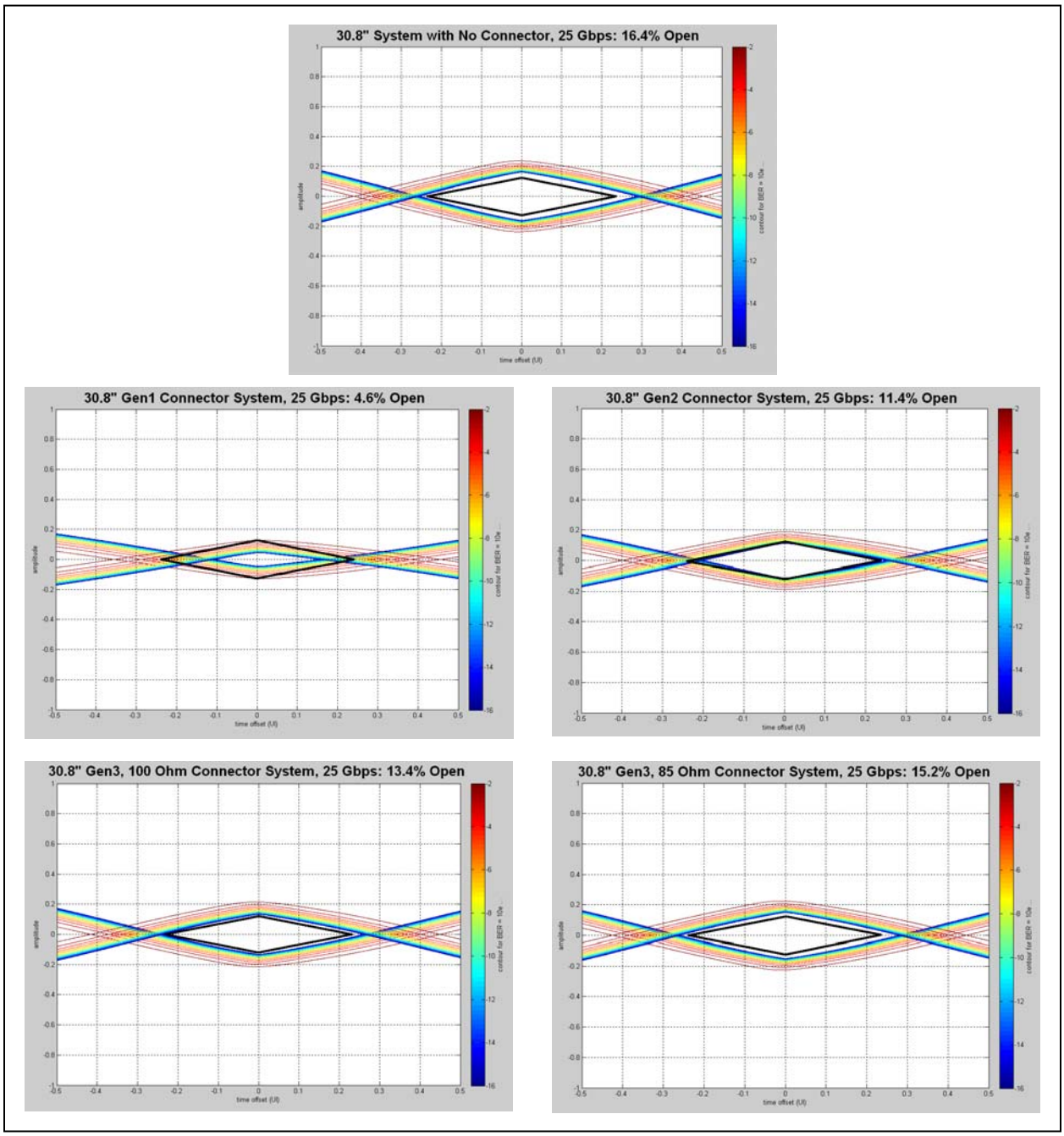


Figure 11: 30.8" System Comparison Data – 25 Gbps Eye Patterns (5-tap Pre-emphasis, 7-tap DFE)

It is immediately clear in Figure 11 that the Gen1 connector (and footprints) do not perform well enough electrically to allow 25 Gbps data transmission. Even though the baseline system eye pattern is over 16% open, the impedance discontinuities of the Gen1 connector (and footprints) cause the eye pattern to fail the receive mask at 25 Gbps. Although the Gen2 connector improves on the Gen1 eye pattern, it still fails the receive mask at 25 Gbps. Ultimately, the Gen3, 100 Ω connector (in 100 Ω system) and the Gen3, 85 Ω connector (in 85 Ω system) both allow successful 25 Gbps transmission for a 30.8" system when no NEXT or FEXT is included.

The next step is to examine each connector (and footprint) channel performance when full NEXT is present or when full FEXT is present. Table 2 shows all 30.8" 25 Gbps eye pattern simulation results. The first three rows of data give results for the eye patterns shown in Figure 11. The second three rows of data give eye pattern values when full NEXT is included, and the final three rows of data give eye pattern values when full FEXT is included. Note that all actual eye patterns are included in Appendix A.

	Base System	Gen1 System	Gen2 System	Gen3 System	Gen3 System
Throughput-Only:	100 Ω	100 Ω	100 Ω	100 Ω	85 Ω
Eye Opening:	16.4%	Closed	11.4%	13.4%	15.2%
P-P Jitter (10^-15):	0.44 UI	Closed	0.54 UI	0.50 UI	0.45 UI
Pass/Fail:	PASS	FAIL	FAIL	PASS	PASS
Throughput w/ NEXT:	Base 100	Gen1 100	Gen2 100	Gen3 100	Gen3 85
Eye Opening:	16.4%	Closed	6.7%	11.9%	14.1%
P-P Jitter (10^-15):	0.44 UI	Closed	0.65 UI	0.52 UI	0.48 UI
Pass/Fail:	PASS	FAIL	FAIL	FAIL	PASS
Throughput w/ FEXT:	Base 100	Gen1 100	Gen2 100	Gen3 100	Gen3 85
Eye Opening:	16.4%	Closed	6.4%	13.2%	14.9%
P-P Jitter (10^-15):	0.44 UI	Closed	0.69 UI	0.50 UI	0.47 UI
Pass/Fail:	PASS	FAIL	FAIL	PASS	PASS

Table 2: 30.8" System 25 Gbps Eye Pattern Summary

It is clear from Table 2 that both Gen3 systems successfully transmit 25 Gbps signals, even in the presence of full FEXT. In the presence of full NEXT, the Gen3, 100 Ω system barely fails the receiver eye mask, while the Gen3, 85 Ω system passes. Of course, both the Gen1 and Gen2 systems had failed without the presence of noise, so the addition of noise doesn't change that.

It is interesting to note that the Gen3 eye patterns close with the introduction of NEXT by ~1.5%, even though the TDR plot of Figure 9 shows less than 0.62% total NEXT. Again, there are two reasons for this increased eye closure. First, overall noise increases with increasing bit speed, as noise duration causes bit-to-bit noise growth. Second, although FIR pre-emphasis helps throughput, it also amplifies noise.

Interestingly, the introduction of FEXT into the Gen3 systems only causes ~0.3% eye closure, when Figure 9 shows 0.62% total FEXT. In this case, remember that Figure 9 shows worst-case asynchronous noise, where all aggressors are aligned to achieve a worst-case TDR noise figure. Stateye, on the other hand, adds noise in a correlated manner, so no time-shifting is done. As a result, in the case of the Gen3 systems with FEXT, bit-to-bit noise addition and noise amplification are not enough to offset the reduction in noise caused by the Stateye's correlated noise calculation over the TDR worst-case asynchronous noise calculation.

Summary

This paper has shown that noiseless systems with reflections only from low-capacitance chip parasitics can successfully transmit 25 Gbps signals across backplanes up to 30.8" in length with proper equalization. However, it has been shown that 25 Gbps signal transmission is difficult or impossible to achieve when Gen1 or Gen2 connectors, available from a number of vendors today, are inserted into the backplane systems. However, it has also been shown that more modern Gen3 connectors, now available from Tyco Electronics, have been designed to allow successful 25 Gbps signal transmission, even in the presence of full NEXT or FEXT.

Given the slightly aggressive system and simulation parameters chosen in this study, one can deduce connector (and footprint) performance guidelines necessary for successful 25 Gbps transmission. First, one can infer the lowest impedance tolerable by 100 Ω systems and then work to achieve this value in backplane footprints, where PCB via aspect ratio limits make achieving this value difficult. Second, one can examine connector (and footprint) TDR NEXT and FEXT numbers and figure out the values that will allow 25 Gbps transmission, even when bit-to-bit noise addition and noise amplification increase the base TDR values.

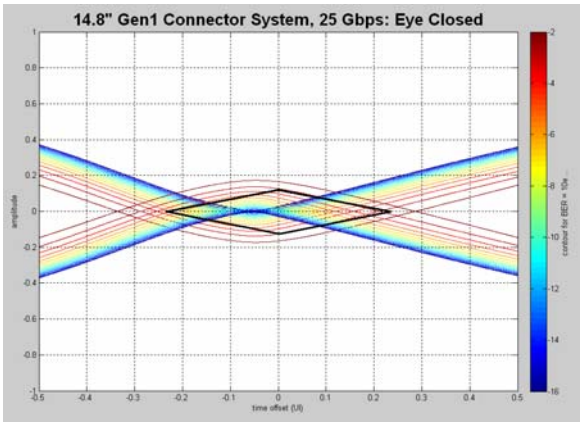
Of course, one can always choose better system parameters in order to decrease the performance requirements of the connectors (and footprints). For example, lower loss, less dispersive dielectric materials can be used. Also, improved equalization can be implemented with sub-baud-spaced intervals or more taps. However, the material and equalization values chosen in this paper are already aggressive for current backplane systems.

Ultimately, a system designer must be aware of difficulties that might be encountered in designing a 25 Gbps link. At 25 Gbps, the unit interval of a bit is only 40 ps, so any skew introduced by non-homogenous, woven-glass reinforced dielectrics or other sources will quickly cause the system to fail. Also, the jitter budget used in this paper for the transmitter, receiver, and clock data recovery (CDR) is only 12 ps peak-to-peak at BER=10^{-15}. This value, along with a maximum chip parasitic capacitance of 0.14 pF, may be challenging to achieve. Finally, although latest generation connectors (and footprints) create improved insertion loss-to-crosstalk ratios (ICR), as shown in Appendix B, one must be aware of the absolute value of insertion loss and crosstalk data, as ICR margin will do no good if all data is below the random noise floor.

There is little question that creating functional, dependable 25 Gbps backplane channels at usable lengths is a challenge. However, this paper makes it clear that the selection of next generation connectors (and footprints) is critical in helping to achieve this goal. There are numerous high-speed, high-density connectors available from Tyco Electronics and other companies today. However, at 25 Gbps, one needs to consider the use of premium connector (and footprint) performance in order to achieve successful link operation.

Appendix A: System Eye Pattern Results

14.8” System with Generation 1, 100 Ohm Differential Connector



FIR Settings:
- Tap 1 = +0.735937
- Tap 2 = -0.264063
- Tap 3 = Unused
- Tap 4 = Unused
- Tap 5 = Unused

DFE Settings:
- Tap 1 = Unused
- Tap 2 = Unused
- Tap 3 = Unused
- Tap 4 = Unused
- Tap 5 = Unused
- Tap 6 = Unused
- Tap 7 = Unused

Figure A1a: 14.8” Gen1, 100 Ohm System Performance – Throughput Only

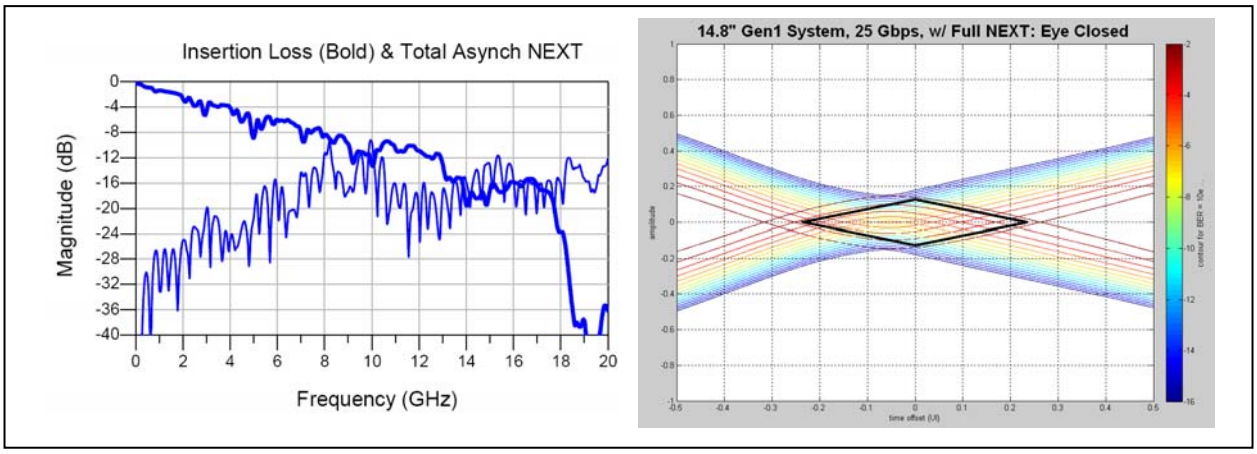


Figure A1b: 14.8” Gen1, 100 Ohm System Performance with Total NEXT

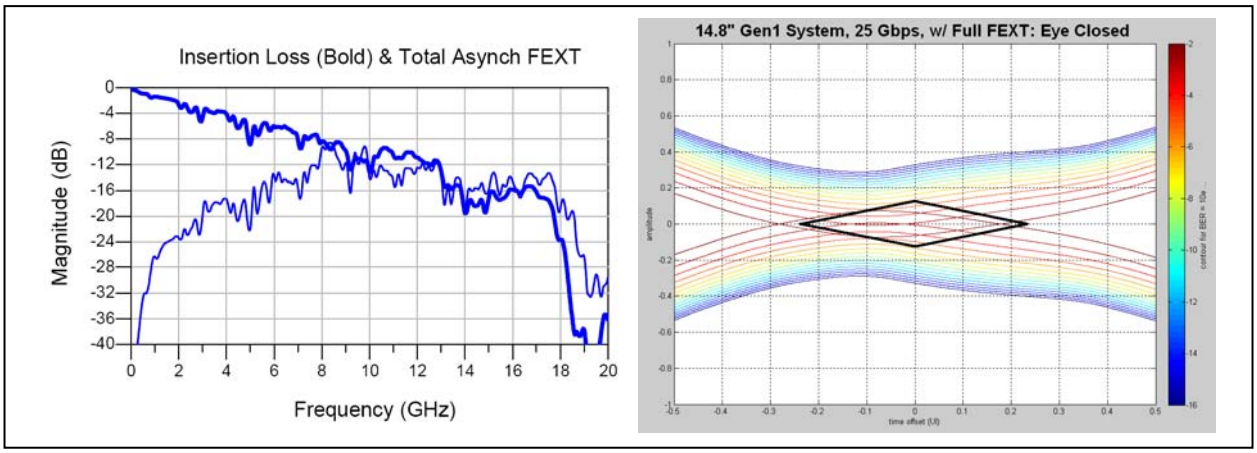
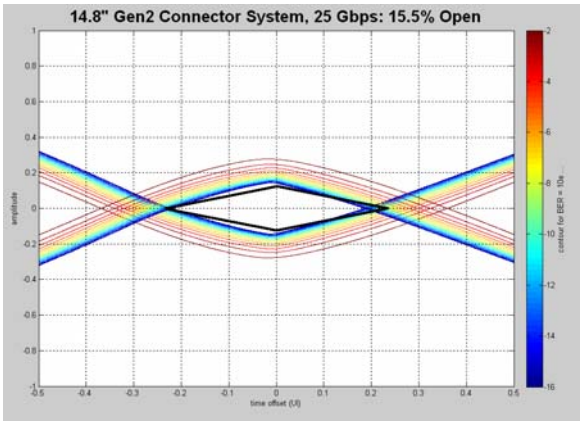


Figure A1c: 14.8” Gen1, 100 Ohm System Performance with Total FEXT

14.8” System with Generation 2, 100 Ohm Differential Connector



FIR Settings:
- Tap 1 = +0.79375
- Tap 2 = -0.20625
- Tap 3 = Unused
- Tap 4 = Unused
- Tap 5 = Unused

DFE Settings:
- Tap 1 = Unused
- Tap 2 = Unused
- Tap 3 = Unused
- Tap 4 = Unused
- Tap 5 = Unused
- Tap 6 = Unused
- Tap 7 = Unused

Figure A2a: 14.8” Gen2, 100 Ohm System Performance – Throughput Only

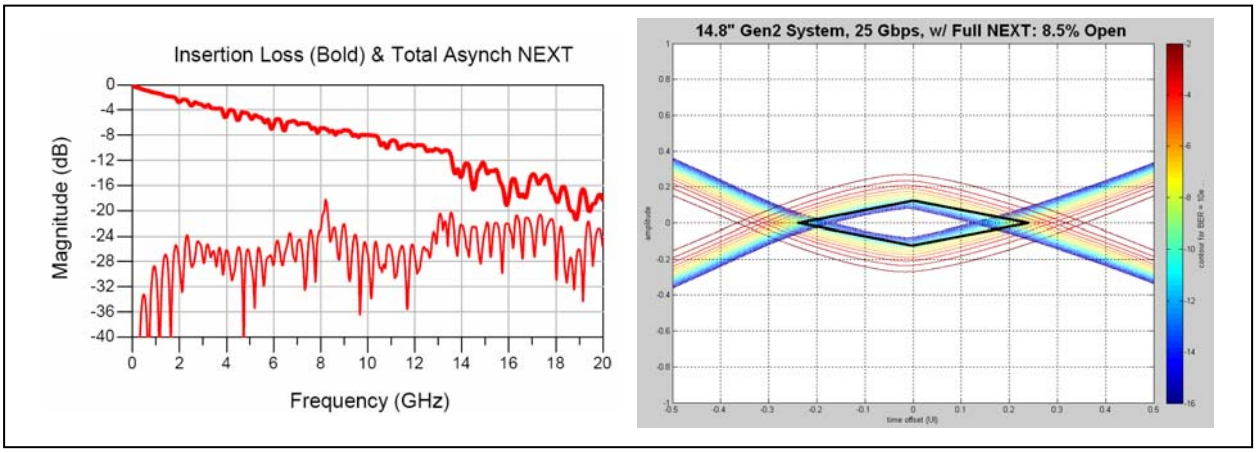


Figure A2b: 14.8” Gen2, 100 Ohm System Performance with Total NEXT

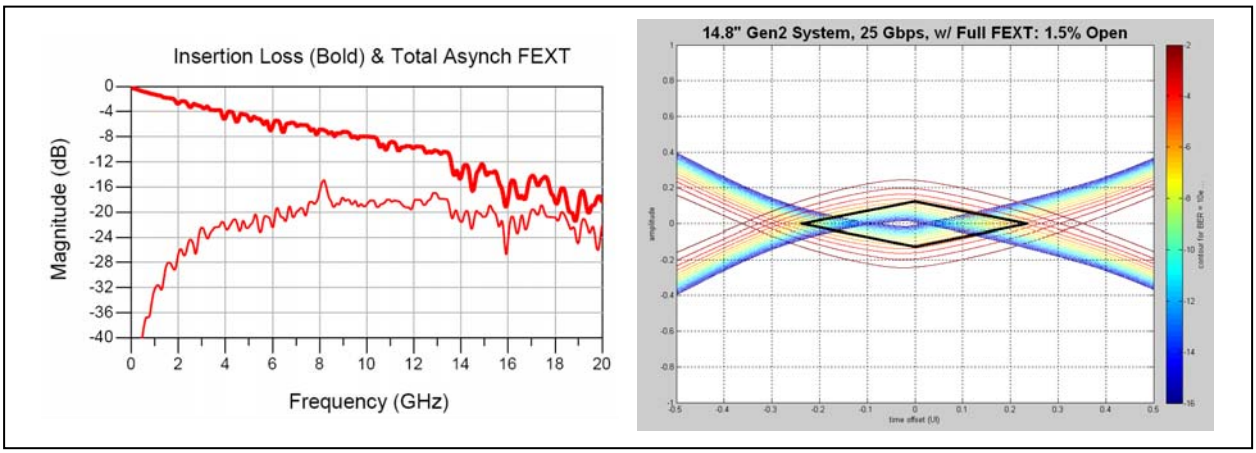
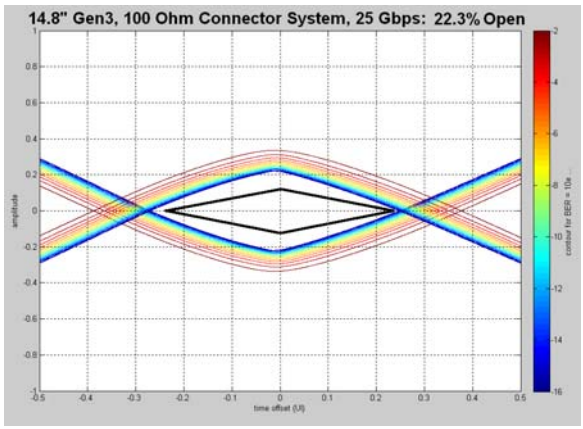


Figure A2c: 14.8” Gen2, 100 Ohm System Performance with Total FEXT

14.8” System with Generation 3, 100 Ohm Differential Connector



FIR Settings:
- Tap 1 = +0.80625
- Tap 2 = -0.19375
- Tap 3 = Unused
- Tap 4 = Unused
- Tap 5 = Unused

DFE Settings:
- Tap 1 = Unused
- Tap 2 = Unused
- Tap 3 = Unused
- Tap 4 = Unused
- Tap 5 = Unused
- Tap 6 = Unused
- Tap 7 = Unused

Figure A3a: 14.8” Gen3, 100 Ohm System Performance – Throughput Only

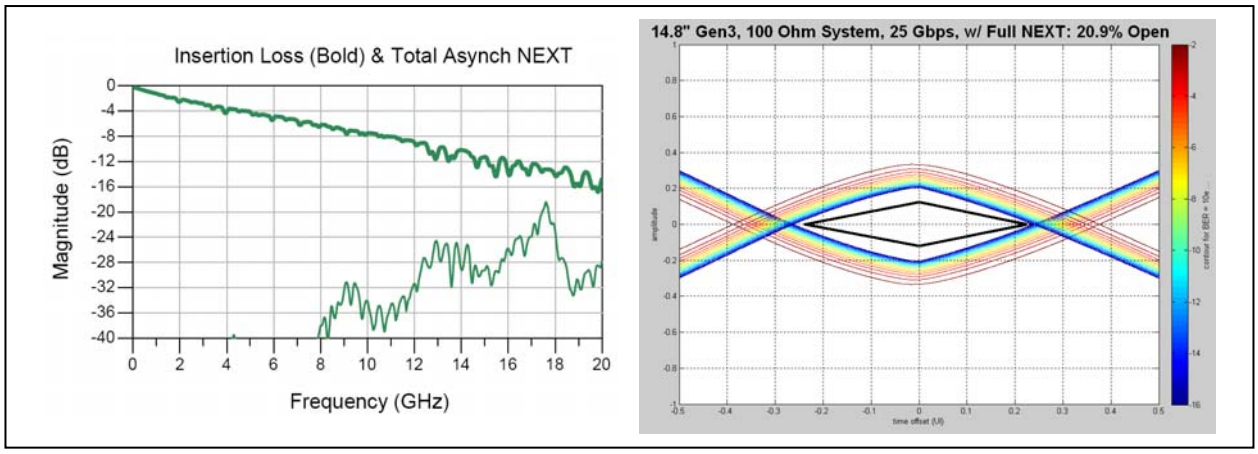


Figure A3b: 14.8” Gen3, 100 Ohm System Performance with Total NEXT

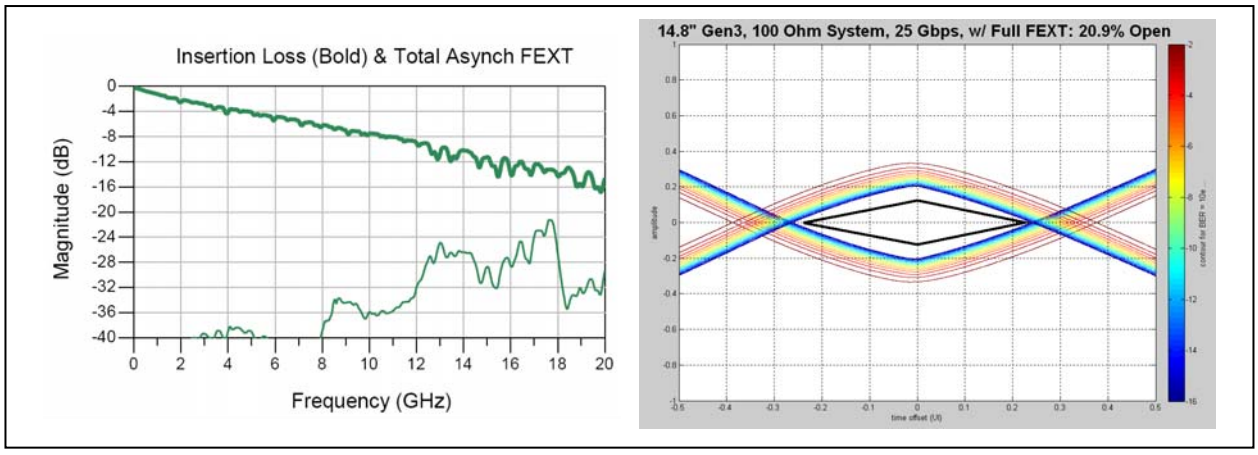
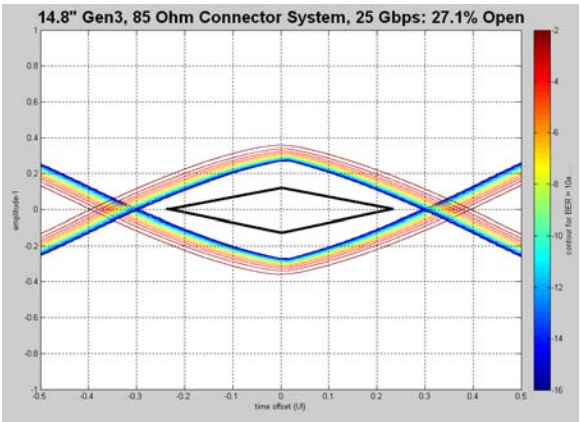


Figure A3c: 14.8” Gen3, 100 Ohm System Performance with Total FEXT

14.8” System with Generation 3, 85 Ohm Differential Connector



FIR Settings:
- Tap 1 = +0.80625
- Tap 2 = -0.19375
- Tap 3 = Unused
- Tap 4 = Unused
- Tap 5 = Unused

DFE Settings:
- Tap 1 = Unused
- Tap 2 = Unused
- Tap 3 = Unused
- Tap 4 = Unused
- Tap 5 = Unused
- Tap 6 = Unused
- Tap 7 = Unused

Figure A4a: 14.8” Gen3, 85 Ohm System Performance – Throughput Only

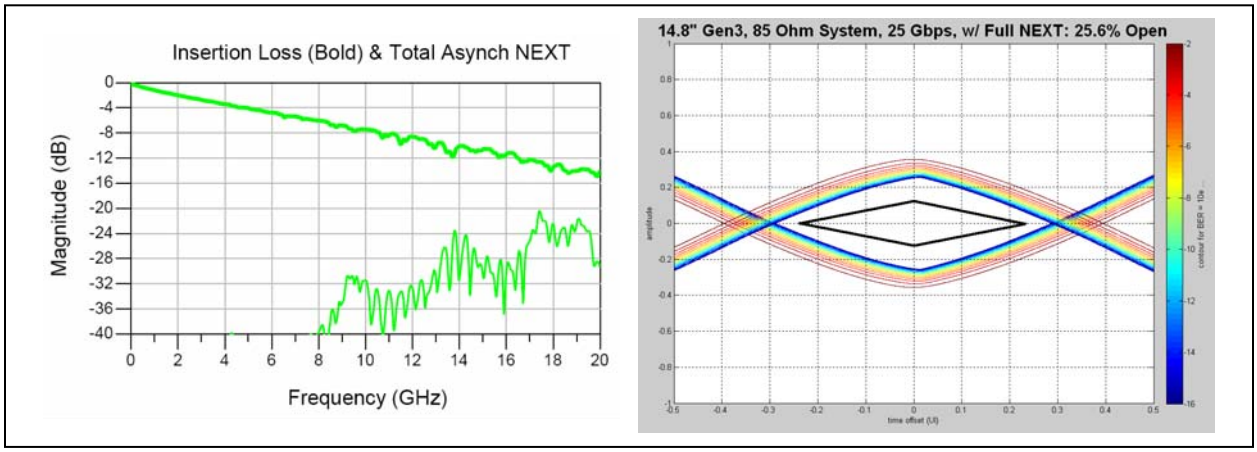


Figure A4b: 14.8” Gen3, 85 Ohm System Performance with Total NEXT

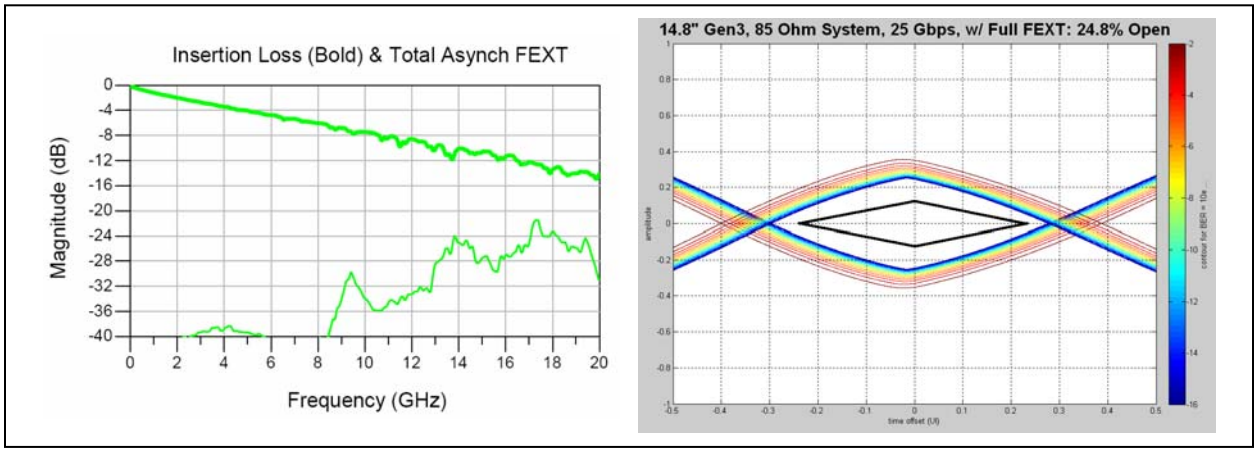
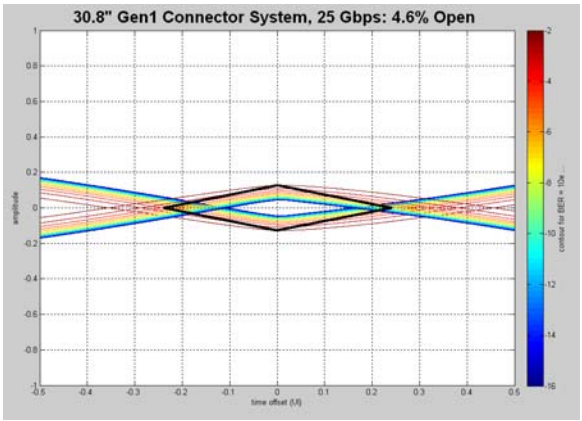


Figure A4c: 14.8” Gen3, 85 Ohm System Performance with Total FEXT

30.8” System with Generation 1, 100 Ohm Differential Connector



FIR Settings:
- Tap 1 = +0.0133342
- Tap 2 = -0.0973341
- Tap 3 = +0.789292
- Tap 4 = -0.0641899
- Tap 5 = -0.0358495

DFE Settings:
- Tap 1 = 0.136708
- Tap 2 = 0.065991
- Tap 3 = 0.035945
- Tap 4 = 0.028280
- Tap 5 = 0.013896
- Tap 6 = 0.010913
- Tap 7 = 0.011889

Figure A5a: 30.8” Gen1, 100 Ohm System Performance – Throughput Only

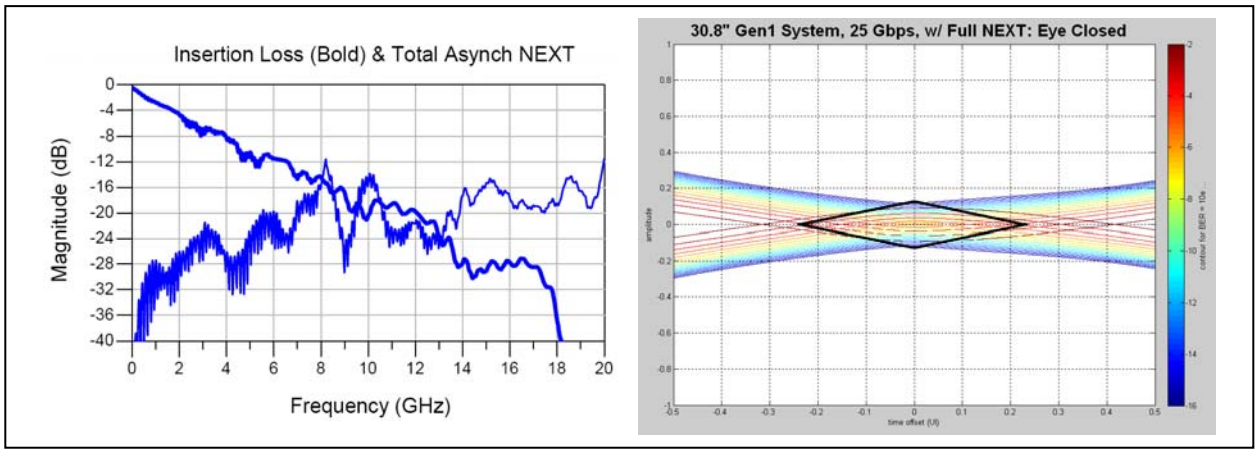


Figure A5b: 30.8” Gen1, 100 Ohm System Performance with Total NEXT

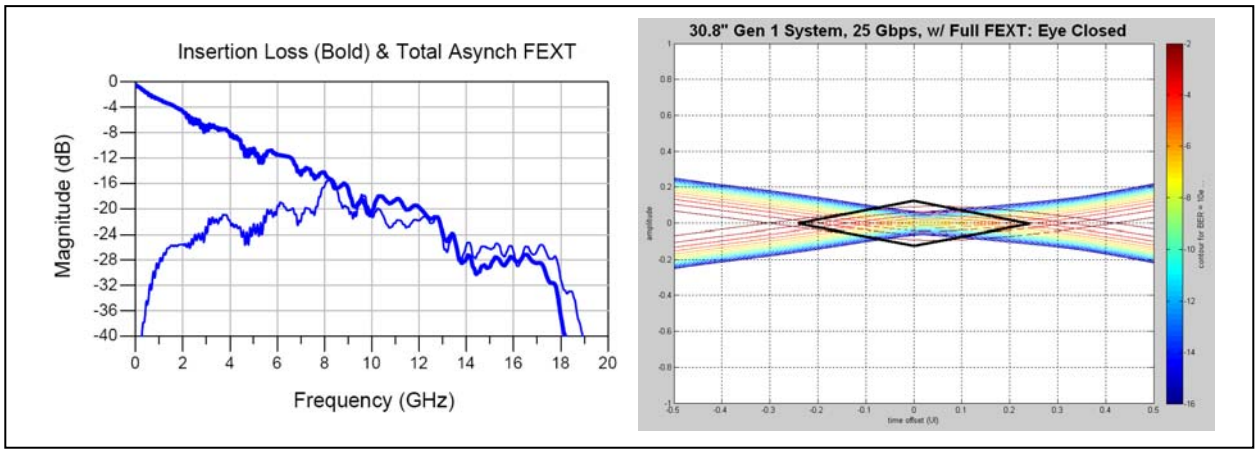
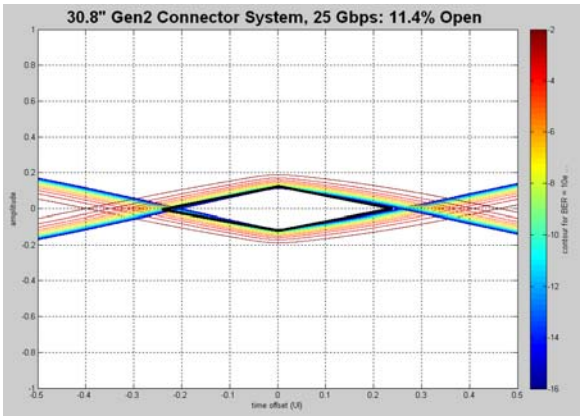


Figure A5c: 30.8” Gen1, 100 Ohm System Performance with Total FEXT

30.8” System with Generation 2, 100 Ohm Differential Connector



FIR Settings:
- Tap 1 = +0.000052
- Tap 2 = -0.068233
- Tap 3 = +0.892603
- Tap 4 = -0.016269
- Tap 5 = -0.228420

DFE Settings:
- Tap 1 = 0.17154
- Tap 2 = 0.08271
- Tap 3 = 0.05128
- Tap 4 = 0.03515
- Tap 5 = 0.02202
- Tap 6 = 0.01497
- Tap 7 = 0.01290

Figure A6a: 30.8” Gen2, 100 Ohm System Performance – Throughput Only

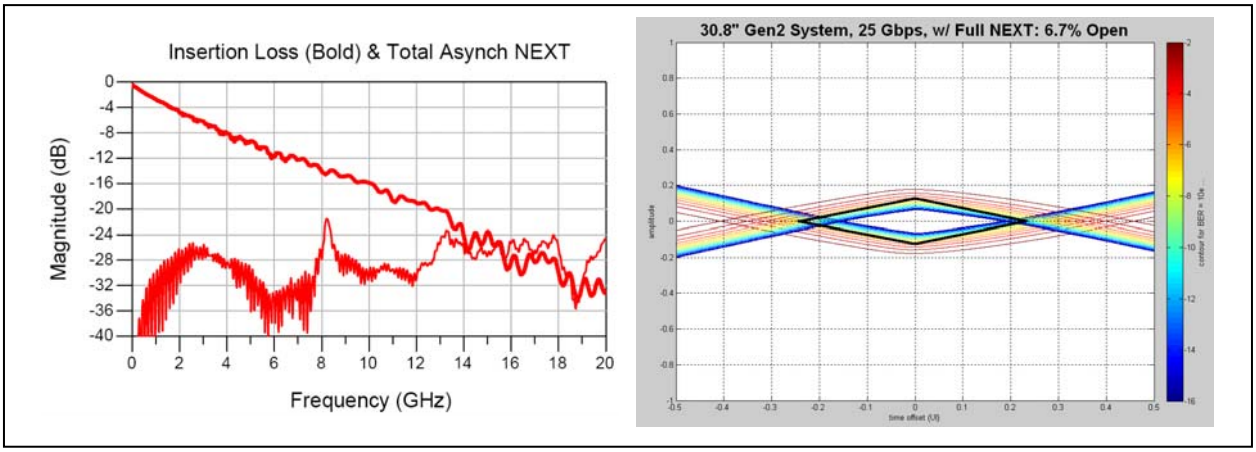


Figure A6b: 30.8” Gen2, 100 Ohm System Performance with Total NEXT

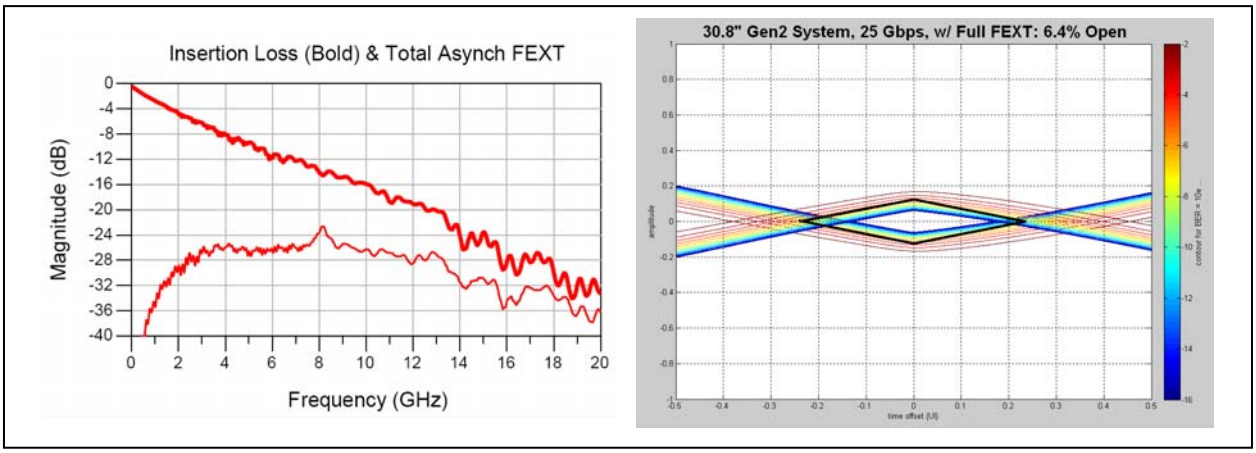
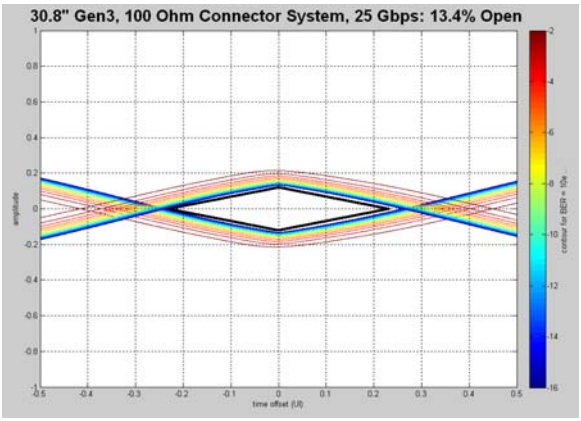


Figure A6c: 30.8” Gen2, 100 Ohm System Performance with Total FEXT

30.8” System with Generation 3, 100 Ohm Differential Connector



FIR Settings:
- Tap 1 = -0.000819
- Tap 2 = -0.271072
- Tap 3 = +0.948993
- Tap 4 = -0.008098
- Tap 5 = -0.014982

DFE Settings:
- Tap 1 = 0.194531
- Tap 2 = 0.089561
- Tap 3 = 0.053578
- Tap 4 = 0.036108
- Tap 5 = 0.025762
- Tap 6 = 0.016928
- Tap 7 = 0.014662

Figure A7a: 30.8” Gen3, 100 Ohm System Performance – Throughput Only

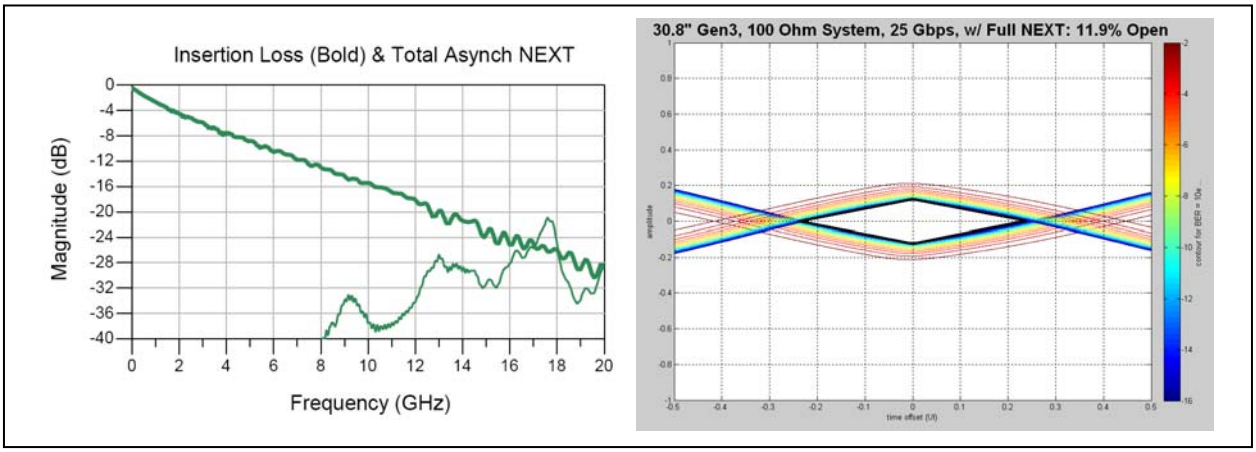


Figure A7b: 30.8” Gen3, 100 Ohm System Performance with Total NEXT

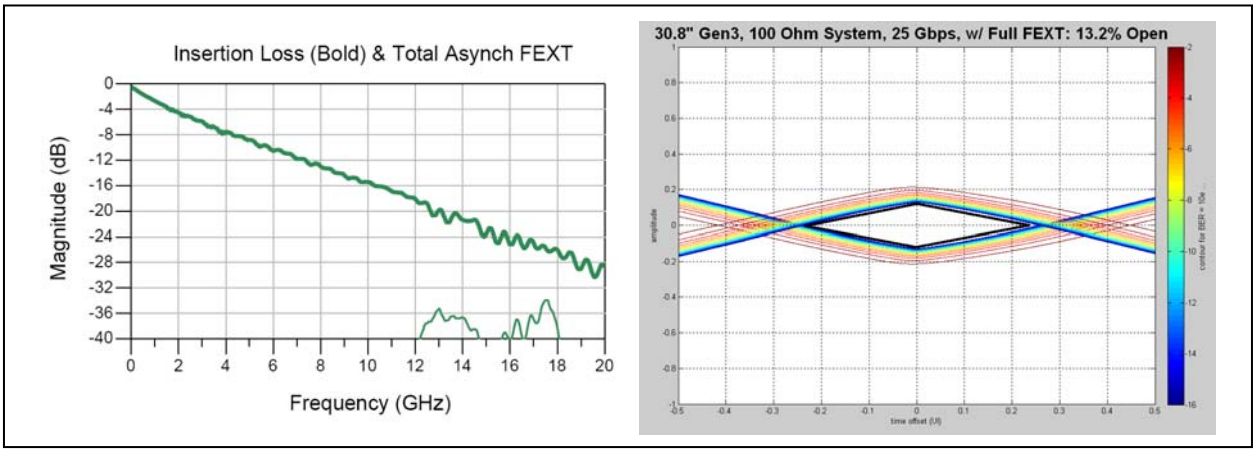
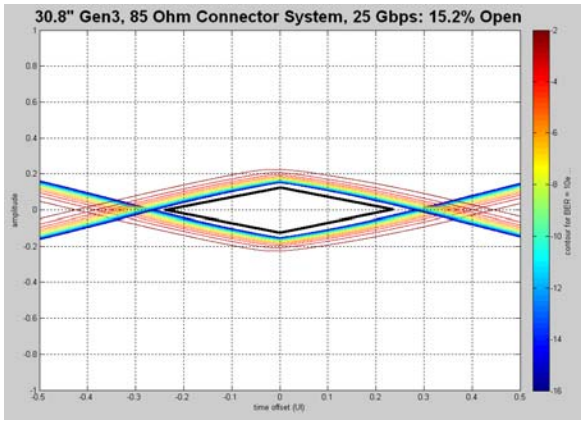


Figure A7c: 30.8” Gen3, 100 Ohm System Performance with Total FEXT

30.8” System with Generation 3, 85 Ohm Differential Connector



FIR Settings:
- Tap 1 = -0.001739
- Tap 2 = -0.020144
- Tap 3 = +0.955654
- Tap 4 = -0.002633
- Tap 5 = -0.019830

DFE Settings:
- Tap 1 = 0.203672
- Tap 2 = 0.091477
- Tap 3 = 0.052330
- Tap 4 = 0.033882
- Tap 5 = 0.023578
- Tap 6 = 0.017058
- Tap 7 = 0.013156

Figure A8a: 30.8” Gen3, 85 Ohm System Performance – Throughput Only

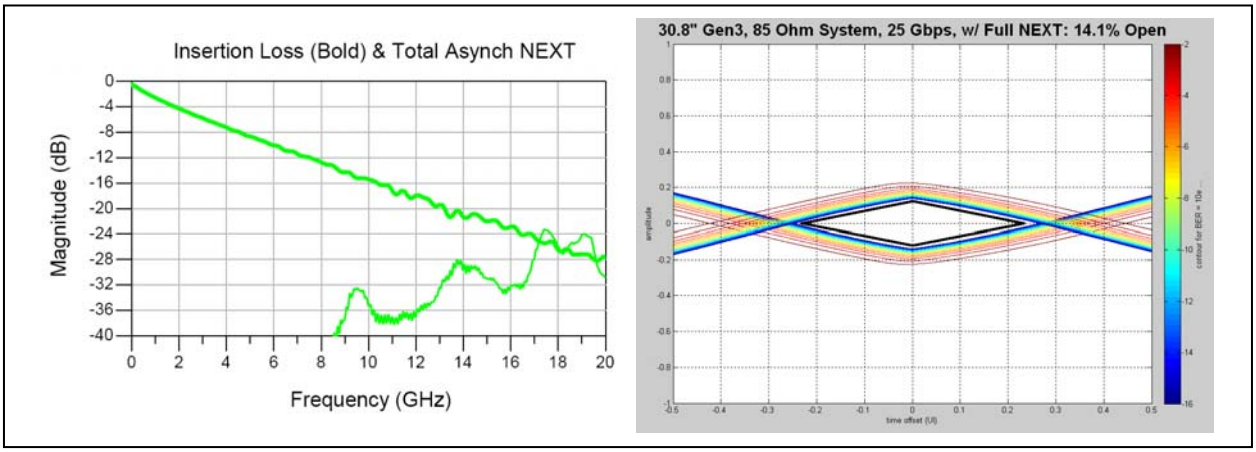


Figure A8b: 30.8” Gen3, 85 Ohm System Performance with Total NEXT

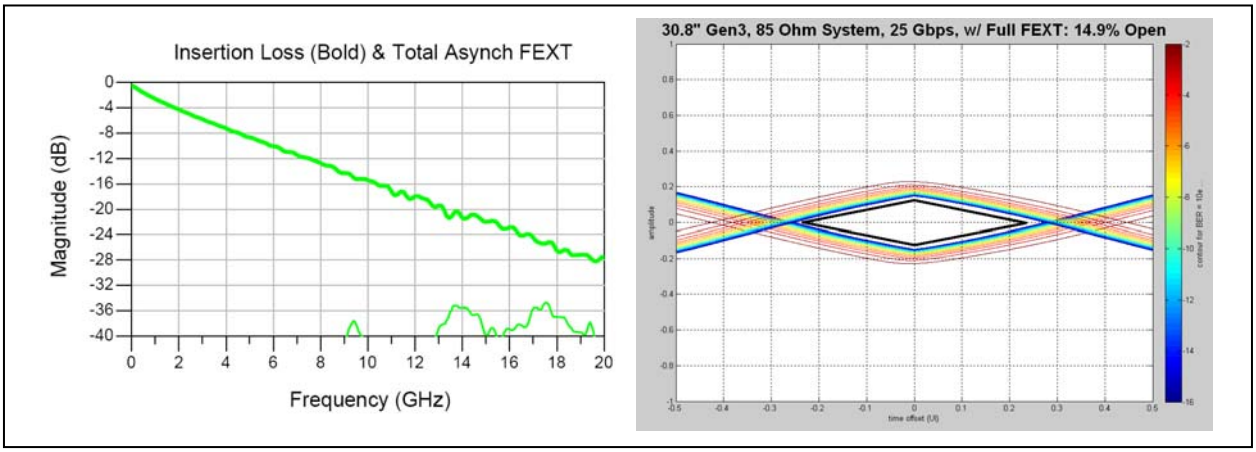


Figure A8c: 30.8” Gen3, 85 Ohm System Performance with Total FEXT

Appendix B: Insertion Loss-to-Crosstalk Ratio Comparison

This appendix includes insertion loss-to-crosstalk ratio (ICR) comparison plots for various systems. The four 14.8" connector (and footprint) systems are compared using both full NEXT and full FEXT. Similarly, the four 30.8" connector (and footprint) systems are also compared.

Note that ICR is calculated as the difference between differential insertion loss (in dB) and the total NEXT or FEXT (in dB). In this case, total NEXT and FEXT values for various systems are calculated by adding the *magnitudes* of all aggressors (not using root sum of squares - RSS). An example calculation of the ICR calculation is as follows:

$$ICR = Insertion\ Loss\ (in\ dB) - Total\ Noise\ (in\ dB) = (-16dB) - (-30dB) = 14\ dB$$

All ICR calculations below are taken from the frequency-domain plots in Appendix A. Notice the distinct improvement in ICR from Gen1 connectors (and footprints) to Gen3 connectors (and footprints). Also, notice that there is little change in ICR between short and long systems. This is because noise is damped by trace loss as throughput is damped. Ultimately, however, one must be careful using ICR alone as a metric, as modern equalization is not perfect and random noise exists in systems. Therefore, absolute values of loss and noise are also important.

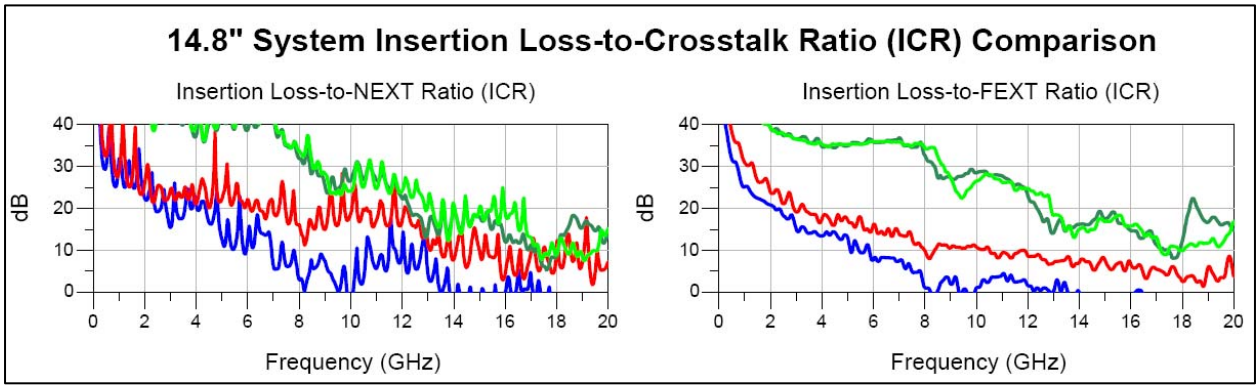


Figure B1: 14.8" NEXT and FEXT ICR Comparison
(Gen1 100 Ω=Blue, Gen2 100 Ω=Red, Gen3 100 Ω=Green, Gen3 85 Ω=Lime)

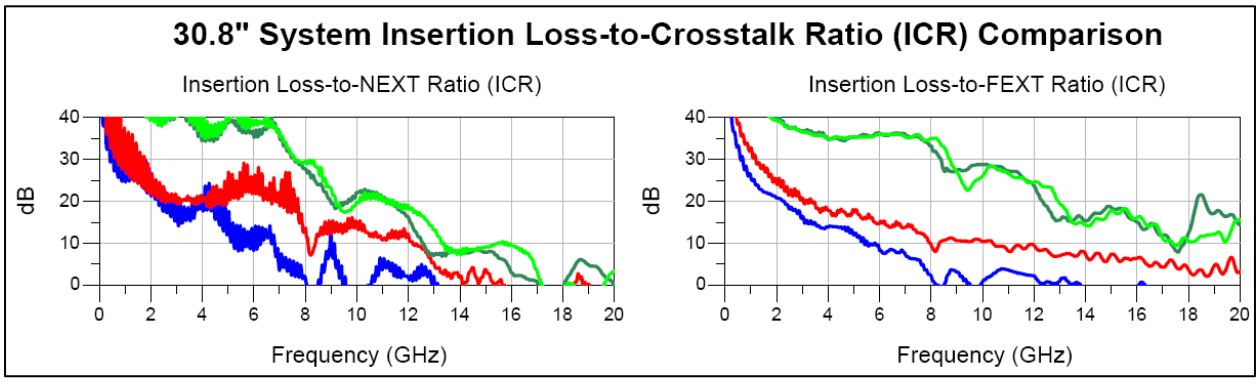


Figure B1: 30.8" NEXT and FEXT ICR Comparison
(Gen1 100 Ω=Blue, Gen2 100 Ω=Red, Gen3 100 Ω=Green, Gen3 85 Ω=Lime)

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