Fast Acting Over Current Power Circuit Protection Scheme

Abstract

A power circuit protection scheme is presented which utilizes a fast acting, digital output, Hall effect based over current detector. The scheme combines a pulse by pulse current limit with a pulse count shutdown. The pulse by pulse current limit provides a fast acting shutdown. The pulse count shutdown acts to distinguish a normal over current event from a hard failure, and latch off the circuit in the case of a hard failure. The effectiveness of the scheme is demonstrated by application to a low inductance power MOSFET circuit. In this demonstration circuit, a MOSFET is connected directly across a DC power source. A very fast rising, high current (comparable to a shoot through current on a bridge circuit) is generated when the MOSFET is turned on. Waveforms are presented showing the current, detector output, gate drive, and MOSFET switching waveforms.

Introduction

This paper presents a robust method for active over current protection in power electronic circuits. The method eliminates failures in power electronic circuits by protecting power transistors and other power semiconductors against over current events. It actively distinguishes between temporary events often caused by transient load conditions such as motor starting, and hard events caused by internal circuit failures or output load shorts. In both cases, the method prevents circuit failure by providing a fast acting pulse by pulse shutdown of power transistors. For temporary events, the circuit simply rides through the event on a pulse by pulse basis and returns to normal operation when the condition has cleared. When the event is hard, the circuit acts to latch off the power circuit to prevent any failure caused by continued power circuit operation.

While this method can be incorporated using a variety of over current detection techniques, the key to its effectiveness is using a fast acting, noise immune, digital output Hall effect over current detector. This detector is a simple low cost implementation of the widely used Hall effect current sensing technique. The detector reacts in 1 μs, is highly immune to the noise prevalent in power switching circuits, and provides isolation allowing current to be detected at different voltage levels.

The method is demonstrated with a circuit using a MOSFET operating into a direct short. The circuit is designed to demonstrate the operation of the protection scheme while operating under this worst case operating condition. The operation of this circuit is explained and operating waveforms are presented.

Over Current Detector Description

When engineers consider incorporating over current protection into their circuits, one of the first considerations is the technique to detect the over current condition. Among the popular techniques are current sense transformers, Hall effect current sensors, current sensing resistors, and de-sat sensing on power transistors. For each method, the engineer is faced with trade-offs between cost, size, simplicity, isolation, noise immunity, power dissipation and robustness. The scheme featured in this paper uses a digital output Hall effect over current detector (OCD) to detect the over current condition.

This detector, designed and manufactured by E-T-A, is fully integrated with its output factory programmed to go low at a specific input current level. It is designed to be mounted directly to a printed circuit board and like other Hall effect current sensors, provides isolation between the sensed current and the output. The OCD's unique digital output provides a fast response time (1 μs) and a high level of noise immunity. These features are critical to obtaining the robust protection provided by the implementation described here. Fast response time is important for two reasons:

1.) The quicker an over current event is detected, the sooner a transistor shutdown can be initiated. This is important due to the various propagation delays present in a shutdown caused by control logic and transistor drive circuits, and the transistor short circuit current ratings which are often 10 μs. By utilizing a fast response detector, sufficient margin can be maintained between the worst case shutdown time and the short circuit capability of the transistor.

2.) Parasitic inductances can become destructive in high current paths with slower response times. These inductaces store significant energy, particularly under high current conditions. The energy stored is proportional to the square of the current and this energy must be dealt with at the time

of the shutdown. In some cases, the circuit topology provides a commutating path that safely manages this energy. In other cases, the energy is dissipated in snubbers or through transistor avalanche at shutdown. In all cases, the energy present at the time of detection is dramatically higher with a detector having a 3 μs response time instead of a 1 μs response time. This energy can cause failure particularly when operating in a repetitive pulse by pulse current limiting mode. Using a fast response OCD minimizes this energy.

The arguments presented for the importance of response time also apply to noise immunity. Filtering must be added to techniques that provide less immunity. This filtering slows the response time - reducing shutdown margin time and increasing the parasitic energy that must be dealt with at shutdown. This same problem is typically encountered when utilizing a detection scheme that converts an analog sense signal to a digital over current signal. This method would be required with a linear Hall effect current sensor, current sense transformer, or current sense resistor. The digital output Hall effect technique provides excellent noise immunity and eliminates the need for any significant filtering which would slow the response of the detector circuit.

An E-T-A TD Series OCD provides a simple interface to the circuit, having both an input side and an output side. The current to be sensed is passed though the input side of the detector. The output side has three connections. Two of the connections are used to provide logic power to the detector, typically 5 to 12 VDC. This supply must be properly decoupled in order to ensure noise immunity and fast response time. The third output connection is a simple open collector pin. A 4.7 kΩ resistor is used to pull the pin high. The detector forces the pin low when a current exceeding the trip level of the detector is passed through the input.

Protection Scheme

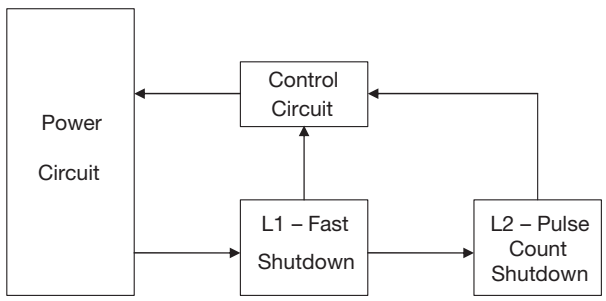
A functional block diagram for the protection scheme is shown in Figure 1. The implementation uses two levels of shutdown:

1.) Fast response pulse by pulse shutdown. This level is designed to provide a quick response without distinguishing between temporary and hard events.

2.) Pulse count shutdown. This level is designed to distinguish between transient and hard events, and latch off the power circuit in the case of a hard event.

In the demonstration circuit, the first level shutdown is implemented using a D flip-flop and a shutdown input to the gate drive circuit for the power MOSFET. This minimizes the propagation delay, providing a fast response shutdown. A microcontroller is used to implement the general control logic and second level shutdown in the demonstration circuit. An available pulse count input is used for the second level shutdown. Over

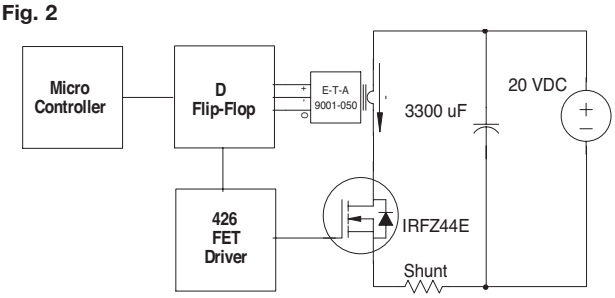
Fig. 1



current pulses are accumulated over a window of time. If a set count limit is exceeded before the window of time ends, the controller latches off the power MOSFET via the gate drive circuit. If the set count limit is not exceeded at the end of the time window, the count is reset to zero. The set count limit is designed to be set by the engineer, and should be set to distinguish between temporary and hard events. For instance, a motor starting may generate 100 over current pulses in a motor drive circuit. Setting the pulse count limit above the count achieved with all temporary events would distinguish temporary events from hard events.

Demonstration Circuit Description

Fig. 2



The circuit, shown in Figure 2 as a block schematic, can be split into two sections. The first section is the power or high current portion of the circuit. The second section is the control of logic section of the circuit. The power section consists of a 20 VDC power supply connected in series with an N-channel MOSFET, a shunt, and a 50 amp OCD. This circuit creates a short across the power supply when the MOSFET is turned on, creating a fast rising fault current. For this demonstration, a IRFZ44E is used for the MOSFET. This is a 60 volt, 48 amp, 23 mΩ device. It is considered to be representative of 40-60 amp, 60 volt MOSFET's which have been available for several years. The connections between the power supply and the rest of the circuit consists of 20 gage leads 8 inches long. In order to maximize the rise time of the short circuit current, a 3300 uF capacitor is included directly on the PCB. The total length of the power traces and leads in the demonstration circuit connecting the MOSFET to the capacitor and OCD is 5 inches.

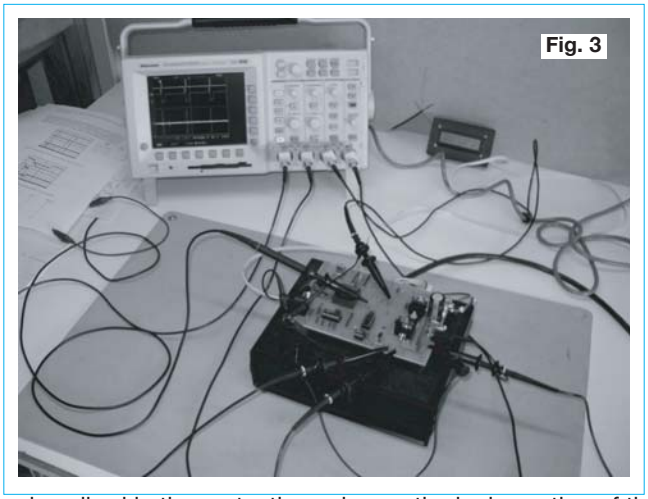


Fig. 3

As described in the protection scheme, the logic section of the circuit consists of a microcontroller driving the clock input of a D flip flop with the output of the flip flop driving a gate MOSFET gate driver. The output of the OCD is fed back to clear the flip-flop which turns the MOSFET gate drive off when an over current event is detected. Figure 3 displays the test set up.

Demonstration Circuit Waveforms

The MOSFET and OCD operating waveforms are shown in Figures 4 - 6 with the circuit operating at 30 kHz. In these plots, waveforms are numbered R1-R4 from the bottom to the top. Trace R1 is the gate to source voltage at 10 V/div. Trace R2 is the drain current measured by measuring the voltage across the 10 mΩ shunt at 1 volt/div (=100 amps/div). Trace R3 is the OCD output at 5 volts/div. Trace R4 is the drain to source voltage at 20 V/div.

Figure 4 is a low resolution view of the waveforms intended to show three successive turn on - shutdown sequences at 30 kHz. Figure 5 provides a view of one turn-on - shutdown sequence. The figures demonstrate the fast response of the OCD output and the turn off of the MOSFET within 1 μs of the fault current event. The shunt used for current measurement

Fig. 4

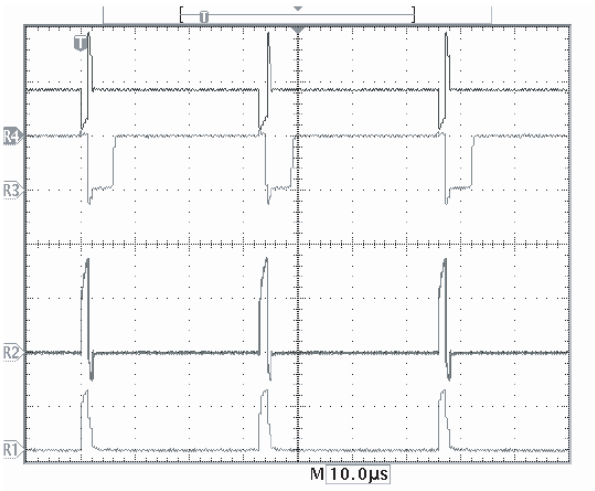
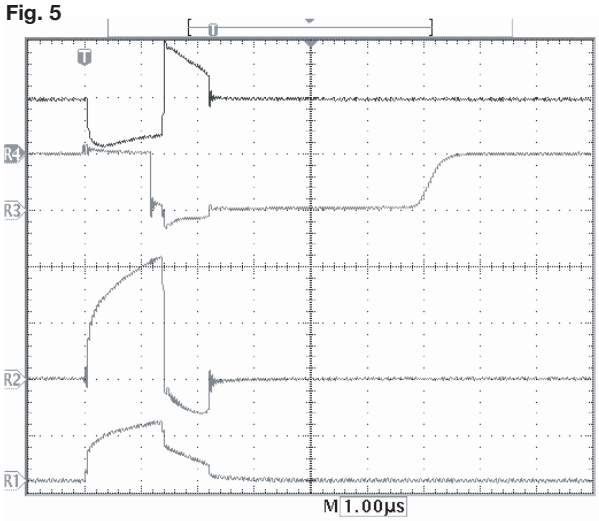


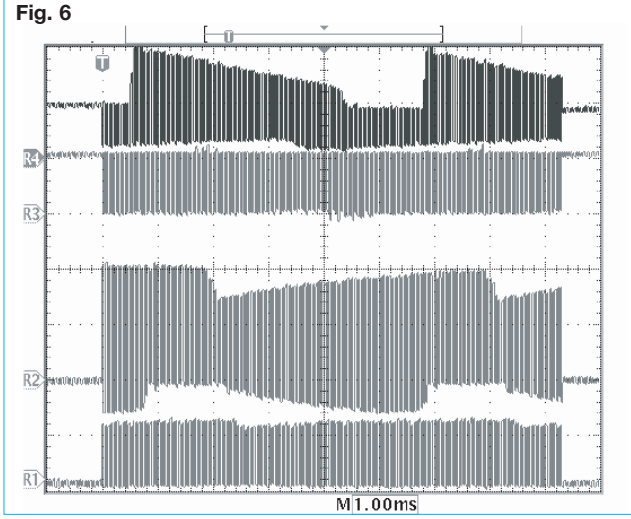
Fig. 5



contributes a measurement error to trace R2. Although a low inductance shunt is used, it does have 10 nH of inductance which adds a voltage drop not representative of the current value. In this case, this inductance provides a 1 volt drop at a current rise rate of 100 A/μs. This can be seen at the turn on of the MOSFET where the voltage across the shunt instantaneously jumps to 1 volt, and during the turn off phase when the voltage instantaneously goes negative.

Figure 6 provides a complete view of a pulse count shutdown sequence at 1 ms/div. Although the waveforms are distorted by aliasing, they provide a view of the pulse count shutdown level of protection. In this case, the pulse count limit is set for 250, and the count window 1 second. The circuit latches off after 8.33 ms.

Fig. 6



Conclusion

Design engineers face trade-offs between cost, size, simplicity, isolation, noise immunity, power dissipation and robustness when incorporating over current protection in their circuits. This paper presents a simple, robust and cost effective method of incorporating over current protection in power electronic circuits to eliminate circuit failures. The method uses a digital output Hall effect OCD to detect the over current condition and

two levels of shutdown to protect against temporary and hard over current events.

The implementation of the protection scheme is explained by application to a demonstration circuit. In this circuit, a power MOSFET is turned on repetitively into a direct short. This action creates a short circuit current and results in a repetitive sequence of turn-on - detection - shutdown. This circuit is operated at frequencies up to 30 kHz demonstrating its effectiveness. Waveforms for the circuit are also presented to aid in the explanation of the operation of the protection scheme.