# High Capacitance Stacked Multi-Layer Ceramic Capacitors for Power Supplies

Jeff Franklin, John Bultitude, John McConnell, Reggie Phillips, Mark Laps, John Prymak and Travis Ashburn

KEMET Electronics Corporation 2835 KEMET Way, Simpsonville, SC 29681, USA Tel: +01-864-228-4401, Fax: +01-965-582-4707, e-mail: jefffranklin@kemet.com

# Abstract

The need for high capacitance coupled with high reliability performance has driven KEMET's development of a new range of surface mountable, leaded MLCC stacked capacitors. The reliability of these stacked capacitors made with class II X7R BME MLCC will be reviewed. Their ability to withstand excessive board flexure as well as many thermal cycles will be described and compared to the standard MLCC performance. The reasons for the improved performance of the stacks will be discussed in detail. The advantages of this technology for use in high frequency switch mode power supplies (SMPS) will be demonstrated using experimental ripple current measurements and these results will be compared to a SPICE based model. The critical factors contributing performance will be described. Microphonic measurements will be presented showing reduced noise using these stacks compared to surface mounted MLCC. Performance comparisons will also be made with larger stacks based on MIL-PRF-49470 form factors. The continuing development of stacked ceramic capacitors with enhanced microphonic and high temperature performance by using a robust Class-1 C0G BME MLCC technology with nickel electrodes will also be described.

# **Introduction**

The continuous development of thinner active layers with class II X7R BME MLCC properties has allowed very high capacitance values to be realized. However, in demanding applications such as power supplies the ability to with withstand excessive board flexure as well as many thermal cycles is a concern. Also as high value MLCC become available in smaller package sizes their ripple current capability performance in high frequency switch mode power supplies (SMPS) needs to be carefully considered since MLCC are rated and sold according to their DC capability. Another application concern for MLCC is the audible, microphonic noise that may occur when a bias is applied to X7R capacitors mounted on circuit boards. The flexure, thermal cycling, ripple current and microphonic performance of selected parts from a new range of J-lead, surface mountable, stacked class II X7R MLCC (KEMET Power Solutions, KPS) have been measured and compared with the capacitors used in their construction. A ripple current comparison is also made with a much larger military case code 3 stack with similar capacitance and voltage rating. The performance data for a 2 x MLCC 2220 J-lead stacks made using robust Class-1 C0G BME MLCC with nickel electrodes are also reviewed and compared to the class II X7R.

# **Board Flexure**

Board flexure failures of MLCC remain a concern in circuits because this failure mode cannot be 100% detected in post assembly testing. Flexure robust capacitors have been developed<sup>1</sup> and in this earlier work the additional benefits of attaching a lead frame to the MLCC were noted. In this study we compared MLCC made with a standard termination of plated tin and nickel over fired fritted copper with J-lead stacks made with these capacitors. The board flexure testing was carried out using the same test system previously described<sup>1</sup>. Samples were reflow soldered to test boards using a Pb-free, Type II Sn96.5/Ag3/Cu0.5 solder paste. The assembled test boards were flexed at 1mm/sec to a maximum of 10mm with 20 readings of the capacitor value per second for 30 samples of each capacitor type. Failures were recorded if the capacitance changed by more than  $\pm/-2\%$  from one reading to the next. The Weibull graphs of failures for selected 1210 and 2220 case sizes are shown in Figures 1 and 2 respectively.



Figure 1. Board flexure failures for 1210 Case Size.

Figure 2. Board flexure failures for 2220 Case Size.

In both the 1210 and 2220 case sizes the failures in the J-lead stack occur at the higher flexure than the MLCC with standard termination. The initial failures in the MLCC samples begin around 4mm flexure in both case sizes. The 1210 J-lead sample had no failures at 10mm flexure but the 2220 stack had some failures between 7.5 and 10.0mm flexure. Cross-sections of the 2220 MLCC failures are shown in Figure 3 and can be compared to the J-lead samples that with failure below >7.5mm in Figure 4.



**Figure 3.** A typical board flexure failure for 2220 MLCC with standard termination at < 7.5mm flexure.

**Figure 4.** A typical board flexure failure for 2220 J-Lead Stack at > 7.5mm flexure.

The MLCC crack begins at the end of the termination and in the case shown (Figure 3.) it propagated through the end margin area of the capacitor removing the entire corner in contact with the test board pad. The J-lead failure (Figure 4.) shows the lead remains attached to the solder and plating with some breakaway of the ceramic in the end termination area of the MLCC itself. This indicates that in both cases the ceramic is where failure occurs. Since failures occur in the J-lead at much higher flexure it can be concluded that the lead adds significant compliancy and so retarding the ceramic cracking. No failures were detected in the 1210 J-lead stack after flexure to 10mm.

# **Thermal Cycling**

It has long been known that coefficient of thermal expansion (CTE) mismatch between MLCC and the circuit board material can produce a tensile stress on the ceramic capacitors leading to failures during thermal cycling or in the event of a severe thermal shock. The CTE for ceramic capacitors made with barium titanate<sup>2</sup>, such as class II X7R MLCC, is around 10 PPM/°C. This compares to a CTE in the range of 11 to 15 PPM/°C reported in the literature<sup>3</sup> measured in the plane of FR4 circuit boards. The differences in CTE between the MLCC and FR4 have to be compensated for by elasticity that is obviously low in the case of a surface mounted ceramic component. These differences and the potential benefit of a compliant lead frame as with J-lead stacks are depicted in Figure 5.



Figure 5. CTE mismatch between MLCC or J-Lead and Circuit board.

In simple terms it can also be seen that for larger MLCC a greater expansion and contraction during thermal cycling is expected leading to a greater mismatch compared to the FR4 board. The performance of 2220 and 1210 J-lead stacks and the MLCC used in the stacks were compared for 3000 temperature cycles -55 to +125°C, with 15°C/minute ramp between temperatures and a 30 minute dwell at these temperatures using 100 samples of each part. The capacitors were reflow soldered to FR4 test boards using a Pb-free, Type II Sn96.5/Ag3/Cu0.5 solder paste then tested at intervals of 250, 500, 1000, 2000 and 3000 cycles. The results are summarized in Table 6.

| Cycles                        | 250   | 500   | 1000  | 2000  | 3000  | <b>Total Failures (%)</b> |
|-------------------------------|-------|-------|-------|-------|-------|---------------------------|
| 1210, 22µF, 25V, J-Lead Stack | 0/100 | 0/100 | 0/100 | 0/100 | 0/100 | 0                         |
| 1210, 10µF, 25V, MLCC         | 0/100 | 0/100 | 0/100 | 0/100 | 0/100 | 0                         |
| 2220, 47µF, 25V, J-Lead Stack | 0/100 | 0/100 | 0/100 | 0/100 | 0/100 | 0                         |
| 2220, 22µF, 25V, MLCC         | 0/100 | 1/100 | 1/100 | 2/100 | 0/100 | 4                         |

Table 6. 1210 and 2220 Thermal Cycling.

On FR4 laminated circuit boards these results show a much more robust performance for the J-lead 2220 case size compared to the MLCC. The 2220 MLCC was developed for the J-lead product and has not been released as a surface mount part. The smaller case size 1210 MLCC are far less prone to thermal cycle failures as expected.

# **<u>Ripple Current Capability</u>**

MLCCs are rated according to their ability to withstand DC voltage. Applying a high AC voltage as experienced in high frequency switch mode power supplies causes self heating of the capacitors as the ferroelectric domains move in the direction of the voltage polarity<sup>4</sup> as depicted in Figure 7. This also depicts the situation for class I dielectrics that do not contain domains so have no heating contribution from the switching. The performance of J-lead COG stacks based on this MLCC technology are described later in this article.



Figure 7. Effect of AC Voltage on Different Ceramic Dielectrics.

The self-heating MLCC can lead to failures depending on the voltage applied in the application. There is no convention on what represents an acceptable level of self-heating but we recommend  $< 50^{\circ}$ C above the ambient temperature. Ripple current measurements were made at 100 kHz on selected J-lead stacks and the MLCC used in the stacks and are shown in Figure 8.



Figure 8. Ripple current of J-lead stacks and MLCC at 100 kHz.

The addition of the J-lead in this case (KPS) has only a small effect on the ripple current at 100 kHz compared to the MLCC. Experimental Ripple current measurements at 100 kHz are shown for a selection of J-lead stacks in Figure 9.



Figure 9. Ripple Current at 100 kHz for selected J-lead stacks

The temperature increases more for the smaller case size 1210 J-lead products than the larger 2220. The power dissipated can be calculated using the equation  $P = I^2 R$ . Using this relationship the power dissipated in each case was calculated at 15Arms and shown in comparison to the measured absolute temperatures at this current in Table 10.

|                                   | 2220, 47µF, | 2220, 22µF, | 1210, 22µF, | 1210, 4.7µF, |
|-----------------------------------|-------------|-------------|-------------|--------------|
| J-Lead Stack                      | 25V rated   | 50V rated   | 25V rated   | 50V rated    |
| ESR @ $100$ kHz (m $\Omega$ )     | 1.88        | 2.60        | 3.05        | 6.60         |
| Power Dissipation @ 15Arms (W)    | 0.42        | 0.59        | 0.69        | 1.49         |
| Absolute Temperature @ 15Arms (C) | 50          | 54          | 84          | 125          |

Table 10. ESR and Power Dissipation for selected J-lead stacks

Higher ESR results in increased power dissipation and there is some general correlation with increased temperature. However, although the  $22\mu$ F stacks have quite similar ESR and power dissipation the temperature of the 1210 stack is 30°C higher than the 2220. This can be explained by considering the thermal resistivity. The 2220 has a significantly higher volume and more electrode area. The electrodes are good at conducting heat and the larger MLCC have more thermal mass so are better able to absorb and conduct heat. This is a challenge not only with respect to further miniaturization of the capacitors but the designers of the power supplies should consider the implications of heat conduction in the circuit board designs.

A SPICE model has been developed that allows ripple current heating to be calculated<sup>5</sup>. The calculated heating has quite good agreement with the experimental measurements for 2220, J-lead stacks as shown in Figure 11.



Figure 11. Experimental and SPICE Calculated Ripple Current Comparison for 2220 J-Lead Stacks at 100 kHz.

As noted earlier the case size can have a significant impact on ripple current. The ripple current measurements of the 2220,  $47\mu$ F, 25V rated J-lead product is compared to measurements on much larger case size Military stack (MIL-PRF-49470) in Figure 12.



Figure 12. Ripple Current Comparison J-Lead Vs CC3 Military Stack at 100 kHz.

The military stack has a much lower temperature increase even though the ESR at 100 kHz was  $2.20m\Omega$  that is higher than the 2220 at  $1.65m\Omega$ . The thermal resistivity differences are even more pronounced in this case because of the large difference in size, the J-lead 2220 stack capacitors take up 0.14cc compared to 4cc for the Case Code 3 Military Stack. The much higher volume of the Military stack allows the heat to be absorbed because of its greater heat capacity but the down side is the space taken up by such a large component. Designers therefore should consider how heat is conducted away from the circuit board when using the smaller J-lead stacks for miniaturization.

## Microphonic Measurements

High capacitance Class II ferroelectric MLCC usually have strong piezoelectric coupling with applied bias causing movement at certain frequencies. The circuit board acts as a sounding board transmitting the MLCC movement. Noise in the frequency range 20Hz to 20 kHz is audible to the human ear. This audible noise is what's known as microphonic. Earlier work on lower capacitance MLCC indicated that using a lead frame to mechanically decouple the capacitor from the circuit board can significantly reduce the microphonic noise<sup>6</sup>. High capacitance J-lead stacks were measured and compared to MLCC using the same equipment as shown in Figure 13.



Figure 13. Microphonic measurements.

The noise floor for this measurement system is 23dB. The overall sound pressure at 1 kHz for 1210 and 2200 J-lead for the same capacitance and voltage rating are compared to the MLCC used in these stacks in Figure 14.



Figure 14. Overall Sound Pressure for 50V rated 1210 and 2220 MLCC and J-lead stacks at 1 kHz.

This work shows that the overall sound pressure for the 2220 J-lead part remains at the noise floor of the measurement system whereas the corresponding surface mounted MLCC reaches > 40dB. Placing a J-lead on the smaller 1210 part was less effective at reducing the noise but even so this was around 6dB lower than the corresponding surface mounted 1210 part ant it should be noted that an increase of 3dB represents 2 x more noise. This result indicates that the 1210 parts tested have stronger piezoelectric coupling at these voltages and frequency. This is attributable to the thinner active used in this MLCC that results in a higher effective voltage per active layer.

In a similar experiment the overall sound pressure from a  $4.7\mu$ F, 50V rated 1210 with a J-lead was compared to the noise from 5 surface mounted 1206,  $1\mu$ F, 100V rated MLCC to determine the potential for reducing noise in an LCD, Figure 15.



Figure 15. Overall Sound Pressure for 50V rated 1210 4.7 $\mu$ F, J-lead compared to 5 x 1206, 1 $\mu$ F, 100V rated MLCC at 1 kHz.

The 1206,  $1\mu$ F, 100V rated MLCC were sourced by a customer to have the lowest microphonic noise but the J-lead is nearly 10dB lower with the added advantage of reduced board space.

This same J-lead 4.7 $\mu$ F, 50V rated 1210 was tested by a customer<sup>7</sup> in a high pass filter circuit and compared to an surface mounted MLCC with the same capacitance and rating , Figure 16.



Figure 16. MLCC Compared to 1210 4.7µF, J-lead for High Pass Filter Noise

This comparison shows the filter output spikes caused by noise are suppressed in the J-lead part. This work and the microphonic comparisons show that using the J-lead can be an effective way to reduce noise compared to MLCC.

#### Class I COG Ni MLCC Stacks

Class I COG MLCC with nickel inner electrodes and relatively high capacitance values have been developed<sup>8</sup>. J-lead stacks of 2 x  $0.47\mu$ F, 50V rated 2220 were made using the same process as the aforementioned J-lead X7R (KPS) to give a  $1\mu$ F stack. The ripple current, microphonic noise and capacitance stability with temperature as well as voltage were measured and comparisons made to the X7R stacks. The ripple current at 100 kHz is shown in Figure 17 that compares C0G to the best performing J-lead X7R (KPS) stack.



Figure 17. Ripple Current Comparison J-Lead X7R (KPS) Vs C0G Stack at 100 kHz.

Despite a far lower capacitance the ripple current performance of the C0G stack at 100 kHz was similar to the best X7R performance. For many applications high capacitance is a necessity but in some applications this very low ripple current coupled with lower dissipation factors for C0G may be desirable. The microphonic noise of the  $0.47\mu$ F, 50V rated, 2220 surface mounted C0G MLCC and  $1\mu$ F stack were measured, Figure 17.



Figure 18. Overall Sound Pressure for 50V rated C0G 2220,  $0.47\mu$ F, MLCC compared to the  $1\mu$ F, 50V J-Lead Stack (2 MLCC) at 1 kHz.

At 1 kHz up to 15V peak to peak the overall sound pressure remained at 23dB, the noise floor of the measurement system, for both MLCC and J-Lead C0G stack. This was not unexpected since unlike X7R the C0G is not ferroelectric (ref. Figure 7.) so does not exhibit strong piezoelectric coupling with applied bias. The capacitance of C0G is much more stable with temperature and voltage than X7R as shown for stacks in Figure 19.



Figure 19. Change of Capacitance with Temperature and Voltage for J-lead COG and to X7R Stacks.

The X7R stack looses over 60% of the available capacitance at 200°C with the rated voltage applied whereas the C0G capacitance hardly changes. In addition to having stable temperature and voltage MLCC using this C0G system have reliable performance above 200°C<sup>9</sup>. Further work is underway to demonstrate the reliability of C0G J-lead stacks at 200°C to offer higher capacitance solutions at these temperatures.

# **Summary**

A new range of J-lead, surface mountable, stacked class II X7R, BME MLCC (KEMET Power Solutions, KPS) has been developed and shown to have better board flexure performance than MLCC. The stacks had no failures on 3000 thermal cycles (-55 to +125°C). The ripple current performance was measured experimentally and calculated using a SPICE model that allows designers to check the ripple current performance for their specific switch mode power supply application conditions. The importance of designing the circuit board to for effective heat dissipation was noted when considering using the smaller J-lead for miniaturization. The J-lead was shown to be an effective way to reduce microphonic noise compare to MLCC. The performance of COG, BME MLCC J-lead stacks is being evaluated at 200°C as part of our development of stacks for use at higher temperatures.

## **Acknowledgements**

The authors would like to acknowledge the support of their colleagues, Abhijit Gurav, Xilin Xue, Mike Lopez, Jim Magee, Kevin Lynn and Peggy Bryson.

## References

- "Flex Robust Capacitors", Bill Sloka, Dan Skamser, Reggie Phillips, Allen Hill, Mark Laps, Roy Grace, John Prymak, Michael Randall, Aziz Tadjuddin, CARTS 2007 Symposium Proceedings, Albuquerque, New Mexico, USA, March 2007.
- 2. US Patent Number 6,081,416, H. Trinh, A. D. Devoe and D. Devoe, June 27, 2000.
- 3. "Electronic Materials Handbook, Volume 1, Packaging", ASM International, 1989, p58.
- 4. "Electroceramics", Second Edition, A. J.Moulson and J.M.Herbert, Wiley &sons, 2003, p79.

- 5. "KEMET Spice An Update", Bill Long, Mike Prevallet, John Prymak, CARTS 2004, San Antonio, Texas, USA, March 2004.
- "Capacitors for Reduced Microphonics and Sound Emission", Mark Laps, Roy Grace, Bill Sloka, John Prymak, Xilin Xu, Pascal Pinceloup, Abhijit Gurav, Michael Randall, Philip Lessner, Aziz Tadjuddin, CARTS 2007 Symposium Proceedings, Albuquerque, New Mexico, USA, March 2007.
- 7. "DSA Data Integrity in a High Vibration Environment", April 17, 2009, Kevin R. Ballou, David McDaniel, National Instruments
- 8. "BME COG MLCC: The High Capacitance Class-I Solution", Xilin Xu, Abhijit Gurav, Michael Randall, Jim Magee, Aziz Tadjuddin, CARTS-Europe 2007 Symposium Proceedings, Barcelona, Spain, November 2007.
- "Robust Reliability of BME Class-I High Temperature Capacitors", Xilin Xu, Jeff Franklin, Travis Ashburn, John Bultitude, Clive Randall, Abhijit Gurav, Components for Military and Space Electronics Conference & Exhibition, February 8 -11, 2010, LAX Radisson Hotel, Los Angeles, CA