SHARC's ASRC example

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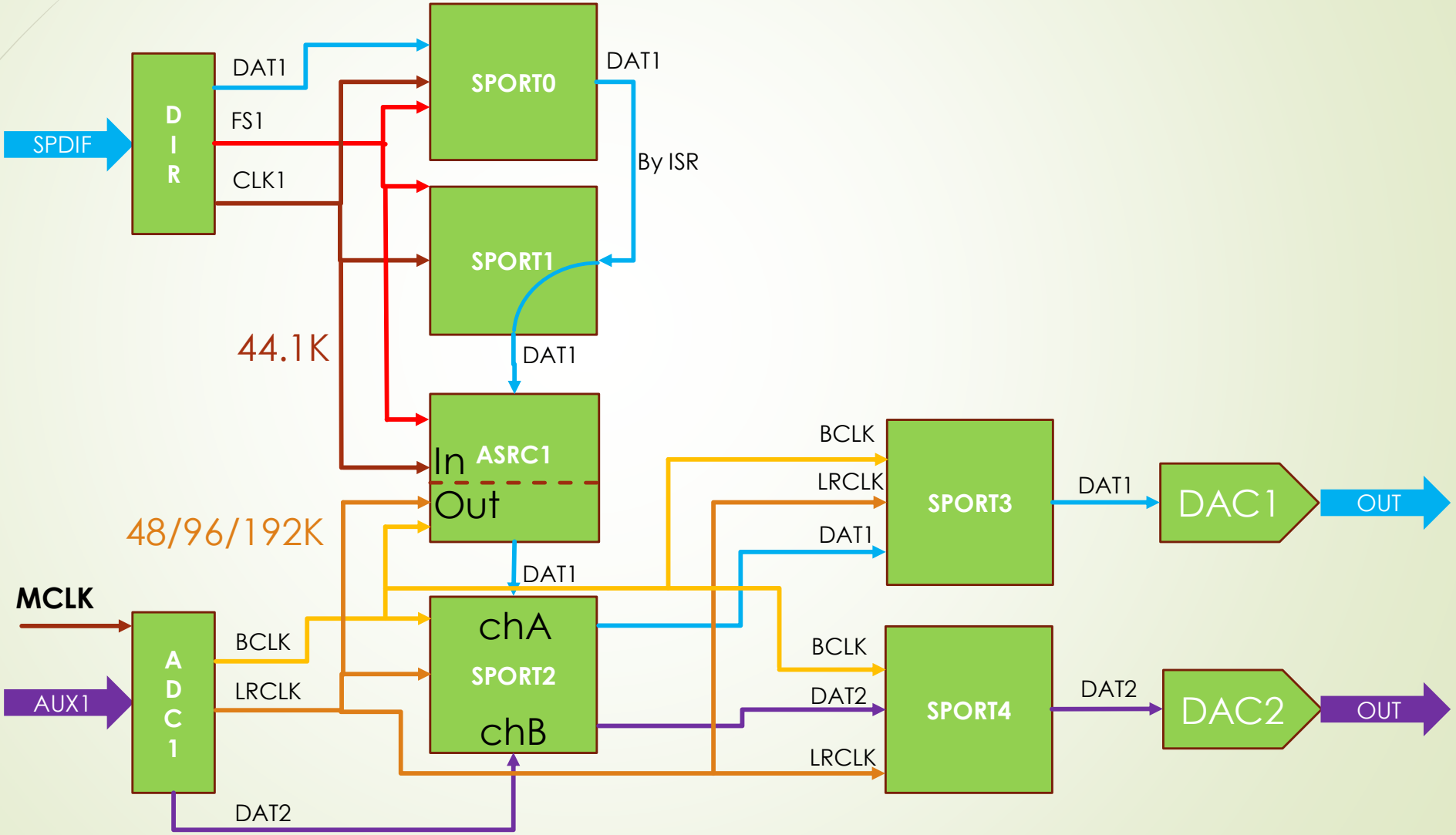
This doc is based on the example project in VisualDSP++5.1.2

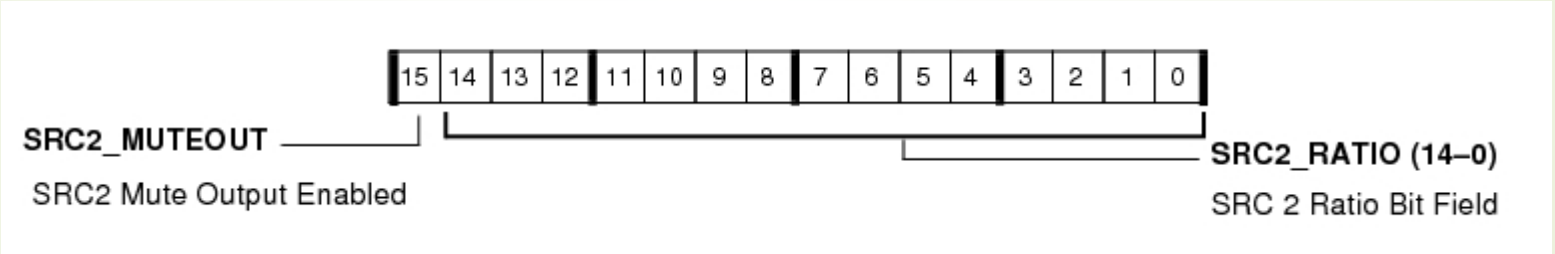
- Project location: $:\Program Files (x86)\Analog Devices\VisualDSP 5.1.2\214xx\Examples\ADSP-21489 EZ-Board\SPDIF to Analog TalkThru with SRC (C)
- TalkThrough reads audio samples from the on-chip SPDIF receiver and it passes the unmodified data through to the two DACs of the AD1939.
- There are two clock domains in this project:
  - The first is derived from the SPDIF input stream. Each interrupt reads a single 24-bit sample (alternating left and right) using SPORT0A and immediately writes the same value to SPORT1A. All audio is transmitted in I2S mode.
  - The second clock is provided by the AD1939. Each interrupt reads a single 24-bit sample (alternating left and right) using SPORT2 and immediately writes the same value to both the A and B data channels of SPORT3 and SPORT4. All audio is transmitted in I2S mode.
- The ADC1 data is being received on SPORT2B while the SPDIF is being received on SPORT2A. The ADC1 data is being copied to DACs 1 & 2, and the SPDIF data is being copied to DACs 3 & 4.
- An Asynchronous SRC is being used to convert the data between the two clock domains so that the input data from the SPDIF receiver can be sent to the DACs.

System diagram(data/clock flow)



SRCRAT0 TABLE/REG in 2148x HRM

SRCRAT0	48K	96K	192K
SPDIF(44.1K)	08B6 8000	116B 8000	22D5 8000
in binary	0000 1.000 1011 0110	0001 0.001 0110 1 011	0010 0.010 1101 0101
in dec	1.088	2.177	4.354



Bit	Name	Description
14–0	SRCx_RATIO	**Sampling Ratio of Frame Syncs.** These bits can be read to find the ratio of output to input sampling frequency (SRCx_FS_OP_I/SRCx_FS_IP_I). This ratio is reported in 4.11 (integer.fraction) format where the 15-bit value of the normal binary number is comprised of 4 bits for the integer and 11 bits for the fraction.
15	SRCx_MUTEOUT	**Mute Status.** The SRCx_MUTEOUT bits in SRCRATx register report the status of the MUTE_OUT signal. Once the SRCx_MUTEOUT signal is cleared then the ratio can be read. When the SRCx_ENABLE is set or there is a change in the sample ratio, the MUTE_OUT signal is asserted. The MUTE_OUT signal remains asserted until the digital servo loop's internal fast settling mode is complete. When the digital servo loop has switched to slow settling mode, the MUTE_OUT signal is deasserted. Reset = 0x80008000.