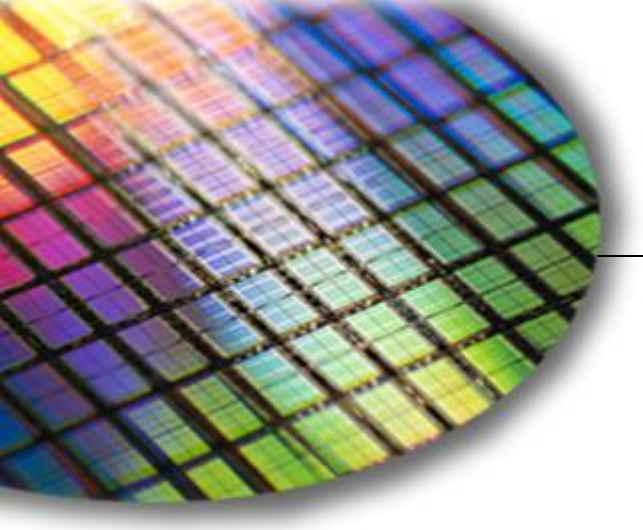


The World Leader in High Performance Signal Processing Solutions

ADSP-BF60x Guide to Power Estimation
Rev 4 (05/16/2014)

ANALOG DEVICES

Revision history

Revision	Changes
Rev 0 (6/18/2012)	Initial Revision
Rev 1 (6/25/2012)	Fixed typos, formatting, and added thermal diode data
Rev 2 (7/12/2012)	Added hibernate data and more details on how to read typical data
Rev 3 (1/16/2013)	Added typical static power data over temperature, additional PVP power data, and hibernate power data
Rev 4 (05/06/2013)	Removed references to “preliminary”. Adjusted example to a more realistic scenario.

Introduction

This document describes how to estimate power consumption for the BF60x processors.

The application note EE-297: Estimating Power for ADSP-BF534/BF536/BF537 Blackfin® Processors should be used as a reference since much of it also applies to BF60x. EE-297 is available at www.analog.com/blackfin under application notes.

Please consult the following sections of the ADSP-BF60x Data Sheet (PrE or later) for the following specifications referred to throughout this document:

- See the Operating Conditions section for details regarding VDD_INT, VDD_EXT, VDD_DMC, VDD_USB, and VDD_TD ranges.
- See the Ordering Guide section for a list of the presently available ADSP-BF60x models processors.

Power Consumption

Derived Power Consumption (PDD_TOT)

- **PDD_TOT = ΣP_{DDn} where n = each V_{DD} domain**

Standard Power Domains (All Blackfin Products)

- **Internal Power Consumption (PDD_INT)**
  - Static and Dynamic Components

    Static (Leakage) is a function of Voltage (VDD_INT) and Operating Junction Temperature (T_J)

    Dynamic is a function of Voltage and Frequency
- **External Power Consumption (PDD_EXT)**
  - PDD_EXT factors several components

    Voltage, Frequency, Output Pins Toggling, and Usage

    Largely an estimation based on application run-time averages

Other Power Domains

Some have the same rules as PDD_EXT

- **MEM (P_{DDMEM}) – ADSP-BF51x and ADSP-BF52x**
- **FLASH ($P_{DDFLASH}$) – ADSP-BF51x**
- **DDR Memory (P_{DDDMC} /P_{DDDDR}) – ADSP-BF54x, ADSP-BF60x**

Others Are Specified In Datasheet

- **OTP Memory (P_{DDOTP}) – ADSP-BF51x and ADSP-BF52x**
- **USB (P_{DDUSB}) –ADSP-BF52x, ADSP-BF54x, ADSP-BF60x**
- **Thermal Diode (P_{DDTD}) – ADSP-BF60x**

Maximum Internal Power (PDD_INT)

Internal Power Consumption (PDD_INT)

Consumed by core, PLL, peripherals, and other internal circuitry

- **Voltage, Frequency, and Temperature influence numbers**
- **Dependent on the application code running**

Typical and Maximum specifications for IDD_INT are given at specific voltages, frequencies, and temperatures

I_{DDINT} Estimation

The following equation is used to estimate IDDINT:

$$I_{DDINT} = I_{DDINT\_CCLK\_DYN} + I_{DDINT\_SYSCLK\_DYN} + I_{DDINT\_SCLK0\_DYN} + I_{DDINT\_SCLK1\_DYN} + I_{DDINT\_DCLK\_DYN} + I_{DDINT\_USBCLK\_DYN} + I_{DDINT\_DMA\_DR\_DYN} + I_{DDINT\_DEEPSLEEP} + I_{DDINT\_PVP\_DYN}$$

- **Static Component – IDDINT_DEEPSLEEP**
  - Accounts for process variation
  - Vast majority of parts will have plenty of headroom to this maximum
- **Dynamic Components**
  - IDDINT_CCLK_DYN – Dynamic current from the core clock domain. Depends on the ASF (activities scaling factor) of each core, CCLK frequency, and VDD_INT
  - IDDINT_SYSCLK_DYN, IDDINT_SCLK0_DYN, IDDINT_SCLK1_DYN, and IDDINT_DCLK_DYN – Dynamic components calculated from the frequency of the clock, VDD_INT, and an ADI-provided coefficient which was measured for each clock domain.
  - IDDINT_USBCLK_DYN – Dynamic component that is added if USB is used
  - IDDINT_DMA_DR_DYN – Dynamic component that represents the total data rate used in non-CCLK clocking domains. Calculated by adding the data rate of each DMA and core driven access to peripherals and L2/external memory. This number is then multiplied by an ADI-provided coefficient and VDD_INT
  - IDDINT_PVP_DYN – Dynamic current from using the PVP.

$I_{DDINT\_DEEPSLEEP}$ – Static Component of Power (Maximum)

Maximum Static Current – IDDINT_DEEPSLEEP (mA)							
	Voltage (VDD_INT)						
T_J (°C)	1.190	1.200	1.225	1.250	1.275	1.300	1.320
-40	1.7	1.8	2.2	2.5	2.7	3.1	3.4
-20	4.0	4.2	4.6	5.1	5.6	6.2	6.8
0	8.4	9.0	9.6	10.6	11.5	12.5	13.4
25	19.0	19.8	21.5	23.2	25.3	27.2	29.0
40	29.9	31.7	34.4	36.8	40.0	42.8	45.4
55	46.6	48.9	52.4	56.4	60.6	65.0	68.1
70	66.4	70.4	75.5	80.6	86.2	92.4	97.9
85	93.9	99.3	105.9	113.0	120.7	128.9	136.4
100	137.2	144.2	153.6	163.4	173.9	185.1	194.1
105	153.8	162.4	172.5	183.4	195.2	207.5	217.5
115	193.3	203.7	216.2	229.5	243.9	258.6	271.1
125	236.1	247.2	261.8	277.3	294.0	311.9	326.4

- **Static Component (IDDINT_DEEPSLEEP) is exactly the value in this table**
  - Recall: Deep Sleep Mode – CCLK = SYSCLK = DCLK = SCLK0 = SCLK1 = 0 MHz with Power On
  - Specification is a maximum current across process. In other words, Analog Devices does not sell any production grade BF60x parts with IDDINT_DEEPSLEEP above the values in the table above.
  - Changes with VDD_INT and Tj (junction temperature)
- **VDD_INT plots of IDD_INT vs. Temperature follow exponential curve**

IDDINT_CCLK_DYN

CCLK Dynamic Current per core (mA, with ASF = 1)							
	Voltage (V_{DDINT})						
f_{CCLK} (MHz)	1.190	1.200	1.225	1.250	1.275	1.300	1.320
500	97.9	98.8	101.5	103.9	106.7	109.3	110.8
450	88.6	89.5	91.9	94.1	96.7	98.9	100.6
400	79.3	80.1	82.2	84.3	86.5	88.6	90.1
350	70.0	70.7	72.5	74.4	76.3	78.3	79.4
300	60.6	61.2	63.0	64.6	66.3	68.0	69.1
250	51.3	51.8	53.2	54.7	56.3	57.6	58.5
200	42.0	42.4	43.6	44.8	46.0	47.2	48.2
150	32.5	32.9	34.0	34.8	35.9	37.0	37.4
100	23.2	23.5	24.2	25.0	25.7	26.5	26.9

I_{DDINT} Power Vector	ASF
IDD-PEAK	1.34
IDD-HIGH	1.25
IDD-FULL-ON_TYP	1.00
IDD-APP	0.86
IDD-NOP	0.72
IDD-IDLE	0.14

IDDINT_CCLK_DYN (mA) = (CCLK Dynamic Current per core) · (ASF_core0 + ASF_core1)

- **CCLK Dynamic Current per core is measured by Analog Devices and can be taken straight from the table above**
- **ASF indicates activity level on the core**
  - **1.00 is Baseline – uses "Typical" application previously defined (See the next slide)**
    - Core Performing 75% Dual-MAC, 25% Dual-ALU Operations
    - No DMA Activity
    - Core fetches a data pattern from L1 (half the data bits toggling)
  - **Multipliers are specifications based on characterization**
  - **User must determine which Activity Level most closely matches their own application**

Activity Scale Factors (ASF)

$I_{DD-IDLE}$

- **Core executing the IDLE instruction only, with no core memory accesses, no DMA, and no interrupts**

I_{DD-NOP}

- **Core executing the NOP instruction only, with no core memory accesses, no DMA, and no interrupts**
  - Useful for software delay loops

I_{DD-APP}

- **Core executing an application comprised of 30% dual-MAC instructions and 70% load-store and NOP instructions**
- **All instructions and data are located in L1 SRAM, and peripherals/DMA are not enabled**

I_{DD-TYP}

- **Same as I_{DD-APP} except application is 75% dual-MAC instructions and 25% dual-ALU instructions**
  - Datasheet baseline

$I_{DD-HIGH}$

- **Same as I_{DD-APP} except application is 100% dual-MAC instructions**

$I_{DD-PEAK}$

- **Same as $I_{DD-HIGH}$ except with memory DMA moving a data pattern (toggling all bits every access) from L1 Data A memory to L1 Data B memory**
- **NOTE: The test code used to measure IDD-PEAK represents worst-case processor operation. This activity level is not sustainable under normal application conditions.**

IDDINT_SYSCLK_DYN, IDDINT_SCLK0_DYN, IDDINT_SCLK1_DYN, and IDDINT_DCLK_DYN

The following equations are used to estimate clock domain dependent dynamic components:

$$I_{DDINT\_SYSCLK\_DYN}\ (\mathbf{mA}) = .187\ \frac{mA}{MHz \cdot V} \cdot f_{SYSCLK}\ (\text{MHz}) \cdot V_{DDINT}\ (\text{V})$$

$$I_{DDINT\_SCLK0\_DYN}\ (\mathbf{mA}) = .217\ \frac{mA}{MHz \cdot V} \cdot f_{SCLK0}\ (\text{MHz}) \cdot V_{DDINT}\ (\text{V})$$

$$I_{DDINT\_SCLK1\_DYN}\ (\mathbf{mA}) = .042\ \frac{mA}{MHz \cdot V} \cdot f_{SCLK1}\ (\text{MHz}) \cdot V_{DDINT}\ (\text{V})$$

$$I_{DDINT\_DCLK\_DYN}\ (\mathbf{mA}) = .024\ \frac{mA}{MHz \cdot V} \cdot f_{DCLK}\ (\text{MHz}) \cdot V_{DDINT}\ (\text{V})$$

These dynamic components are calculated from the frequency of the clock, VDD_INT, and an ADI-provided coefficient that was measured for each clock domain.

IDDINT_USBCLK_DYN

There is a small dynamic adder to IDDINT when the USB peripheral is used:

Is USB Used?	IDDINT_USBCLK_DYN
Yes	5 mA
No	0 mA

IDDINT_DMA_DR_DYN

The following equation is used to estimate the data-rate-dependent dynamic component in BF60x processors:

$$I_{DDINT\_DMA\_DR\_DYN}\ (\mathbf{mA}) = .0578\ \frac{mA}{MBPS \cdot V} \cdot \text{DataRate (MBPS)} \cdot V_{DDINT}\ (\text{V})$$

The general form of this equation is:

IDDINT_DMA_DR_DYN = DRC · DataRate · VDDINT

Data Rate

- Represents the total data rate used in non-CCLK clocking domains
- Expressed in MBPS (MBytes/second)
- Calculated for the end application by adding the data rate of each DMA and core driven access to and from peripherals and L2/external memory.
- Because it is expressed in MBPS the frequency is already taken into account
- Basic example for a single peripheral: SPORT receive clock is running at 25 MHz and the SPORT is in DMA mode. 2 data lines are being used:

  2 bits/cycle · 25 M cycles/second · 1/8 bytes/bit = 6.25 MBPS

DRC (Data Rate Coefficient)

- Units are $\frac{mA}{MBPS \cdot V}$
- When multiplied by Data Rate and VDDINT the result is IDDINT_DMA_DR_DYN (mA)

IDDINT_PVP_DYN

There is a dynamic adder to IDDINT when the PVP is used:

IDDINT_PVP_DYN (mA) = PVPSF * VDD_INT

PVP Activity Level	PVPSF (PVP Scaling Factor)
High	42.4
Medium	20.0
None	0.0

High – This test case uses the camera pipe and memory pipe with all blocks operating.

Medium – Uses the PVP (memory pipe only) as a co-processor to perform Canny edge detection. The pipe first performs Gaussian low pass filtering on the frame before performing Canny edge detection and classification. Three convolution blocks, the Polar Magnitude and Angle (PMA) block, and the Pixel Edge Classifier (PEC) block are used in the pipe along with the input and output formatters. A continuous stream of 1280x960 frames were used for the test.

None – If the PVP is not used IDDINT_PVP_DYN = 0

Typical Internal Power (PDD_INT Typical)

How to Read Typical IDD_INT Data

How is typical power usually defined?

- Nominal VDD_INT (typical data across the operating voltage range is also available)
- Tjunction = 25˚ C (typical data across the operating temperature range is also available)
- ASF (Activity Scaling Factor) = 1.0 for each core
- Typical silicon - some individual BF60x parts will consume more IDDINT_DEEPSLEEP (static current) and some individual BF60x parts will consume less IDDINT_DEEPSLEEP.
- The most useful information is the typical IDDINT_DEEPSLEEP (static current) since IDDINT_DEEPSLEEP varies from part to part whereas the rest of the components of IDD_INT are the same on every part.

DO:

- Do use for back of the envelope calculations
- Do use typical data to estimate AVERAGE battery life
- Compare to other manufacturers typical data (carefully because of different definitions of typical)
- Make your own estimate of ASF and I/O Power when using typical data

DO NOT

- Do not use typical data to size a power supply
- Do not confuse typical data with maximum data
- Do not assume that all parts are typical
- Do not use typical data for system thermal analysis

ADSP-BF609 Preliminary Typical IDDINT Current

Conditions: VDD_INT = 1.25V, Junction Temperature = 25C, Typical Silicon					
Current Component	**CCLK (MHz)**	**SYSCLK (MHz)**	**SCLK0/1 (MHz)**	**DCLK (MHz)**	**IDDINT (mA) Typical**
Static Current	0	0	0	0	5.1
Dynamic CCLK Current with both cores running Full-on Typical (ASF = 1)	500	N/A	N/A	N/A	207.8
Dynamic CCLK Current with core0 running Full-on Typical (ASF = 1) and core1 in Idle	500	N/A	N/A	N/A	118.4
Dynamic SCLK/DCLK Current with no peripheral activity	0	250	125	250	106.4

Total Typical Current for VDDINT Power Supply Domain (Core0 : FOT / Core1 : FOT)	**319.3**
Total Typical Current for VDDINT Power Supply Domain (Core0 : FOT / Core1 : IDLE)	**229.9**

Note1: FOT is Full-on Typical (ASF = 1)

Note2: CCLK is core clock; SCLKx are peripheral clocks; SYSCLK is the system clock; DCLK is DDR2 clock

Note3: Test case notes:

- No peripheral activity
- No DDR transactions
- No L2 accesses
- No USB clocks or activity
- No PVP activity
- IDDINT current only - No I/O pad current included

$I_{DDINT\_DEEPSLEEP}$ – Static Component of Power (Typical)

WARNING: Typical power is in the middle of the product distribution. A significant number of devices will exceed typical power. It is recommended that maximum power is used for system analysis.

Typical Static Current – IDDINT_DEEPSLEEP (mA)							
	Voltage (VDD_INT)						
T_J (°C)	1.19	1.200	1.225	1.250	1.275	1.300	1.320
-40	0.6	0.6	0.7	0.9	1.0	1.1	1.2
-20	1.1	1.2	1.3	1.4	1.5	1.7	1.8
0	2.0	2.1	2.3	2.5	2.8	3.2	3.4
25	4.1	4.2	4.5	5.1	5.4	5.9	6.3
40	6.9	7.3	7.4	8.4	8.5	9.2	9.7
55	10.9	11.3	11.8	12.6	13.4	13.9	14.5
70	17.6	18.0	18.4	19.8	21.4	22.0	23.4
85	26.5	27.3	28.8	30.6	32.5	33.6	35.9
100	39.8	40.9	43.0	46.1	48.1	50.4	53.3
105	45.7	46.7	49.1	52.9	55.2	58.2	61.8
115	60.2	61.6	64.8	68.2	71.8	75.5	79.7
125	78.1	79.7	84.2	87.6	93.0	97.9	102.0

- **Typical Static Component (typical IDDINT_DEEPSLEEP) is the value in this table**
  - Recall: Deep Sleep Mode – CCLK = SYSCLK = DCLK = SCLK0 = SCLK1 = 0 MHz with power on
  - The data provided is represents the middle of the product distribution. In other words, static power on an individual device may be higher (up to the maximum IDDINT_DEEPSLEEP specification) or lower
  - Changes with VDD_INT and Tj (junction temperature)
- **VDD_INT plots of IDD_INT vs. Temperature follow exponential curve**

External Power (PDD_EXT) and Others

External Power Consumption (PDD_EXT)

For each unique group of pins, magnitude depends on

- **Number of output pins that switch during each cycle (O)**
- **Maximum frequency at which they can switch (f)**
- **Load capacitance (C)**
- **Voltage swing (VDD_EXT^2)**
- **Utilization factor (U)**

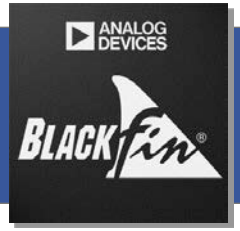
External power estimation calculation

- **$PDD\_EXT = \frac{1}{2} (VDD\_EXT^2) * C * f * O * U$**
  - Model assumes ½ power dissipated by external components
- **Equation extends to cover PDD_DMC**

PDD_USB & PDD_TD

- **Simulation estimates the worst case IDD_USB to be 30mA.**

- **IDD_TD will not exceed 1 µA**



Hibernate Current/Power

Hibernate Current (Only applies when the processor is in the HIBERNATE state)

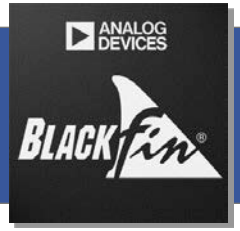
Test Conditions:

VDD_INT = 0V, VDD_DMC = 1.8V, VDD_EXT = 3.3V, VDD_TD = 3.3V, VDD_USB = 3.3V, VREF_DMC = 0.9V, fCLKIN = 0MHz, 25C, USB Wake-up source enabled.

Typical silicon - some individual BF60x parts will consume more hibernate current and some individual BF60x parts will consume less hibernate current.

Total current on IDD_DMC, IDD_EXT, IDD_TD, and IDD_USB during hibernate: **40uA (typical)**

Total power consumption on IDD_DMC, IDD_EXT, IDD_TD, and IDD_USB during hibernate: **130uW (typical)**



Example Power Calculation

When should Maximum Power calculations be used?

Maximum power calculation is intended to cover the following cases:

A) Power Supply sizing

- DO:
  - Use maximum voltage for power supply sizing
  - Use maximum Tjunction (as appropriate for your application maximum Tambient)
  - Use highest ASF possible for the application being run (could occur for a short duration in the application code – but not sustainable)
  - Calculate each unique voltage domain separately
- DO NOT
  - Do not use typical Idd or nominal voltage or room temperature to size a power supply
  - Do not use total device power to size a power supply

B) Total device Thermal Power

- DO:
  - Use nominal voltages to calculate thermal power
  - Use maximum Tjunction (as appropriate for your application maximum Tambient)
  - Use Full-on-Typical or lower ASF (to match realistic application code activity levels)
  - Calculate total power for all voltage domains
- DO NOT
  - Do not use typical Idd data or room temperature to calculate thermal power
  - Do not use maximum voltage (this is not realistic since any transient will exceed max voltage spec)

Total Device Thermal Power Example BF60x – Input Data

The following input data is used to calculate IDD_INT in this example:

VDDINT (V)	1.25
VDDEXT (V)	3.30
Tjunction (°C)	100
CCLK (MHz)	400
SYSCLK (MHz)	200
SCLK0 (MHz)	50
SCLK1 (MHz)	25
DCLK (MHz)	0
ASF_core0	1.00
ASF_core1	0.86

USB, PVP, and DDR memory aren't used. Peripheral usage assumptions are shown on the IDDINT_DMA_DR_DYN and PDD_EXT pages.

First, Obtain Static Component

Static Current – IDDINT_DEEPSLEEP (mA)							
	Voltage (VDD_INT)						
T_J (°C)	1.190	1.200	1.225	1.250	1.275	1.300	1.320
-40	1.7	1.8	2.2	2.5	2.7	3.1	3.4
-20	4.0	4.2	4.6	5.1	5.6	6.2	6.8
0	8.4	9.0	9.6	10.6	11.5	12.5	13.4
25	19.0	19.8	21.5	23.2	25.3	27.2	29.0
40	29.9	31.7	34.4	36.8	40.0	42.8	45.4
55	46.6	48.9	52.4	56.4	60.6	65.0	68.1
70	66.4	70.4	75.5	80.6	86.2	92.4	97.9
85	93.9	99.3	105.9	113.0	120.7	128.9	136.4
100	137.2	144.2	153.6	163.4	173.9	185.1	194.1
105	153.8	162.4	172.5	183.4	195.2	207.5	217.5
115	193.3	203.7	216.2	229.5	243.9	258.6	271.1
125	236.1	247.2	261.8	277.3	294.0	311.9	326.4

Use the Static Current table

- **VDD_INT = 1.25 V, T_J = 100 C**
- **IDDINT_DEEPSLEEP = 163.4 mA**

Calculate the IDDINT_CCLK_DYN Component

CCLK Dynamic Current per core (mA, with ASF = 1)							
	Voltage (V_{DDINT})						
f_{CCLK} (MHz)	1.190	1.200	1.225	1.250	1.275	1.300	1.320
500	97.9	98.8	101.5	103.9	106.7	109.3	110.8
450	88.6	89.5	91.9	94.1	96.7	98.9	100.6
400	79.3	80.1	82.2	84.3	86.5	88.6	90.1
350	70.0	70.7	72.5	74.4	76.3	78.3	79.4
300	60.6	61.2	63.0	64.6	66.3	68.0	69.1
250	51.3	51.8	53.2	54.7	56.3	57.6	58.5
200	42.0	42.4	43.6	44.8	46.0	47.2	48.2
150	32.5	32.9	34.0	34.8	35.9	37.0	37.4
100	23.2	23.5	24.2	25.0	25.7	26.5	26.9

I_{DDINT} Power Vector	ASF
IDD-PEAK	1.34
IDD-HIGH	1.25
IDD-FULL-ON_TYP	1.00
IDD-APP	0.86
IDD-NOP	0.72
IDD-IDLE	0.14

VDD_INT = 1.25 V, f_{CCLK} = 400 MHz

ASF highly dependent on application

One core is running peak activity and the other is running typical

IDDINT_CCLK_DYN (mA) = (CCLK Dynamic Current per core) · (ASF_core0 + ASF_core1)

IDDINT_CCLK_DYN (mA) = 84.3 · (1.00 + 0.86) = 156.8 mA

Calculate IDDINT_SYSCLK_DYN, IDDINT_SCLK0_DYN, IDDINT_SCLK1_DYN, and IDDINT_DCLK_DYN

SYSCLK (MHz)	200
SCLK0 (MHz)	50
SCLK1 (MHz)	25
DCLK (MHz)	0

IDDINT_SYSCLK_DYN (mA) = .187 · fSYSCLK (MHz) ·VDDINT (V)

IDDINT_SYSCLK_DYN (mA) = .187 · 200 MHz · 1.25 V = 46.75 mA

IDDINT_SCLK0_DYN (mA) = .217 · fSCLK0 (MHz) ·VDDINT (V)

IDDINT_SCLK0_DYN (mA) = .217 · 50 MHz · 1.25 V = 13.56 mA

IDDINT_SCLK1_DYN (mA) = .042 · fSCLK1 (MHz) ·VDDINT (V)

IDDINT_SCLK1_DYN (mA) = .042 · 25 MHz · 1.25 V = 1.31 mA

IDDINT_DCLK_DYN (mA) = .024 · fDCLK (MHz) ·VDDINT (V)

IDDINT_DCLK_DYN (mA) = .024 · 0MHz · 1.25 V = 0 mA

Calculate IDDINT_DMA_DR_DYN, IDDINT_USBCLK_DYN, & IDDINT_PVP_DYN

$$I_{DDINT\_DMA\_DR\_DYN}\ (\mathbf{mA}) = .0578\ \frac{mA}{MBPS \cdot V} \cdot \text{DataRate (MBPS)} \cdot V_{DDINT}\ (\text{V})$$

Peripheral	Freq (Hz)	# of Data Bits	Data Rate (MBPS)
8-bit PPI	2.70E+07	8	25.75
SPORT0	4.00E+06	2	0.95
SPORT1	4.00E+06	2	0.95
UART	1.15E+05	2	0.03
Total Data Rate (MBPS)			**27.68**

IDDINT_DMA_DR_DYN = 0.0578 · DataRate · VDDINT = 0.0578· 27.68· 1.25 = 2.00 mA

IDDINT_USBCLK_DYN = IDDINT_PVP_DYN = 0 mA because USB and PVP aren't used in this example

IDD_INT Total & PDD_INT Calculation

$$I_{DDINT} = I_{DDINT\_CCLK\_DYN} + I_{DDINT\_SYSCLK\_DYN} + I_{DDINT\_SCLK0\_DYN} + I_{DDINT\_SCLK1\_DYN} + I_{DDINT\_DCLK\_DYN} + I_{DDINT\_USBCLK\_DYN} + I_{DDINT\_DMA\_DR\_DYN} + I_{DDINT\_DEEPSLEEP} + I_{DDINT\_PVP\_DYN}$$

Component	Current (mA)
IDDINT_DEEPSLEEP (max)	163.40
IDDINT_CCLK_DYN	156.80
IDDINT_SYSCLK_DYN	46.75
IDDINT_SCLK0_DYN	13.56
IDDINT_SCLK1_DYN	1.31
IDDINT_DCLK_DYN	0.00
IDDINT_USBCLK_DYN	0.00
IDDINT_DMA_DR_DYN	2.00
IDDINT_PVP	0.00
Total IDDINT	**383.82**

$$P_{DD\_INT} = IDD\_INT \times V_{DD\_INT}$$

$$P_{DD\_INT} = 383.82\ mA \times 1.25\ V$$

$$P_{DDINT} = \underline{479.78\ mW}$$

Calculating PDD_EXT

Peripheral	Freq (Hz)	# of Output Pins	C/pin (F)	Toggle ratio	Util	VDD_EXT (V)	Pout @ 3.30V (mW)
8-bit PPI	2.70E+07	9	3.00E-11	1	1	3.30	39.69
SPORT0	4.00E+06	2	3.00E-11	1	1	3.30	1.31
SPORT1	4.00E+06	2	3.00E-11	1	1	3.30	1.31
UART	1.15E+05	2	3.00E-11	1	0.25	3.30	0.01
Total Peripheral Power Dissipation @ 3.3V (estimated)						**PDD_EXT**	**42.32**

Total Power Consumption

- **PDD_TOT = ΣP_{DDn} where n = each V_{DD} domain**
- **For this example ADSP-BF60x application:**
  - PDD_TOT = PDD_INT + PDD_EXT
  - PDD_TOT = 479.78 mW + 42.32 mW
  - PDD_TOT = 522.1 mW

Questions?

- **E-mail processor.support@analog.com**