REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

CMOS OUT

J7 — R106 0 — TP1 — C87 OPT — OUT_CMOS

TP2 — GND — GND

R11 OPT — GND — R14 OPT

DEVICE=ADT2-1T-1P
ADTT1-1 /CD542 PKG

GND — 4 5 6 — 3 2 1 — GND

T1

DEFAULT: INSTALL R13, NOT R12
IF USING FILTER: REMOVE R13 & INSTALL BOXED ITEMS

400 MHz LPF — OPTIONAL

DUT OUT/FILTER IN — J4 — R13 OPT — R12 0

C80 2.7PF — C36 5.6PF — C28 6.8PF — C12 3.9PF

C1 5.6PF — L2 22NH — C5 1.0PF

L3 18NH — C10 2.7PF — L1 27NH

C11 2.7PF — C4 5.6PF — C2 6.8PF — C3 3.9PF

R20 0 — J5 — DUT FILTER OUT

SCLK SDIO SDO CSB IO_UPDATE RESET PWRDOWN GND S4 S3 VDD_DACDEC (1.8V) GND VDD_DAC3 (3.3V)

64 63 62 61 60 59 58 57 56 55 54 53 52 51 50 49

R1 10K — GND

(3.3V) SIO_VDD — 1 DVDD_IO
GND — 2 DVSS_1
(1.8V) DVDD — 3 DVDD_1
GND — 4 DVSS_2
(1.8V) DVDD — 5 DVDD_2
GND — 6 DVSS_3
(1.8V) DVDD — 7 DVDD_3
GND — 8 DVSS_4
S1 — 9 S1
S2 — 10 S2
(1.8V) AVDD — 11 AVDD_1
12 NC_1
13 NC_2
(3.3V) SIO_VDD — 14 AVDD3.3
15 NC_3
16 NC_4

U1
AD9912

48 DAC_RSET
47 VDD_DAC3_2 — VDD_DAC3 (3.3V)
46 VDD_DAC3_1 — VDD_DAC3 (3.3V)
45 AVDD_6 — VDD_DACCLK(1.8V)
44 AVDD_5
43 VSS_ISO — GND
42 VDD_FDBK — VDD_DRV (1.8V)
41 FDBK_IN
40 FDBK_INB
39 VSS_DRV_2 — GND
38 OUT_CMOS — OUT_CMOS
37 VDDX_DRV — VDDX_DRV (3.3V)
36 VDD_DRV — VDD_DRV (1.8V)
35 OUT
34 OUTB
33 VSS_DRV_1 — GND

17 NC_5 — 18 NC_6 — 19 AVDD_2 — 20 NC_7 — 21 NC_8 — 22 NC_9 — 23 AVDD_3 — 24 AVDD_4 — 25 VDD_SYSCLK_1 — 26 VDD_SYSCLK_2 — 27 SYSCLK — 28 SYSCLKB — 29 VDD_SYSCLK_3 — 30 VDD_SYSCLK_4 — 31 LOOP_FILTER — 32 CLKMODESEL

(1.8V) AVDD — (1.8V) AVDD — (1.8V HC) AVDD — (1.8V) VDD_SYSCLK — (1.8V) VDD_SYSCLK — SYSCLK — SYSCLKB — (1.8V) VDD_SYSCLK — (1.8V) VDD_SYSCLK

R135 510 — CLK MODE SELECT — GND — JMP1 — VDD_SYSCLK — DEFAULT POS

GND — R6 1K — R24 0

R3 OPT — C88 10PF — R98 2.2K — C83 180PF — VDD_SYSCLK

SYSCLK INPUT CIRCUITRY ON SHEET 4

DEVICE=ADT2-1T-1P
ADTT1-1 /CD542 PKG

R4 100 — 4 5 6 — 3 2 1 — GND

T2

R18 0 — J6 — FDBK_IN

R7 10K — R8 10K

GND — C9 0.1UF

R15 10K — GND — C13 10NF — J1 — OUT

R17 1K

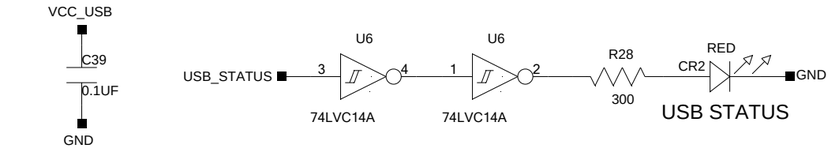
GND — C14 10NF — J2 — OUTB

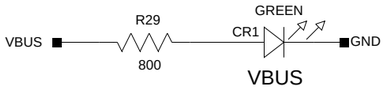
R16 10K — GND

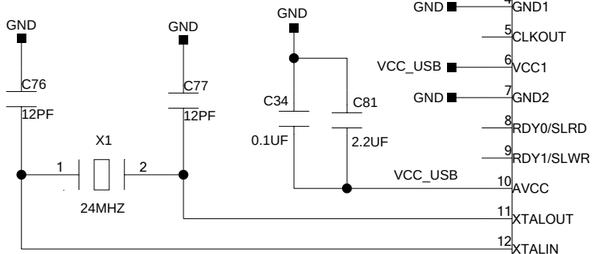
ANALOG DEVICES	HSC GREENSBORO 7910 TRIAD CENTER DRIVE GREENSBORO NC 27409	TITLE AD9912 EVALUATION BOARD	
DATE: 27 MAY 2008	SHEET 1 OF 4	DRAWN BY: W. CLARK	DRAWING NUMBER REV B

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

USB I/O

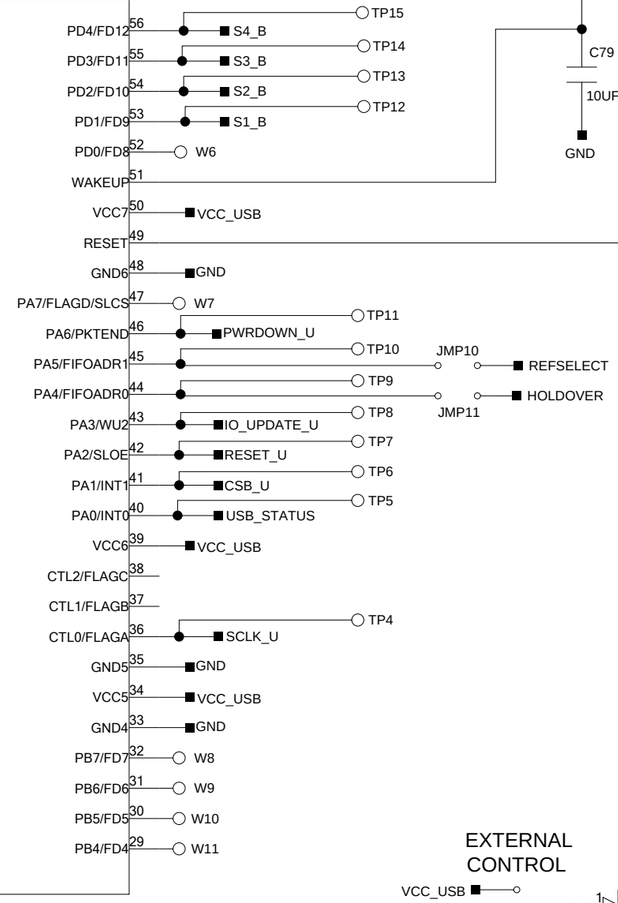


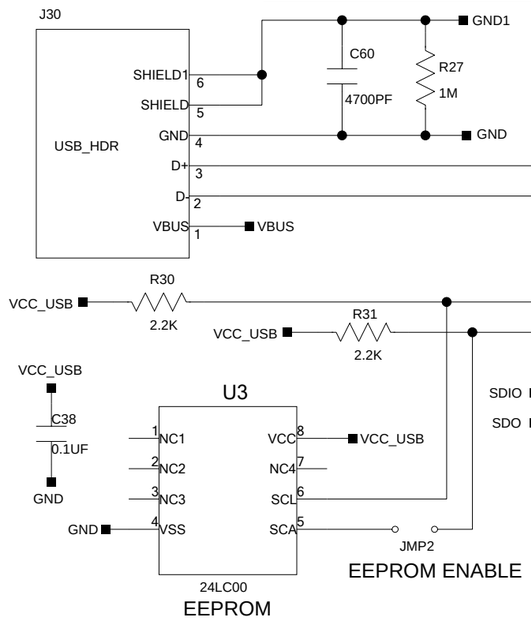


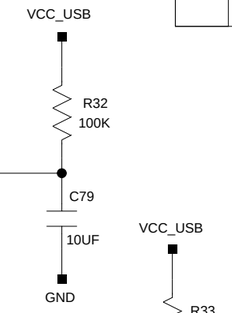


U2

CY7C68013A

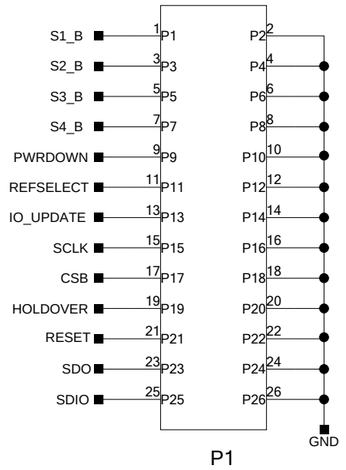




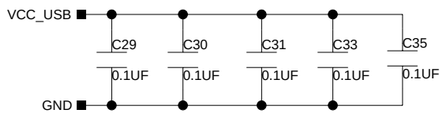


I/O HEADER

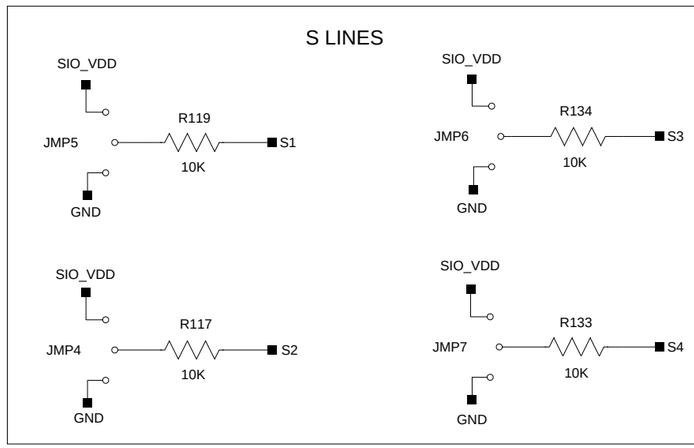
(PROBING/EXTERNAL CONTROL)



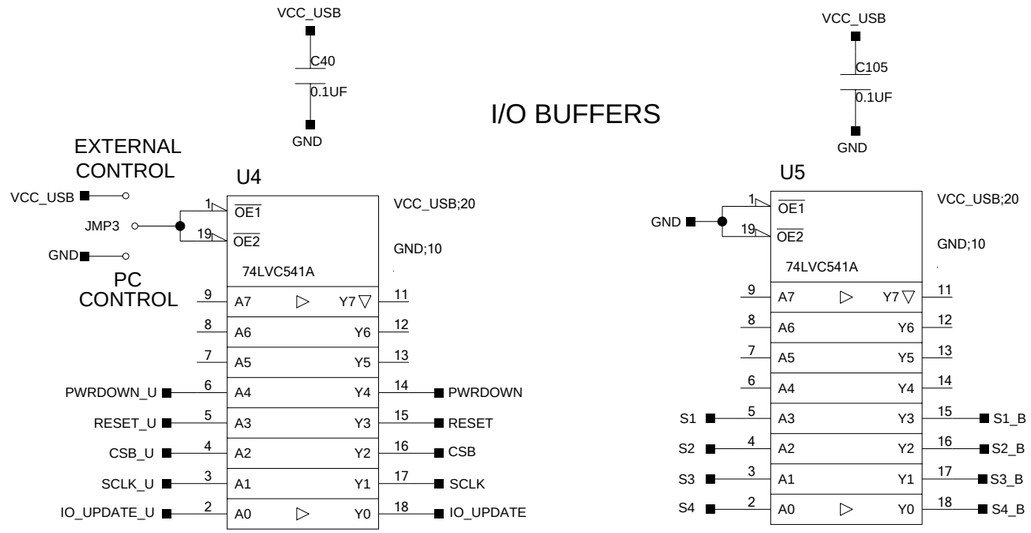
USB BYPASS CAPACITORS



S LINES



I/O BUFFERS

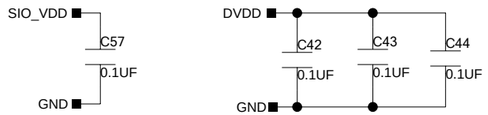


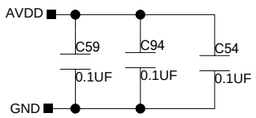
ANALOG DEVICES	HSC GREENSBORO 7910 TRIAD CENTER DRIVE GREENSBORO NC 27409	TITLE: AD9912 EVALUATION BOARD	
DATE: 12 DEC 2007	SHEET 2 OF 4	DRAWN BY: W. CLARK	DRAWING NUMBER / REV: B

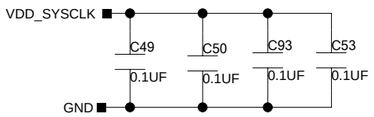
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

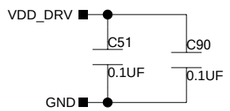
POWER SUPPLIES

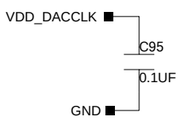
DUT BYPASS CAPACITORS

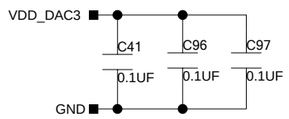


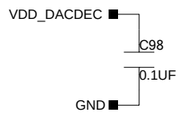


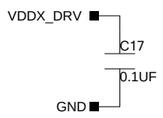




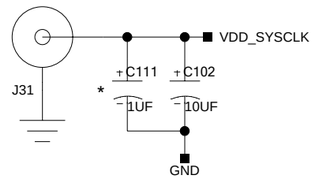




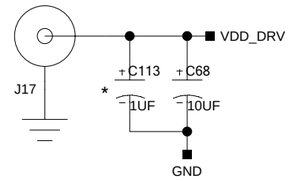




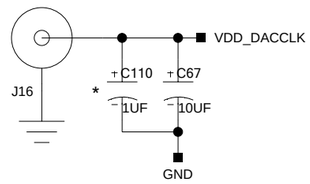
VDD_SYSCLK (1.8V)



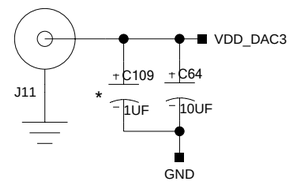
VDD_DRV/VDD_FDBK (1.8V)



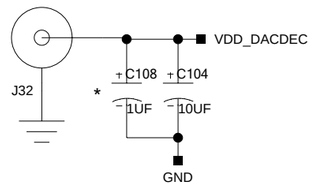
VDD_DACCLK (1.8V)



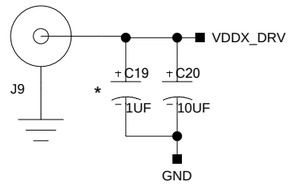
VDD_DAC3 (3.3V)



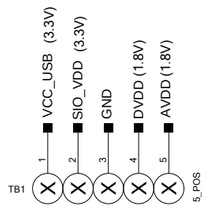
VDD_DACDEC (1.8V)

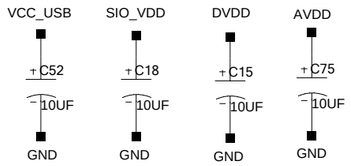


VDDX_DRV (3.3V)

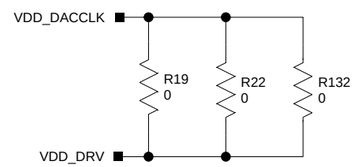


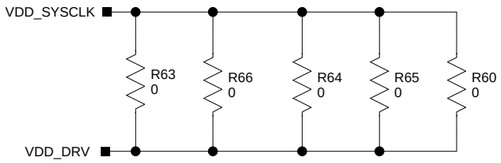
* 1 uF CAP ON BOTTOM SIDE IS OPTIONAL

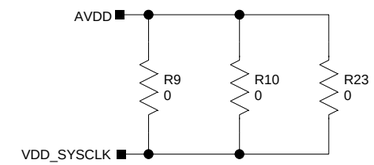




OPTIONAL 1.8V POWER PLANE STITCHING



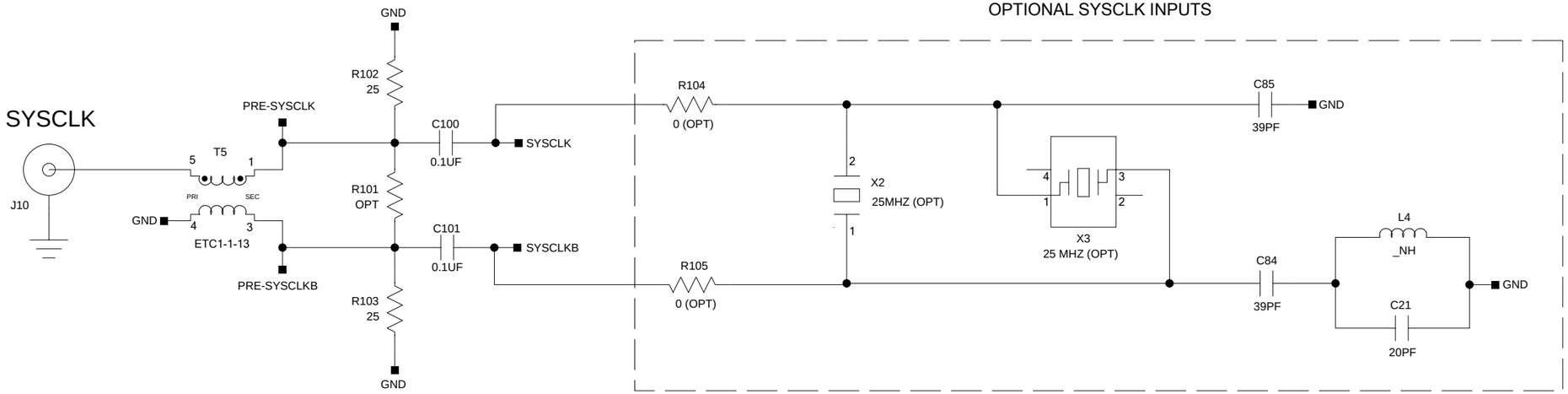




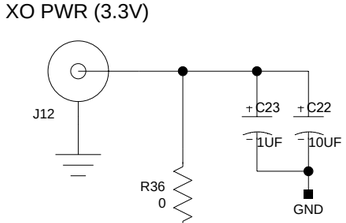
ANALOG DEVICES	HSC GREENSBORO 7910 TRIAD CENTER DRIVE GREENSBORO NC 27409	TITLE: AD9912 EVALUATION BOARD	
DATE: 12 DEC 2007	SHEET 3 OF 4	DRAWN BY: W. CLARK	DRAWING NUMBER / REV: B

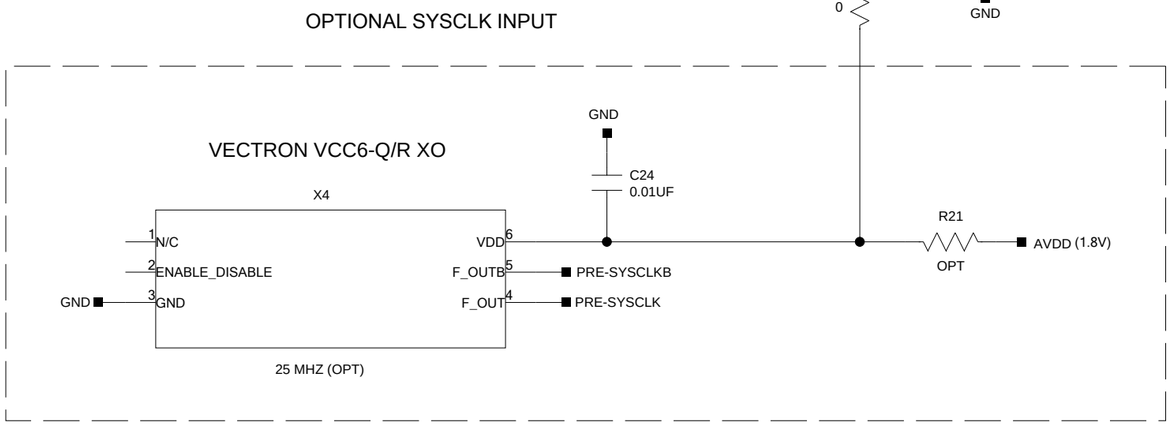
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED

IF USING ONE OF THE CRYSTALS OR THE XO (INSTEAD OF T5):
REMOVE C100, C101 & INSTALL ASSOCIATED BOXED ITEMS



DEFAULT: DO NOT INSTALL BOXED ITEMS





DEFAULT: DO NOT INSTALL BOXED ITEMS

ANALOG DEVICES

HSC GREENSBORO
7910 TRIAD CENTER DRIVE
GREENSBORO NC 27409

TITLE: AD9912 EVALUATION BOARD

DRAWING NUMBER

REV: B

DATE: 12 DEC 2007 | SHEET 4 OF 4 | DRAWN BY: W. CLARK