ANALOG DEVICES

Circuit Note
CN-0302

Circuits from the Lab™ Reference Circuits

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0302.

Devices Connected/Referenced	
ADF4159	13 GHz Fractional-N Frequency Synthesizer
AD8065	High Performance 145 MHz *FastFET*™ Op amp

Ultra-Fast Settling PLL with RF to 13 GHz

EVALUATION AND DESIGN SUPPORT

Design and Integration Files

Schematics, Layout Files, Bill of Materials, ADIsimPLL Simulation File

CIRCUIT FUNCTION AND BENEFITS

The PLL circuit shown in Figure 1 uses a 13 GHz Fractional-N synthesizer, wideband active loop filter and VCO, and has a phase settling time of less than 5 µs to within 5° for a 200 MHz frequency jump.

The performance is achieved using an active loop filter with 2.4 MHz bandwidth. This wide bandwidth loop filter is achievable because of the ADF4159 phase-frequency detector (PFD) maximum frequency of 110 MHz; and the AD8065 op amp high gain-bandwidth product of 145 MHz.

The AD8065 op amp used in the active filter can operate on a 24 V supply voltage that allows control of most wideband VCOs having tuning voltages from 0 V to 18 V.

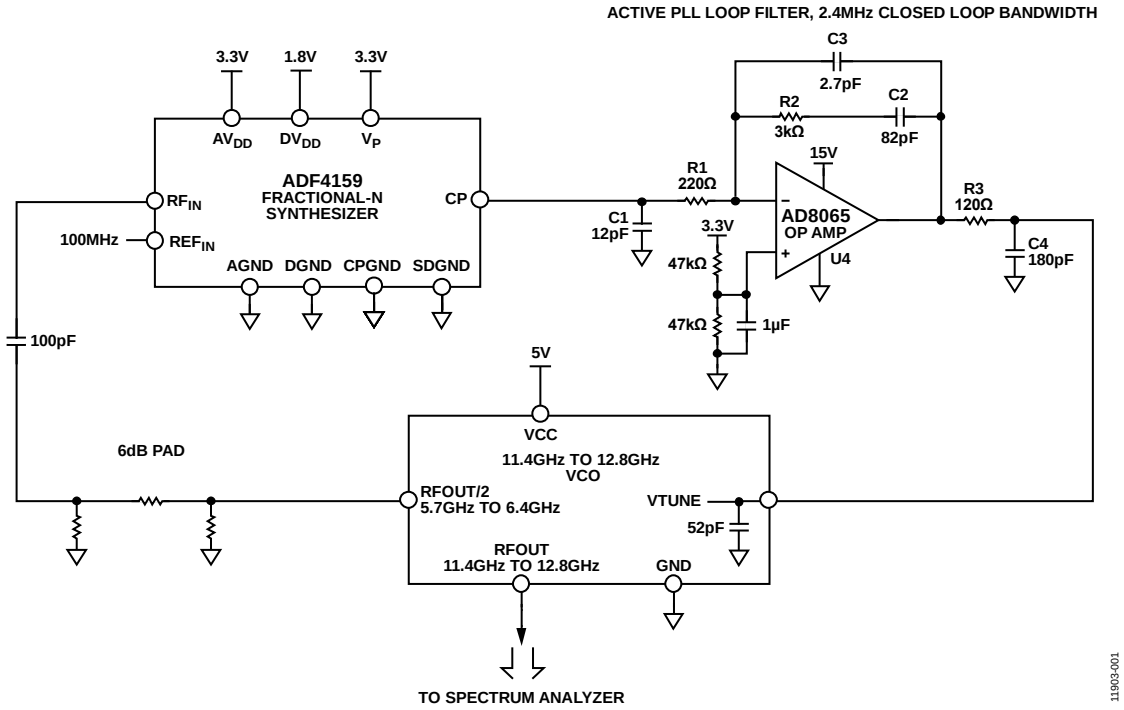

Figure 1. Block Diagram of ADF4159, AD8065 Active Loop Filter, and 11.4 GHz to 12.8 GHz VCO. (Simplified Schematic: All Connections and Decoupling Not Shown)

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

CIRCUIT DESCRIPTION

In a PLL and VCO frequency synthesis system, achieving less than 5 µs frequency and phase settling time requires a very wide loop bandwidth. The loop bandwidth (LBW) defines the speed of the control loop. A wider LBW allows for faster settling time, at the expense of less attenuation of phase noise and spurious signals.

The circuit in Figure 1 operates by locking the ADF4159 to the RF_{OUT}/2 signal (~6 GHz) of the 12 GHz VCO (MACOM MAOC-009269). However, VCOs up to 24 GHz that have a RF_{OUT}/2 signal can be used with the ADF4159, since it accepts RF inputs up to 13 GHz.

ADF4159 Fractional-N Synthesizer

In a Fractional-N architecture PLL, the noise from the sigma-delta modulator (SDM) peaks at half the PFD frequency (f_{PFD}). For example, if a Fractional-N PLL has a PFD frequency of 32 MHz, then the unfiltered SDM noise peaks at 16 MHz. The SDM noise will make the loop unstable, and the PLL will not lock. Figure 2 shows a simulated phase noise plot of this condition.

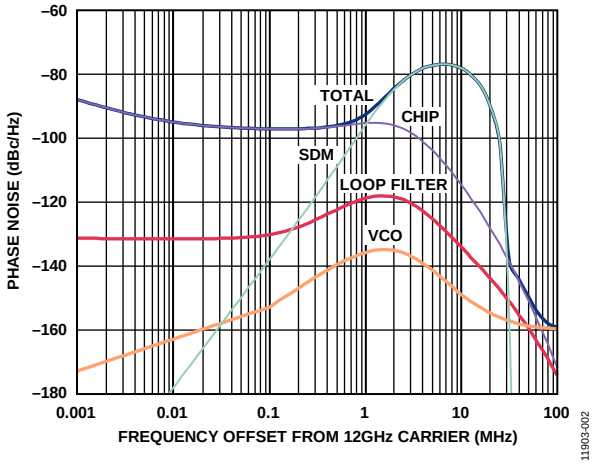

Figure 2. Phase Noise Plot at 12 GHz Output with f_{PFD} = 32 MHz and LBW = 2.4 MHz

The ADF4159 has a maximum PFD frequency of 110 MHz. This means that the unfiltered SDM noise peaks at 55 MHz. Figure 3 shows a phase noise plot with a PFD frequency of 110 MHz. The SDM noise occurs at a large offset from the carrier and is therefore filtered by the loop filter.

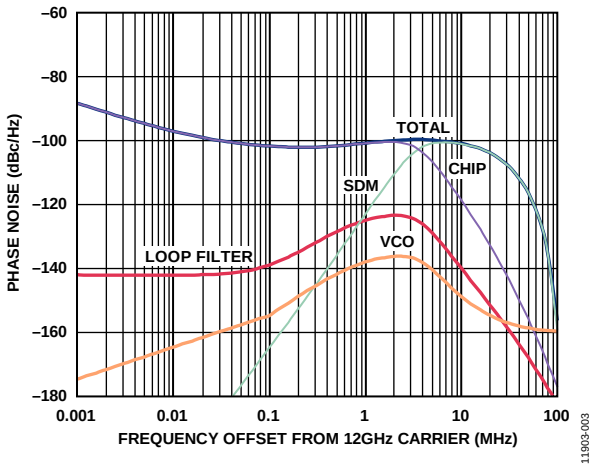

Figure 3. Phase Noise Plot at 12 GHz Output with f_{PFD} = 110 MHz and LBW = 2.4 MHz

The ADF4159 high maximum PFD frequency is also important because it is recommended to keep the LBW less than 1/10 of the PFD frequency to ensure stability.

The ADF4159 has a maximum RF input frequency of 13 GHz. In the configuration of this circuit, the ADF4159 is actually being driven with the VCO RF_{OUT}/2 signal. This means that when the VCO primary output is 12 GHz, the ADF4159 is actually locking to 6 GHz.

This configuration means a 24 GHz VCO can be used so that the RF_{OUT}/2 signal, of 12 GHz, is fed back to the ADF4159. The evaluation board has a footprint capable of supporting a variety of 32-lead 5 mm × 5 mm LFCSP VCOs.

The supply voltage for the ADF4159 internal charge pump is 3.3 V. However, many wide-band VCOs require a tuning voltage of up to 18 V. To handle this, an active loop filter is required. The active filter multiplies the output tuning range of the ADF4159 by the gain of the op amp. For more detail, see the AD8065 section of this circuit note.

The ADF4159 supports a programmable charge pump current feature. This feature allows the user to easily modify the loop filter dynamic without changing the physical components. In this circuit, the LBW was designed for 2.4 MHz at a charge pump current of 2.5 mA. The charge pump current can be reduced in order to reduce the LBW without physically changing the loop filter components.

The ADIsimPLL simulation for the circuit can be found at the CN0302 Design Support Package located at (http://www.analog.com/CN0302-DesignSupport).

Active Filter Using the AD8065

The AD8065 op amp has a 24 V supply voltage range, a gain bandwidth product (GBP) of approximately 145 MHz, and low noise (7 nV/√Hz). These features make it ideal for an active filter.

For most PLL applications, a phase margin of 45° to 55° is recommended to maintain a stable loop and to minimize settling time. In an active loop filter, i.e. when there is an op amp in a loop filter, an additional pole occurs at the unity gain frequency (or gain bandwidth product) of the op amp. This additional pole adds extra phase lag, so, depending on the frequency of the pole, it can render the loop unstable.

Table 1. Phase Lag as a Function of GBP:LBW Ratio

GBP/LBW Ratio	Extra Phase Lag (°)
5 (e.g. GBW = 1 MHz, LBW = 200 kHz)	11.3
10	5.7
20	2.9

The higher the ratio of GBP to LBW, the less phase lag. For example, Table 1 shows that a GBP/LBW ratio of 10 will reduce the phase margin by 5.7°. If the GBP/LBW ratio is too low, the phase margin will also become too low and result in an unstable loop.

This circuit uses a 2.4 MHz LBW, so the AD8065 145 MHz GBP results in negligible phase lag (GBP/LBW = 60).

Comparison with OP184 Active Filter

The OP184 is a frequently used op amp in active filter PLL applications. However, the OP184 is not suitable for very wide LBW applications due to its 4 MHz GBP. Some optimization of the phase margin will allow the use of the OP184 at wide LBWs, but ultimately, the OP184 will limit the maximum LBW.

The op amp in the active filter is configured in the inverting mode, therefore the ADF4159 is programmed with a negative phase-detector polarity. The inverting configuration is easier to implement because the op amp positive input can be biased at a fixed voltage that does not change with the op amp output (as it would in the non-inverting configuration).

The AD8065 also acts as a buffer to mitigate the input capacitance of the VCO. For a 2.4 MHz LBW passive filter, the combined capacitance of the VCO input and the last capacitor in the filter must be approximately 1.5 pF. However, the VCO measured input capacitance alone is 52 pF.

Ceramic C0G/NP0 capacitors (which discharge quicker than standard capacitors) are recommended for the loop filter capacitors to minimize phase settling time.

Excellent layout, grounding, and decoupling techniques are required for the circuit as described in Tutorials MT-031 and MT-101. A complete schematic, layout files, and bill of materials can be found in the CN-0302 Design Support Package (www.analog.com/CN0302-DesignSupport).

Test Results

The measured phase noise of the circuit is shown in Figure 4. Frequency and phase settling time for a 200 MHz jump in frequency are shown in Figure 5 and Figure 6, respectively.

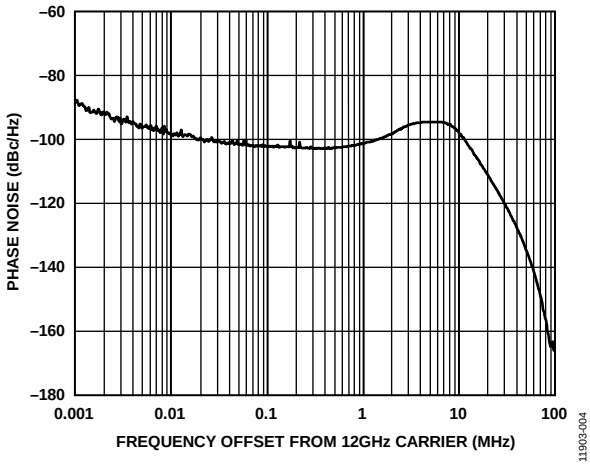

Figure 4. Phase Noise at 12.002 GHz; LBW = 2.4 MHz

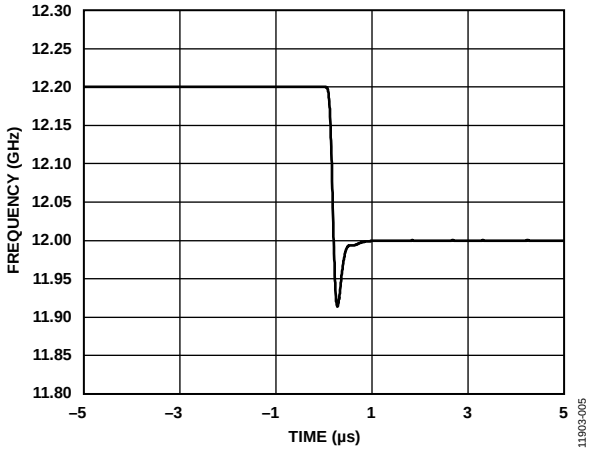

Figure 5. Frequency Settling for a 200 MHz Jump from 12.2 GHz to 12.0 GHz

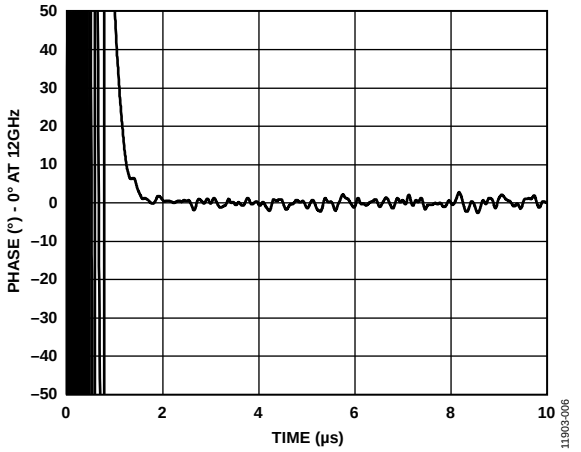

Figure 6. Phase Settling for a 200 MHz Jump from 12.2 GHz to 12.0 GHz

CIRCUIT EVALUATION AND TEST

PC Board Modifications for 2.4 MHz Active Filter

The following modifications to the standard EV-ADF4159EB1Z are required to implement the 2.4 MHz active filter using the AD8065 rather than the OP184:

- Replace U4 with AD8065ARZ (8-lead, SOIC)
- Replace R1 with 220 Ω, 1%, 0603
- Replace R2 with 3 kΩ, 1%, 0603
- Replace R3 with 120 Ω, 1%, 0603
- Replace C1 with 12 pF, 10%, 0603
- Replace C2 with 82 pF, 10%, 0603
- Replace C3 with 2.7 pF, 5%, 0603
- C4 is not changed and remains 180 pF

Equipment Required

- EV-ADF4159EB1Z evaluation board modified for AD8065 op amp and 2.4 MHz LBW filter components
- ADF4159 evaluation software
- Windows® PC with USB port
- +15 V power supply
- +5.5 V power supply
- Spectrum Analyzer: R&S: FSUP26, FSQ26, FSW26, Agilent E5052B or equivalent.

Functional Block Diagram of Test Setup

A functional diagram of the test setup is shown in Figure 7, and a photo of the setup is shown in Figure 8. Refer to User Guide UG-383 for details on running the tests and setting up the software.

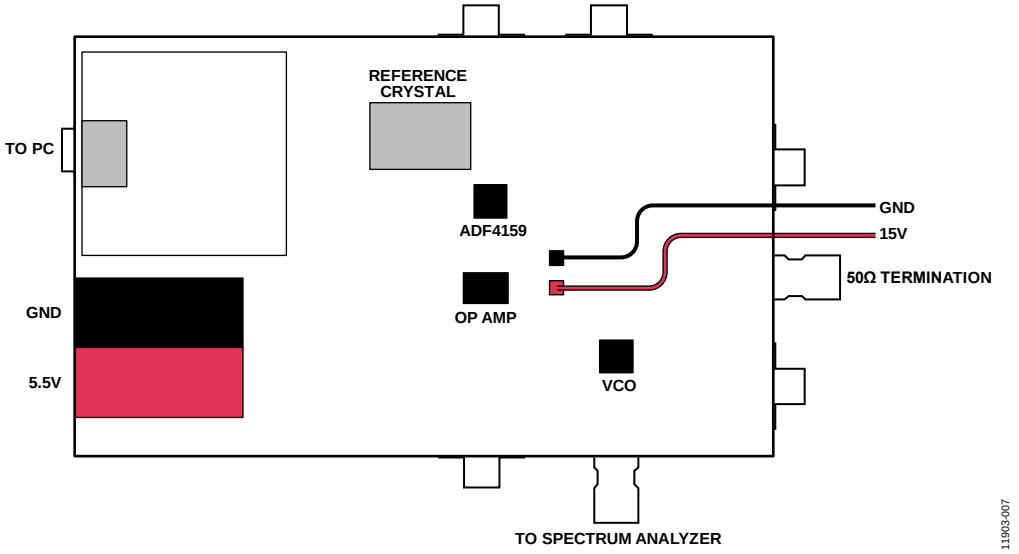

Figure 7. Functional Block Diagram of Test Setup

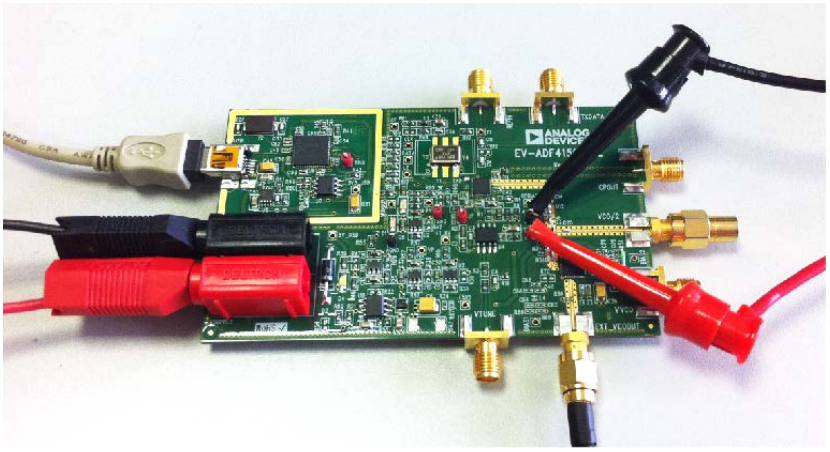

Figure 8. Photo of EV-ADF4159EB1Z Board and Test Setup Showing External Connections

Learn More

CN-0302 Design Support Package:
http://www.analog.com/CN0302-DesignSupport

ADIsimPLL Design Tool

AN-30 Application Note, Ask the Application Engineer—PLL Synthesizers, Analog Devices

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-086 Tutorial, *Fundamentals of Phase Locked Loops (PLLs)*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

UG-383: Evaluating the ADF4159 Frequency Synthesizer for Phase-Locked Loops

Data Sheets and Evaluation Boards

ADF4159 Data Sheet and Evaluation Board

AD8065 Data Sheet

REVISION HISTORY

10/13—Revision 0: Initial Version