Selecting PLLs for timing and phase control

The behavior of PLL parts needs to be characterized in applications where phase control is of particular interest

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Phase-locked loops (PLLs) are extensively used in wireless communications. In base-station applications, their principal use is to provide a stable, low-noise RF local oscillator (LO) for the up-conversion and down-conversion in transmitters and receivers. However, because of their nature, PLLs can also be used to control the timing of clocking signals in many other circuits, and in some applications, can be substituted for more expensive timing chips if used correctly.

Most designers of high-speed digital circuits will opt for expensive timing chips in phase-critical applications because the timing specifications are usually characterized extensively for a limited frequency range (typically the line rates for SONET/SDH frequencies). In contrast, PLL parts usually cover a wide range of frequencies and are usually not specified with respect to phase control or timing. This is due in part to the infinite number of input and output frequencies used and the various combinations of multiplication and divide ratios possible.

Hence the phase delay characteristics are rarely examined and almost never published on PLL datasheets. Characterizing PLL parts for each particular application is recommended because different applications will require different configurations and requirements, which may provide different results.

Phase delay between two different parts
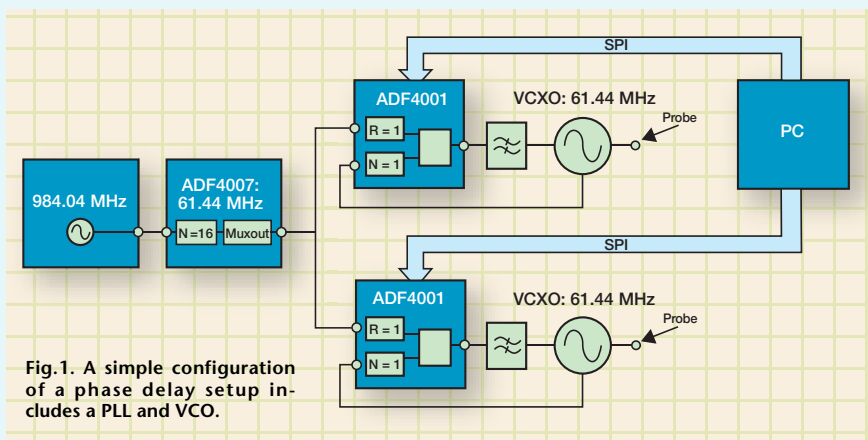
The initial characterization included

Fig.1. A simple configuration of a phase delay setup includes a PLL and VCO.

an examination of the phase skew between two VCO output signals from two PLL parts driven with the same reference (REF) clock. This was undertaken in the belief that if the variation of the REF-to-RF propagation delay from part to part is large and unpredictable, it follows that the use of PLL parts in phase control applications is limited indeed.

Using a low-frequency PLL, such as the ADF4001 from Analog Devices, the simplest configuration is to use the PLL and an external VCXO (see *Fig. 1*). The reference (R) and feedback (N) divider value can both be programmed to equal 1. This effectively means the PLL can act as a clock cleaning circuit, a common application of PLL parts.

To ensure both reference counters on each part are clocked at the same moment as much as possible, a low-noise, short-rise-time square wave needs to be used. To achieve this, a high-frequency divider is used to divide a 984.04-MHz sine wave by 16, outputting a 61.44-MHz high-slew-rate square wave.

Of particular importance is to keep the distance travelled by the signal

through each PLL from the splitter to the REF_{IN} pin for each part exactly the same. This ensures both parts are clocked at the exact same time by the clock pulse.

A further consideration is to ensure the counters in both PLL parts are reset at the same time. This can be accomplished by first writing the desired contents to the PLL registers and then activating both chips by bringing the chip-enable (CE) of both parts high at the same time. This function can also be achieved using the counter reset function in software.

To ensure measurement accuracy, active oscilloscope probes (P6243) were used with a high-frequency digital phosphor oscilloscope (TDS 3054). This largely preserves the shape of the square wave and facilitates an easy comparison between the two waveforms. The resulting plot on the oscilloscope showed a delta of 60 ps between the two almost-identical output signals.

Another way of making this measurement is to use a gain and phase detector to measure the gain and phase difference between two different signals. For this experiment the

Fig. 2. A high-speed oscilloscope plot shows that the skew between both signals to be in phase.

VCXO outputs from both PLLs were fed to the inputs of the gain and phase detector.

Care was taken again to ensure identical cables of equal length carried the RF signals to the inputs on the gain and phase detector. The resulting signal output from the phase output was 1.85 V, which exceeds the expected datasheet value of 1.8 V equivalent to a 0° phase difference.

REF-to-RF phase delay

Having established that the propagation delay from the REF to RF is very similar between PLL parts, the next task was to determine the phase relationship between the REF and the RF VCO output signal. A low REF-to-RF delay is ideal, as this allows the part to be used more easily in clock cleanup and distribution circuits.

For this experiment, a single-chip integer-N PLL synthesizer with an integrated voltage-controlled oscillator (VCO) was selected. The part used is similar to the ADF4001, but with the addition of a bipolar prescaler (which enables both a higher frequency range and higher divider values) plus an integrated on-chip VCO. The experiment can also be performed with external VCO parts, but the trace length between the VCO output and the feedback N divider will affect the phase relationship. This parameter is insignificant on an integrated PLL as the VCO is practically next to the feedback counters.

Again, a high-slew-rate square wave should be used as the reference. This time the PLL was used as a clock multiplier, multiplying 20.48 MHz internally to 491.52 MHz, while the use of the output divide-by-2 function gave

an output of 245.76 MHz.

To achieve this output, the 20.48 MHz signal was divided by 8 in the R counter giving a PFD frequency of 2.56 MHz. Use of a high PFD allows the use of a smaller N value, which is best for close-in phase noise, as any noise on the reference is increased by 20 log (N). The overall feedback ratio is 192.

To make the measurement, the same equipment as earlier was used, but the measurement was made as closely as possible to the REF and RF pins. The phase delay from input to output is very small (less than 140 ps). The actual delay is probably less than can be easily measured with the oscilloscope. This delay value increases with a temperature increase and decreases (sometimes below 0 ps) with a temperature decrease. Similar variations occur with supply voltage, but experiments in this configuration have shown the delay over the voltage range (3.0 to 3.6 V) and temperature range (–40° to 85°C) to always be within a delay range of ±500 ps.

The first experiment was then repeated for an output frequency of 400 MHz for two single-chip integer-N PLL synthesizers with on-chip VCOs. Using a gain and phase detector showed the skew between both signals to be in phase as much as the phase detector could show.

A high-speed oscilloscope plot (see *Fig. 2*) largely confirmed this. Anomalies in the waveform are due to output component mismatches, which affect the output power. However, a close examination of the waveform peaks shows the signals to be largely in phase.

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Comments

Needs additional corrections	AAs	Final—ready for pdf