# AD9516 DEBUG PROCEDURE STEP BY STEP

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This note will help engineer to debug AD9516 step by step to try to identify which circuit that results in the “ad9516 has no output”.

Step0: Hardware Connections Check

Make sure all power supplies (VS, VCP, VS_LVPECL) are connected to correct.

/SYNC=High

/PD=High

/RESET=High,

Important Note 1, Remove RC reset network typically found in CPU application.

Step1: SPI Write/Read Check

Write REG0x11=0xAA

Write REG0x232=0x01

Read REG0x11, it should be 0xAA

Note 2, AD9516 default SPI is 3 line mode. User can change it to 4 line mode by enable SDO bit in REG0x000.

Step2: Use AD9516/7/8 Evaluation Software to generate correct .stp file for AD9516

Step3: Load .stp file registers in sequence to AD9516

Step4: IO_Update

Write REG0x232=0x01

Step5: VCO Calibration,

Write REG0x18[0]=0

Write REG0x232=0x01

Write REG0x18[0]=1

Write REG0x232=0x01

Wait 500ms

Important Note 3, make sure that selected reference be valid when doing VCO calibration

Step6: IO_Update

Step7: Check Key Status Register

Read REG0x1F to check AD9516

Step8: Sync output (Optional)

Write REG0x230[0]=1

Write REG0x232=0x01

Write REG0x230[0]=0

Write REG0x232=0x01

Important Note 4, at this point, AD9516 should output correct frequencies. If not, do the following

Step9: Route reference divider output to STATUS pin and check waveform with oscilloscope, it should be square wave with frequency equals to fref/R

Write REG0x17[7:2]=000 010

Write REG0x232=0x01

Note 5, if no dynamic waveform, the reference is not accepted by AD9516, check reference receiver circuit.

Step10: Route N divider output to STATUS pin and check waveform with oscilloscope, it should be square wave with frequency equals to VCO/(PB+A)

Write REG0x17[7:2]=000 001

Write REG0x232=0x01

Note 6, if no dynamic waveform, VCO calibration may not be successful.

Step11: If SPI read is not available, user can use switching STATUS pin low/high to check SPI write operation

Write REG0x17[7:2]=000 000 (STATUS=GND)

Write REG0x232=0x01

Write REG0x17[7:2]=110 000 (STATUS=VS)

Write REG0x232=0x01

Step 12: Read back all the registers and do comparison with the .stp file,

Step 13: Send 1) the .stp file 2) readback registers content 3) AD9516 related schematic to ADI local FAE for further analysis

PLL loop stability

Try to reproduce issue in lab

## APPENDIX

1. SPI Timing- 3 Line SPI Write REG0x11=0xAA


Total 24 SCLK cycles in one /CS low period: 0, 1, 2, …, 23. On each rising edge of SCLK, AD9516 samples SPI command (address+data).

2. SPI Timing- 3 Line SPI Read REG0x11=0xAA


Total 23 SCLK cycles in one /CS low period, 0, 1, 2, …, 22. On the 15$^{th}$ falling edge of SCLK, AD9516 output data[7] via SDIO, On the the 22$^{th}$ falling edge of SCLK, AD9516 output data[0] via SDIO.

3. SPI Timing- 4 Line SPI Write REG0x11=0xAA


Total 24 SCLK cycles in one /CS low period: 0, 1, 2, …, 23. On each rising edge of SCLK, AD9516 samples SPI command (address+data).

4. SPI Timing- 4 Line SPI Read REG0x11=0xAA


Total 23 SCLK cycles in one /CS low period, 0, 1, 2, …, 22. On the 15$^{th}$ falling edge of SCLK, AD9516 output data[7] via SDO, On the the 22$^{th}$ falling edge of SCLK, AD9516 output data[0] via SDO.