ANALOG DEVICES

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APPLICATION NOTE

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Design Considerations for the ADV7441A/AD9388A Internal EDID

by the ATV Video Applications Group

INTRODUCTION

The ADV7441A and AD9388A are high quality graphics digitizers. These devices feature an internal RAM dedicated to storing extended display identification data (EDID) images. This feature allows you to save up to two EDID storage devices, which reduces the overall BOM cost of a high definition multi-media interface (HDMI) application.

This application note outlines the hardware and software considerations to take into account when building HDMI-compliant applications that use internal EDID and are fully compliant to the latest HDMI and high bandwidth digital content protection (HDCP) specifications. Consult the ADV7441A/AD9388A hardware manuals in conjunction with this application note. Contact your local Analog Devices, Inc., field applications engineer to receive the latest ADV7441A and AD9388A hardware manuals.

HDMI AND HDCP SPECIFICATION REQUIREMENTS

The five EDID-related requirements are found in the HDMI and HDCP industry specifications (these specifications are listed in the References section of this application note). The first four requirements are taken directly from the HDMI specifications while the fifth requirement is part of the HDCP specifications (see the References section.)

1. "All sinks shall contain a CEA-861-D compliant E-EDID data structure accessible through the DDC."
2. "The sink should be capable of providing E-EDID information over the enhanced DDC channel whenever the +5 V power signal is provided. This should be available within 20 msec after the +5 V power signal is provided."
3. "An HDMI sink shall not assert high voltage level on its hot plug detect pin when the E-EDID is not available for reading. This requirement shall be fulfilled at all times, even if the sink is powered-off or in standby."
4. "An HDMI sink shall indicate any change to the contents of the E-EDID by driving a low voltage level pulse on the hot plug detect pin. This pulse shall be at least 100 ms."
5. "The detection of hot plug detect indicates that a sink device is attached and that the EDID ROM is available for reading."

The first requirement, from the HDMI specifications, is required for all HDMI sinks, which must integrate an EDID storage device accessible to an HDMI source through the display data channel (DDC) on the HDMI interface.

The second requirement, also from the HDMI specifications, states that the EDID should always be available on the DDC bus if the source provides a +5 V power signal, even if the sink is powered down. This requirement, which uses the conformance level word *should*, is not mandatory and can be disregarded unless the application requires that the E-EDID be available in power-down mode, such as with applications that support the consumer electronic control feature.

The HDMI and HDCP requirements for the EDID can be rephrased in the following four rules, which should be followed for an HDMI design:

1. All HDMI sinks must have CEA-861-compliant E-EDID connected to the DDC bus.
2. The only function of the hot plug detect (HPD) is to indicate that the E-EDID can be accessed.
3. The HDP signal must be asserted low if the E-EDID is not accessible.
4. The HDP signal must be asserted low for a minimum of 100 ms to indicate a change in the E-EDID.

FIRMWARE DESIGN

The four EDID-related rules lead to the definition of firmware routines that must be implemented to correctly use the internal EDID feature of the ADV7441A/AD9388A.

Keep HPD Deasserted During Chip Power-Down

The internal EDID is not accessible when the chip is powered down or when the crystal clock is disabled.

The HPD must be deasserted for any of the following cases:

- The power supplies to the ADV7441A/AD9388A are turned off.
- The ADV7441A/AD9388A are powered down by setting the 2-bit PWRDN field, Bits [1:0], to 0x3. This field is located in the User Map, Register 0x0F.
- The ADV7441A/AD9388A are placed in power saving mode by setting the field PWRSAV to 1. This field is located in the User Map, Register 0x0F.

Configure the EDID at Power-Up

The EDID, being RAM based, must be programmed when the ADV7441A/AD9388A are powered up. The HPD should be deasserted for a minimum of 100 ms during the configuration of the internal EDID (see Figure 1).

Deassert HPD During Reset

The ADV7441A/AD9388A can be reset by using either of the following two methods:

- A software reset is done by setting the chip reset bit in User Map Register 0x0F, Bit 7, to 1.
- A hardware reset is done by asserting the reset pin low for a minimum of 5 ms.

The internal EDID stays active and accessible by an external HDMI transmitter while the ADV7441A/AD9388A are reset. The transition minimized differential signaling (TMDS) clock and data terminations are disabled and the HDCP engine is reset upon a hardware or software reset. Therefore, it is recommended to keep the HPD deasserted, the TMDS clock and data terminations disabled, and the internal EDID disabled for a minimum period of 100 ms upon reset. This prevents the HDMI transmitter, connected to the active port of the ADV7441A/AD9388A, from accessing the internal EDID.

The HDMI transmitter also restarts HDCP authentication when the HPD is reasserted and the terminations are again enabled (see Figure 2).

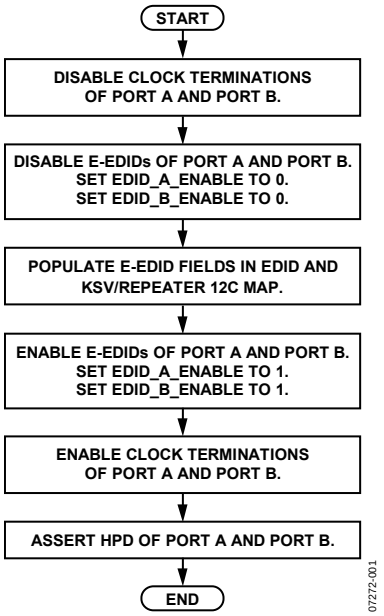

Figure 1. Configuring Internal EDID for Port A and Port B

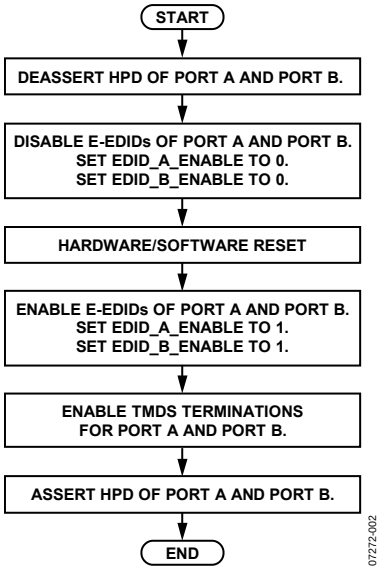

Figure 2. Deasserting HPD During Reset.

HARDWARE CONFIGURATION

A reference schematic for the hardware required to use the internal EDID of the ADV7441A/AD9388A is provided (see Figure 3). Note that an external controller is required to assert and deassert HPD by driving the HPD-CONTROL signal.

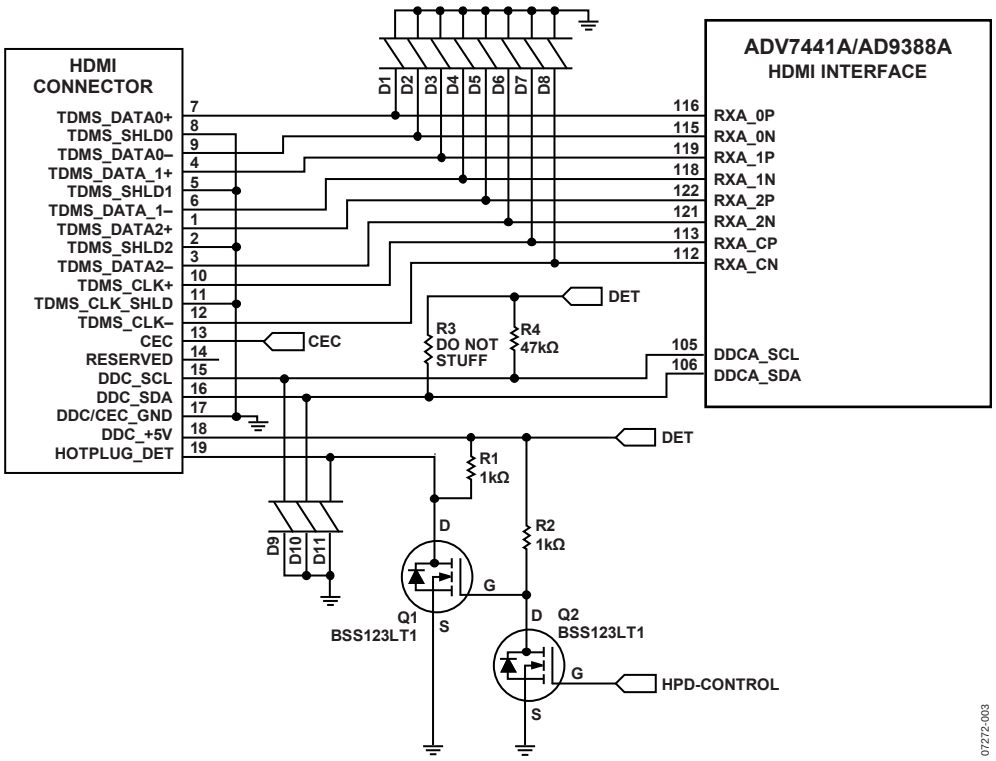

Figure 3. Hardware Requirements for Internal EDID on Port A

LOW POWER MODE

Setting the ADV7441A/AD9388A in power-down or power saving mode stops the crystal clock used to clock the EDID controller. The EDID is effectively disabled in power-down or power saving mode.

It is possible to put the device into an alternative low power mode that keeps the EDID controller active. This alternative low power mode is set by a series of I²C® writes detailed in the following subsections.

Alternative Low Power Mode in HDMI Mode

To set the alternative low power mode in HDMI mode

1. Set CORE_PD to 1 (User Map, Register 0x13, Bit 4).
   This write stops all clocks except the crystal clock, which is the only clock required for the internal EDID.
2. Set User Map Register 0xBA, Bit 5, to 0.
   Set User Map Register 0xBA, Bit 7, to 1.
   These writes power down the HDMI core, which lowers the CVDD current.
3. Set CLOCK_TERM_PORT_A to 1 (HDMI Map, Register 0x1, Bit 6).
   Set CLOCK_TERM_PORT_B to 1 (HDMI Map, Register 0x1, Bit 5).
   These writes disable the clock and data terminations for both Port A and Port B to lower the TVDD current.

Alternative Low Power Mode in Analog Mode

To set the alternative low power mode in analog mode

1. Set CORE_PD to 1 (User Map, Register 0x13, Bit 4).
   This write stops all clocks except the XTAL clock crystal clock, which is the only clock required for the internal EDID.
2. Set User Map, Register 0xBA, Bit 5, to 0.
   Set User Map, Register 0xBA, Bit 7, to 1.
   These writes power down the HDMI core which lowers the CVDD current.
3. Set Reserved Map, Register 0x54, to 0x19 to power down the ADC band gap and reference buffer. Note that the default value of the Reserved Map, Register 0x54 is 0x1.
4. Set PDN_ADC0 to 1 (User Map, Register 0x3A, Bit 3).
   Set PDN_ADC1 to 1 (User Map, Register 0x3A, Bit 2).
   Set PDN_ADC2 to 1 (User Map, Register 0x3A, Bit 1).
   Set PDN_ADC3 to 1 (User Map, Register 0x3A, Bit 0).
   These writes disable all four ADCs of the analog front end. Note that the last write (PDN_ADC3, above) applies only to the ADV7441A.
5. Set CLOCK_TERM_PORT_A to 1 (HDMI Map, Register 0x1, Bit 6).
   Set CLOCK_TERM_PORT_B to 1 (HDMI Map, Register 0x1, Bit 5).
   These writes disable the clock and data terminations for both Port A and Port B to lower the TVDD current.

Table 1. Normal Mode and Alternative Power-Down Currents Measurements.

Mode	I_{AVDD} (mA)	I_{PVDD} (mA)	I_{TVDD} (mA)	I_{DVDDIO} (mA)	I_{DVVD} (mA)	I_{CVDD} (mA)
HDMI 1080i60 Normal	0.0012	8	120	74	11	80
HDMI 1080i60 Power-Down	0.0005	8	12	3	8	6
Analog CVBS Normal	62	15	166	72	18	80
Analog CVBS Power-Down	8	13	3	3	9	6
Analog Graphic 640 x 480 @ 60 Normal	159	7	67	72	14	80
Analog Graphic 640 x 480 @ 60 Power-Down	1.77	1	8	3	8	6
Analog Component 1080i60 Normal	165	19	126	72	16	80
Analog Component 1080i60 Power-Down	1.77	1	10	3	10	6

FREQUENTLY ASKED QUESTIONS

Questions frequently asked by customers, along with the answers, are provided here.

Are external EDID storage devices also supported by the ADV7441A/AD9388A?

Yes. The internal EDID can be enabled or disabled on a specific port, thus allowing the use of an external EDID. The internal EDID is disabled by setting EDID_A_ENABLE to 0 for HDMI Port A and setting EDID_B_ENABLE to 0 for HDMI Port B.

Does the internal EDID fully support the 256-byte data structure specified in the HDMI specification?

Yes. The internal EDID RAM supports the EDID 1.3 and the CEA extension data structure.

Is the internal EDID read-only via the DDC bus?

Yes. The internal EDID is read-only via the DDC lines. The internal EDID is, therefore, seen as a ROM by a HDMI transmitter connected to Port A or to Port B.

How is the internal EDID configured?

The internal EDID is populated and configured via the general I^2C interface of the ADV7441A/AD9388A. Refer to the device hardware manuals for more details on how to configure the internal E-EDID.

When the dual port is used, is it possible to differentiate between the video formats supported by each port?

Yes. This can be accomplished by having a different EDID data image for each port of the HDMI receiver. There are three ways to do this.

- Use two external EDIDs for Port A and Port B.
- Use one external EDID on one HDMI port and the internal EDID on the other port.
- Use the internal EDID on both ports, and reprogram the internal EDID before switching from one port to another. This is acceptable as long as the HPD signal is always unasserted on the inactive port, thus indicating to the receiver that the EDID of the inactive port is not accessible.

Does the internal EDID support Current Address Read?

No. Current Address Read refers to an I^2C read request in which the address location to access is not specified. It is assumed to be known or in a previous I^2C read request.

REFERENCES

High Definition Multimedia Interface Specification Version 1.3, June 22, 2006.

High Bandwidth Digital Content Protection System Specification Rev 1.3, Digital Content Protection LLC, 2006.

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