Design and Implementation of a Broadband RF-DAC Transmitter for Wireless Communications

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To the memory of my father, Gebhard Zimmermann

Acknowledgment

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3GPP	3rd Generation Partnership Project
ACPR	adjacent channel power ratio
ADPLL	all-digital PLL
AM	amplitude modulation
ASK	amplitude shift keying
balun	balanced-to-unbalanced converter
BER	bit error rate
BOM	bill of materials
CCDF	complementary cumulative distribution function
CDC	clock domain converter
CDMA	code division multiple access
CIC	cascaded integrator-comb
CML	common mode logic
CMOS	complementary metal-oxide-semicondutor
cw	continuous wave
DAC	digital-to-analog converter
DECT	Digital Enhanced Cordless Telecommunications
DFT	discrete Fourier transformation
DFTS-OFDM	DFT-spread OFDM
DNL	differential nonlinearity
DPA	digitally controlled PA
DRFC	digital-RF converter
DWA	data weighted averaging
EDGE	Enhanced Data Rates for GSM Evolution
EDR	Enhanced Data Rate (Bluetooth extension)
EIRP	effective isotropically radiated power
ENOB	Effective Number of Bits
ESD	electrostatic discharge
ESL	element selection logic
EVM	error vector magnitude
FDD	frequency division duplex
FFT	fast Fourier transformation
FMC	FPGA Mezzanine Card
FPGA	field programmable gate array
FSK	frequency shift keying

GaAs	gallium arsenide
GMSK	Gaussian minimum shift keying
GPS	Global Positioning System
GSM	Global System for Mobile Communications
HPC	High Pin Count connector
HSPA	High Speed Packet Access
IC	integrated circuit
ICI	inter-carrier interference
IDFT	inverse discrete Fourier transformation
IEEE	Institute of Electrical and Electronics Engineers
IF	intermediate frequency
IMD	intermodulation distortion
INL	integral nonlinearity
ISI	inter symbol interference
ISM	industrial, scientific, medical
LAN	local area network
LCM	least common multiple
LINC	LInear amplification with Nonlinear Components
LNA	low noise amplifier
LO	local oscillator
LSB	least significant bit
LTE	3GPP Long Term Evolution
LUT	look up table
LVDS	low voltage differential signaling
MIM	metal-insulator-metal
MIMO	multiple input multiple output
MSB	most significant bit
NiMH	nickel-metal hydride
NTF	noise transfer function
OFDM	Orthogonal Frequency Division Multiplex
PA	power amplifier
PAE	power added efficiency
PAPR	peak to average power ratio
PC	personal computer
PCB	printed circuit board
PLL	phase locked loop
PM	phase modulation
PSK	phase shift keying
QAM	quadrature amplitude modulation
RF	radio frequency
RFIC	RF integrated circuit
RTZ	return to zero

Rx	receive
SAW	surface acoustic wave
SC-FDMA	single carrier frequency division multiple access
SDR	software defined radio
SiGe	silicon germanium
SMA	SubMiniature version A connector
SMD	surface mounted device
SNR	signal to noise ratio
SPICE	Simulation Program with Integrated Circuit Emphasis
STF	signal transfer function
TDD	time division duplex
TSPC	true single phase clock
Tx	transmit
UMTS	Universal Mobile Telecommunications System
USB	universal serial bus
VCO	voltage controlled oscillator
VGA	variable gain amplifier
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VSWR	Voltage standing wave ratio
WCDMA	Wideband CDMA
WiMAX	Worldwide Interoperability for Microwave Access
WLAN	wireless LAN
XO	crystal oscillator

1 Introduction

Within the last 20 years, digital wireless communications has got an indispensable part of our daily lives. In 2010, the number of mobile cellular subscriptions worldwide reached five billion [Eri10]. Each year, more than one billion cellular phones are being sold. Ericsson, one of the leading telecommunications and network equipment suppliers, estimates that there will be more than 50 billion connected devices by 2020 [Eri10]. In history, there has never been a technology which has got a comparably high market penetration in such a short time.

One of the main drivers of this astonishing development is the rapid decline of production costs. Since the invention of the integrated circuit by Jack Kilby and Robert Noyce in 1958, semiconductor industry has seen a doubling of the number of transistors per chip area every 18 month. This exponential growth was already predicted by Gordon Moore in 1965 [Moo65]. His prediction is still valid today and widely known as "Moore's law".

Moore's law does not only lead to low production costs but also results in enormous signal and data processing capabilities of modern mobile phones. So-called smartphones have more computational power than most desktop computers in recent years. To allow an optimum user experience, smartphones have to support high-data-rate wireless connections. Furthermore, to be able to use a broad range of different services, these devices need to support a lot of different communication standards, such as UMTS, wireless LAN, Bluetooth, GPS etc. Also, older standards like GSM still have to be supported. Even several years after the rollout of a new broadband communication standard such as UMTS, good network coverage can only be expected in densely populated metropolitan areas, making GSM an indispensable fallback solution. Starting from 2010, the first 3GPP LTE (Long Term Evolution) networks are installed. LTE is the successor of the UMTS standard, enabling even higher data rates, up to 300 Mbps.

The large number of supported communication standards – some allowing the operation in several different frequency bands – requires an equally large number of specialized, high-performance RF frontends. Especially, new OFDM (Orthogonal Frequency Division Multiplex) based standards like LTE require high bandwidth, high linearity and high dynamic range. Moreover, LTE permits configurability for different signal bandwidths and modulation schemes. Modern transceiver chips have a lot of parallel receive and transmit paths to support multistandard and multiband operation. As an example, Infineon's SMARTi™ LU 65 nm CMOS transceiver chip supports up to six 3G and LTE bands simultane-
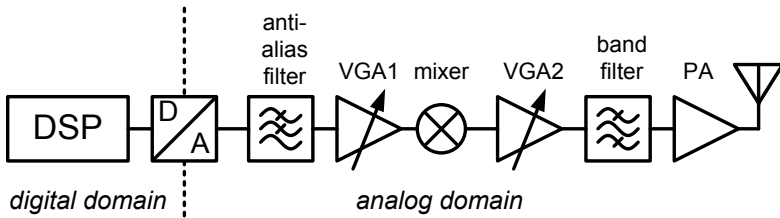
Figure 1.1: Classical analog transmitter.

ously with quad band GSM/EDGE as well as MIMO Rx diversity [Inf10].

Unfortunately, analog and RF parts do not see the same shrinking in area as digital circuits when moving from one CMOS technology node to the following. The required area of digital circuits exhibits a quadratic shrink with a linear decrease in CMOS feature size. The area of the analog blocks however shrinks linearly, at most [Kru08]. A reason for this is that due to the short-channel effect, the lengths of the transistors in the analog circuits cannot be scaled indefinitely when a specific circuit performance has to be achieved. In addition, capacitors, inductors and wiring, which hardly shrink from one technology node to the next, make up a large portion of the footprint of the analog blocks. Therefore, analog blocks require a large portion of the complete area of a mixed-signal chip in nanoscale CMOS. Worse yet, the implementation of several parallel radios on one chip requires even more area and leads to high production costs.

Fig. 1.1 shows the simplified block diagram of the required analog and RF components of one transmit path. In addition to complex analog integrated circuits, each receive and transmit path potentially needs dedicated discrete off-chip components such as SAW filters, power amplifier and antenna switch. These external components are costly and make up a large portion of the total bill of materials (BOM) of a mobile phone. Moreover, these devices are comparatively bulky, limiting the miniaturization of the structural shape of a mobile phone.

To obviate several parallel radios on the same portable device, reconfigurable multistandard, multiband radios are needed. The ultimate goal of the multi-standard radio development is the "software defined radio" (SDR). The term "software defined radio" was coined by Mitola in the 1990th [Mit95].

The most simple and most ideal SDR transmitter would consist only of digital signal processing and a high-speed, high-resolution, high output power digital-to-analog converter (DAC) that directly drives the antenna, as depicted in Fig. 1.2(a). The ideal receiver would have a similar architecture; an analog-to-digital converter would pick up the received signal directly after the antenna, all subsequent signal processing would be done in the digital domain. This

(a) Ideal SDR transmitter   (b) RF-DAC transmitter
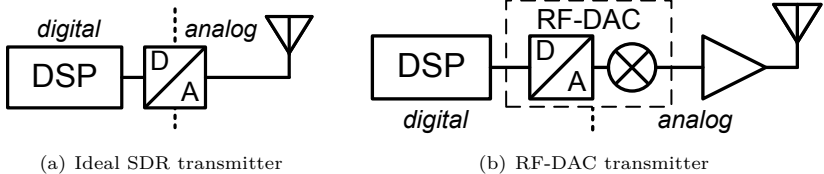
Figure 1.2: "Digital RF" reconfigurable transmitters.

kind of system would be ultimately flexible and reconfigurable for different communication standards. However, the ADC and DAC would have to operate at a multiple of the RF carrier frequency to fulfill the Nyquist criterion. Also, a huge dynamic range and, as a result, a very high resolution of the converter is needed. With today's technology, converters with a performance that is good enough to achieve such a system are not (yet) feasible. Moreover, the extremely high power which such a converter would consume makes it questionable if such an ideal SDR system is reasonable for mobile devices at all [Ken05].

Recently, some reconfigurable transmitters have been demonstrated, that are based on a so-called RF-DAC architecture [Elo+07; JS06; Tal+08]. This kind of transmitter seems to be an excellent alternative to classical transmitter architectures. RF-DAC based transmitters enable broadband OFDM transmission and are reconfigurable for different mobile communication standards. The RF-DAC combines D/A-converter and mixer in a single building block. As this architecture still features a mixer, the digital blocks do not have to operate at a multiple of the carrier frequency. A simplified block diagram of an RF-DAC transmitter is depicted in Fig. 1.2(b). Analog baseband circuitry can be replaced with digital, programmable blocks. Therefore, RF-DAC based transmitters are a step towards Software Defined Radio (SDR).

In addition to being very flexible, the RF-DAC architecture is also very well suited for sub-65 nm CMOS nodes. Nanoscale CMOS nodes permit very fast and power-efficient digital circuits. The low supply voltages which are required by nanoscale CMOS as well as short channel effects of the transistors, however, are large challenges for the implementation of high-performance analog circuits. The transistors in the RF-DAC, on the other hand, operate as switches and do not have high requirements on linearity. High-performance analog baseband building blocks that are needed for classical analog transmitter architectures as e.g. variable gain amplifiers (VGAs) can be replaced by digital signal processing. In addition to achieving compatibility to nanoscale CMOS nodes, replacing analog by digital building blocks makes the portability of the transmitter design from one CMOS process node to the next much easier.

1.1 Goal of the work

The objective goal of this work is the implementation of a reconfigurable RF-DAC based transmitter. The transmitter should be capable of handling broadband high-data-rate OFDM signals such as LTE or WLAN. In addition, the output power of the transmitter should be as high as possible in order to achieve a high integration level and require only a low number of expensive external components, especially high gain power amplifier (PA) modules.

A suitable system architecture has to be found and performance requirements for the different building blocks have to be specified. Based on these findings, a circuit implementation of the mixed-signal transmitter frontend – and in particular of the RF-DAC – has to be conducted. Finally, the fabricated prototype has to be measured.

1.2 Structure of this thesis

The outline of this thesis is as follows:

In chapter 2 the fundamentals of transmitters for wireless communications are presented. The most important transmitter architectures are discussed and the relevant performance requirements as well as the most important performance metrics are introduced. Furthermore, a brief introduction to modern broadband OFDM-based wireless communication standards is given. It is found that OFDM has quite high performance requirements on the RF frontend. Especially the high required peak to average power ratio is an issue.

To decrease production costs and PCB area requirements of the transmitter, it should be as highly integrated in a monolithic CMOS chip as possible. High performance and output power requirements make the integration of the PA an especially difficult task. In chapter 3 the implementation of two different PA prototypes in 130 nm CMOS is discussed. The measurement results show a peak saturated output power of more than 27 dBm at 1.9 GHz. While this is sufficient for connectivity devices like DECT, it is concluded from the measurements as well as published results from other groups that it is not feasible to integrate the PA into a single-chip radio for cellular applications. Thus, subsequently only transmitter architectures with an additional external PA are considered.

In chapter 4, the fundamentals of reconfigurable "direct-digital" RF-DAC transmitters are presented. Different RF-DAC transmitter implementations and akin "digital-RF" architectures that can be found in literature are presented and compared. General benefits and drawbacks of RF-DAC architectures, especially the quite high unwanted emission of spurious signals, are discussed. Finally, techniques to reduce the unwanted emission are introduced.

Subsequently, in chapter 5, the system concept of a transmitter that is based on an RF-DAC based I/Q modulator is presented. Architectural choices are

discussed and substantiated by Matlab system simulations. System performance requirements are derived from the supported wideband OFDM-based communication standards and the spectral emission masks that have to be fulfilled. Furthermore, performance specifications for the main digital, mixed-signal and RF building can be obtained from system simulations.

Chapter 6 presents the circuit implementation of the mixed-signal and RF frontend. Therefore, a 65 nm standard CMOS technology has been chosen as it enables the required performance of the digital blocks. The implementation of the RF-DAC as well as all other major building blocks is presented including simulation results. Additionally, layout considerations are discussed. Finally, simulation results of the complete RF-frontend are presented.

The measurement setup for the prototype IC as well as the major measurement results is presented in chapter 7. The measurement results prove the feasibility and potential of the RF-DAC transmitter concept. The RF-DAC transmitter is capable of processing up to 40 MHz wide 64QAM OFDM signals and fulfills the IEEE 802.11n spectral mask. The peak measured output power is 16 dBm.

Finally, chapter 8 concludes this thesis with a brief summary of the work that has been done and gives an output to possible future improvements.

2 Fundamentals of Transmitters for Wireless Communications

Together with the receiver, the transmitter forms the basis of every radio. The RF transmitter performs modulation, upconversion of a low frequency (LF) baseband signal to the carrier frequency and power amplification of the RF output signal, before it is emitted by the antenna.

2.1 Basic transmitter architecture

Almost all recent communication standards are based on digital signal modulation. The most commonly used RF transmitter architecture for this kind of system is the direct conversion quadrature modulation transmitter, shown in Fig. 2.1. For a direct conversion transmitter, the local oscillator (LO) frequency is equal to the transmitted carrier frequency; thereby the frequency translation from LF to RF is done in one single step.

The transmitter features a digital baseband processor which handles source coding, channel coding, digital modulation and matched filtering of the data to be transmitted [McC10; Kam08]. The generated digital baseband signal is eventually translated to the analog domain, utilizing a digital-to-analog converter (DAC). The DAC obviously has to fulfill the Nyquist criterion, such that an analog reconstruction filter can remove the DAC alias spectra. A quadrature upconversion mixer translates the I/Q baseband signals to the RF carrier frequency.
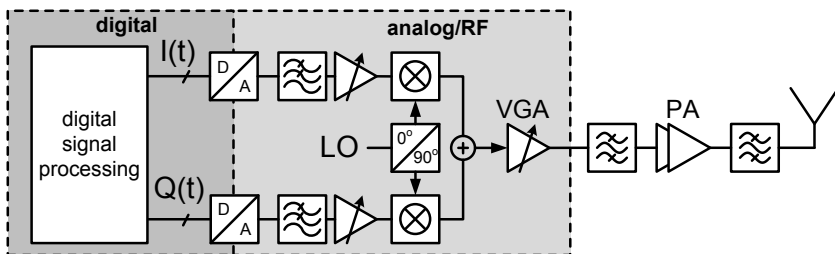
Figure 2.1: Block diagram of a conventional analog quadrature RF transmitter.

Variable gain amplifiers (VGAs) control the output power. These VGAs either can be implemented at baseband – before the mixer stage – or at RF, following the mixer. It is much easier to implement VGAs with high dynamic range at baseband frequencies. Placing two separate amplifiers in the quadrature signal paths, however, may create an I/Q amplitude imbalance. Therefore, sometimes it is preferable to do the power control at RF. Besides, some kind of driver is mostly needed anyway in order deliver the optimal signal amplitude to a subsequent power amplifier (PA).

The PA has the task to generate the required output power and deliver it to the antenna. Typically, the PA is not integrated into the CMOS transceiver, but fabricated as an own chip in a high-performance GaAs or SiGe technology. The PA is connected to the antenna, which has a $50\,\Omega$ input impedance, via an impedance transformation network. Thereby, an optimum load impedance – which is generally lower than $50\,\Omega$ – is presented to the PA, in order to maximize its output power and energy efficiency [Cri06].

Filters are needed to suppress unwanted out-of-band emissions. As the filtering requirements for mobile communications are usually quite strict, high-performance "surface acoustic wave" (SAW) filters have to be used. Often, filtering is not only done at the PA output but also preceding the PA, in order to improve its intermodulation performance.

2.2 Key RF transmitter performance measures and requirements

Subsequently, the most important characteristics of RF transmitters and their measures are briefly introduced.

2.2.1 Maximum output power

Obviously, the maximum output power P_{out} is one of the most important performance measures. Cellular standards define a maximum average output power which has to be achieved by the transmitter, as to guarantee proper operation even for inferior channel characteristics, e.g. when the handheld device is far away from the base station. Wireless connectivity standards such as WLAN and Bluetooth only define a maximally permitted output power, such that a transmitting device does not disturb other devices which are located in some distance but operate at the same frequency. The actually achieved maximum output power of these connectivity devices may be below this limit. Normally, the Tx output power is defined at the input of the antenna or the antenna connector. For some communication standards, the "effective isotropically radiated power" (EIRP) is defined, which takes the antenna gain G_{ant} into account. The EIRP is

the amount of power that a theoretical isotropic radiation antenna would emit to produce the peak power density measured in the direction of maximum antenna gain. Thus, the EIRP can be calculated as

$$\text{EIRP} = P_{out} \cdot G_{ant} \tag{2.1}$$

The actual output power of the PA has to be higher than the maximum output power defined by the standard, as it will be damped by some dB by the subsequent SAW filters and antenna switches.

For amplitude modulated signals a distinction must be made between maximum average output power and peak output power. The maximum average output power is the average over some period of time, e.g. one transmit burst. The peak output power, on the other hand, is the instantaneous maximum output power which is only reached for a very short time duration. The fraction between these two measures is called "Peak to Average Power Ratio" (PAPR) or "Crest factor".

2.2.2 Dynamic range

For some cellular standards, not only the maximum average output power, but also the minimum output power of a transmitter is defined. The dynamic range of the transmitter is given by:

$$\text{dynamic range} = P_{out,max} - P_{out,min}. \tag{2.2}$$

Sometimes, also a power control step size (in dB) is given. For example, the 3GPP WCDMA standard [3GP10] defines an dynamic range[1] of 74 dB (+24 dBm to -50 dBm) and a power control step size of 1 dB for the mobile devices. For communication standards which are based on a code division multiple access scheme (CDMA) this accurate power control is very important to enable the base station receiver to properly disaggregate the signal components which have been sent by different transmitters running at the same carrier frequency.

A sufficient dynamic range is normally achieved by cascading building blocks with several gain steps, such as VGAs and mixer. Also, power control can be implemented with the DAC, if its amplitude resolution is sufficiently high.

2.2.3 Operational bandwidth

The required operational bandwidth is defined by the needed data rate and the chosen modulation scheme. Different digital modulation techniques such as amplitude shift keying (ASK), frequency shift keying (FSK), phase shift keying (PSK), and orthogonal frequency division multiplex (OFDM) have different

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[1] note that this definition of the dynamic range is based on average power levels and does not yet include the PAPR, which is approximately 5 dB for WCDMA.

(a) P_{out} vs. P_{in}

(b) PAE vs. P_{in}
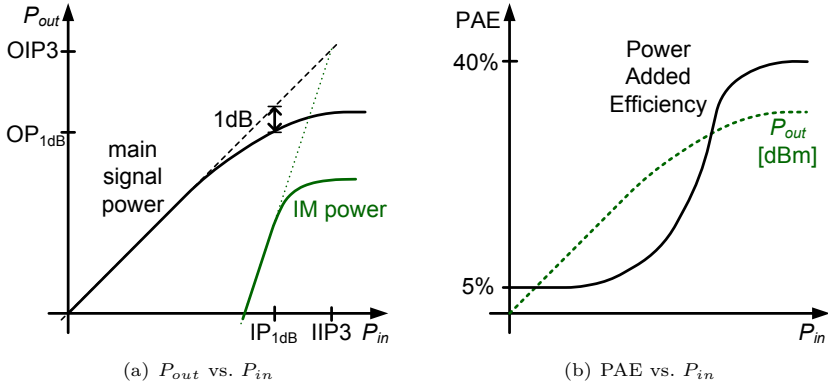
Figure 2.2: Amplifier nonlinearities (a) and power efficiency (b) versus input power.

spectral efficiencies. The spectral efficiency is defined as the number of bits which can be transmitted per time and bandwidth – typically measured at 20 or 60 dBc signal roll-off. Obviously, a modulation scheme with high spectral efficiency is desirable. Nevertheless, trade-offs between spectral efficiency and the required transmitter complexity and power consumption exist.

The bandwidth of each building block must be high enough so that it does not impair the signal quality. On the other hand, the filter bandwidths may not be chosen too high, in order to suppress emissions at frequencies other than the wanted signal.

Modern OFDM-based communication standards support variable signal bandwidths (see section 2.4). As a result, at least the baseband filters should be programmable in bandwidth, in order to achieve optimum performance.

2.2.4 Linearity

For signals that have a non-constant envelope, a highly linear transmitter is essential to achieve a high signal quality and keep intermodulation distortion (IMD) low. For a linear amplifier the output signal is directly proportional to the input signal. Real amplifiers, however, show clipping effects near their maximum capacity, leading to gain compression. An important measure for this phenomenon is the 1 dB compression point, where the power gain of the amplifier is 1 dB below the small signal gain (see Fig. 2.2(a)). For amplitude modulated signals, the peak output power must be well below this point to keep

the signal quality high.

If a sine-wave signal is applied to a nonlinear system, harmonics at multiple frequencies of the fundamental are generated. As the system normally has a low gain at these frequencies, harmonics are typically not measured directly as the multi-tone output of a single-tone input. Rather, a *two-tone test* is done.

If several signals at different frequencies have to be amplified at the same time, the nonlinearities introduced by gain compression lead to *intermodulation* between these signals. The third order intermodulation product of two sinusoidal tones at close frequencies ω_1 and ω_2 is of special interest, as it is notably high. Moreover, it can appear in-band, as the resulting tones are located close to the original signals at $\omega_{IP3_a} = 2 \cdot \omega_1 - \omega_2$ and $\omega_{IP3_b} = 2 \cdot \omega_2 - \omega_1$. To specify the IMD, a performance metric called "third order intermodulation point" (IP3) is given [Raz97, p. 17 ff.]. The IP3 test takes advantage of the fact that the amplitude of the third order harmonic rises cubically, when the amplitudes of the fundamental tones are increased linearly. Typically, the two input signals at ω_1 and ω_2 have equal amplitudes $A_1 = A_2 = A$. When drawn in the logarithmic P_{out} vs. P_{in} plot (see Fig. 2.2(a)) straight lines result (at least in the weakly nonlinear region of the system) with a slope of one for the power of the fundamental components and a slope of three for the IM3 product. The lines cross at the point, which is defined as IP3. This point can either be specified as an input referred power (IIP3) or as an output referred power (OIP3), as shown in Fig. 2.2(a).

2.2.5 Power efficiency

Power efficiency (sometimes also termed "energy efficiency"), is important for a mobile communication device as it determines battery run-time. The transmitter and especially the PA are typically the most power-hungry parts of a transceiver. Therefore, special emphasis has to be laid on maximizing the power efficiency of these building blocks.

Different measures exist for the power efficiency

- The overall transmitter efficiency is defined as RF power P_{out} radiated from the antenna divided by the total DC power P_{supply} drawn from the battery

$$\eta_{OTxE} = \frac{P_{out}}{P_{supply}} \cdot 100\% \tag{2.3}$$

- The (drain) output efficiency is the PA output power divided by the DC power into the final PA stage

$$\eta_{OE} = \frac{P_{out}}{P_{supply,PA}} \cdot 100\% \tag{2.4}$$

- Often, the so-called "power added efficiency" (PAE) is given, when specifying the PA performance. It is the difference between the output power P_{out} and input power P_{in} of the PA, divided by the consumed DC power

$$\text{PAE} = \frac{P_{out} - P_{in}}{P_{supply,PA}} \cdot 100\% \qquad (2.5)$$

For large power amplifications, PAE and η_{OE} are virtually the same.

Power efficiency is highly dependent on the operation point of the PA. A typical PAE versus P_{in} curve for a linear PA, like a class A, AB or B amplifier, is shown in Fig. 2.2(b). As can be seen, a high efficiency can only be achieved, when the PA is operated in compression, close to its maximum saturated output power. For amplitude modulated signals, however, a PA operation in compression is not practicable because of the required linearity, as discussed above. For this reason, constant envelope modulated signals typically permit a higher power efficiency than amplitude modulated signals. Moreover, the system costs for the former may be much lower, as the PA output power capacity can be much reduced.

2.2.6 Unwanted emissions

Unwanted emissions are a major issue of every RF transmitter. To minimize interference with other wireless communications systems, emissions at other frequencies than the wanted signal shall not be too high. Therefore, most communication standards place stringent requirements on both out-of-band and out-of-channel emissions.

The cause of unwanted emissions can be separated into two categories: close-to-carrier and far-off noise. Close-to-carrier noise is dominated by IMD, as illustrated in Fig. 2.3 [Ken05]. Main contributor to IMD is the PA. Typically, cellular standards define the maximum IMD power in the neighboring channels. These measurements are done with real, modulated signals instead of the above given IMD definitions with sinusoidal signals. Therefore, the maximum unwanted signal power in a channel bandwidth, one channel away from the wanted signal, is defined. This power is divided by the power in the wanted channel and given as "adjacent channel power ratio" (ACPR). Noise in the adjacent channel is dominated by the third order IMD product [Anr01]. Also, sometimes the power in a bandwidth two channels away is defined as "alternate channel power ratio". In terms of the IMD measurements, a fifths order product may correspond to the alternate channel power ratio.

In addition to IMD, LO phase noise spreads out the wanted signal in frequency, which can lead to a violation of the spectral mask. This is especially an issue for narrowband systems like GSM, leading to a high phase noise to signal bandwidth ratio. To reduce phase noise, a high-performance VCO as well as an adequate PLL architecture is needed.
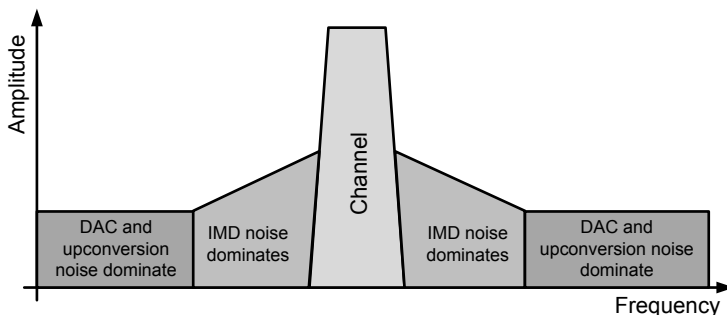
Figure 2.3: Intermodulation distortion noise dominates close to the wanted signal, DAC and upconverter noise dominates far-off the carrier frequency.

Far away from the carrier, IMD and LO phase noise drop off. At these far-off frequencies, DAC quantization noise as well as upconversion mixer noise dominate the unwanted emissions. These types of noise result in a relatively constant noise floor, as shown in Fig. 2.3. DAC noise is defined by the effective resolution of the converter and the quality of the anti-alias filters. The main noise sources of active mixers are switching noise and noise of the transconduction stage [DA00].

2.2.7 Error vector magnitude

The "error vector magnitude" (EVM) is an important measure for the quality of a telecommunication signal. The EVM is plotted in the signal constellation diagram. The error vector is the difference vector between the ideal (reference) symbol phasor and the actual symbol phasor measured at symbol times, as shown in Fig. 2.4.

The error vector magnitude corresponds to the length of the error vector. Sometimes, the average EVM, evaluated for a statistically sufficient number of symbols, is given. The EVM must be normalized with respect to the average power or amplitude of a signal, to get comparable measures for different signals. Normally, the EVM is then stated as a percentage.

Depending on the communication standard, different EVM measures are defined

- The "peak EVM" is the largest EVM value which is measured in a defined length of time, e.g. one transmit burst.

- The EVM_{RMS} is the RMS value of several error vectors, averaged over
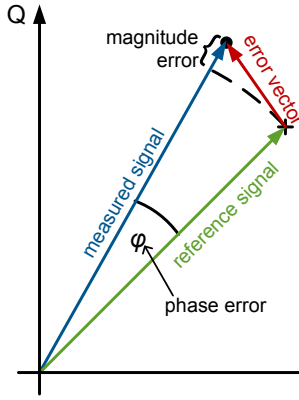
Figure 2.4: Measuring the EVM in a constellation diagram.

some given time interval T. This is the most common measure.

- The EVM$_{99\%}$ defines that 99% of all symbols in a time interval T are better than EVM$_{99\%}$.

The EVM$_{RMS}$ is thus defined as

$$\text{EVM}_{RMS} = \sqrt{\frac{\sum\limits_{r=1}^{T} \left(|I_r - I_{0,r}|^2 + |Q_r - Q_{0,r}|^2 \right)}{\sum\limits_{r=1}^{T} \left(|I_{0,r}|^2 + |Q_{0,r}|^2 \right)}} \tag{2.6}$$

where I_r, Q_r are the measured signal components and $I_{0,r}$, $Q_{0,r}$ are the ideal reference symbols.

Transmitter signal quality and thus EVM performance is determined by several factors:

- the effective resolution of the DAC

- LO leakage

- I/Q mismatch (and thus image suppression)

- LO phase noise

- transmitter linearity

In addition to evaluating the raw EVM value, looking at the constellation diagram can give useful hints, what the limiting factors for the signal quality are. LO phase noise, for example, only generates a phase error, but no magnitude error. Therefore, the measured symbols are lying on a circle that goes through the reference symbols. I/Q mismatch on the other hand can be observed as a deformation of the constellation in the I/Q plane. It is not a square any more, but rather a rectangle with unevenly long sides.

For simulations and measurements on system level, including baseband signal processing, the signal quality is also often specified as *bit error rate* (BER). Anyhow, BER simulations and measurements do only allow to evaluate the performance of the complete transmitter chain including digital baseband processing. It is not possible to evaluate the influence of only the RF frontend on the BER. A BER analysis requires simulations over a very long system time, which is almost not possible for the RF frontend because of the small required simulation time steps.

2.3 Important Transmitter topologies

Subsequently, some of the most important and popular transmitter architectures shall be introduced.

2.3.1 Heterodyne transmitter

Instead of doing the signal translation from baseband to RF in one step, like in the direct conversion transmitter architecture shown in Fig. 2.1, it can also be done in several steps. Such a two-step transmitter, where the I/Q modulator first translates the baseband signal to an intermediate frequency (IF) ω_1, is shown in Fig. 2.5. In a second step, the signal is mixed with a second LO signal at ω_2, translating the signal to the RF frequency $\omega_1 + \omega_2$. A bandpass filter is needed behind the second mixer to remove the unwanted sideband.
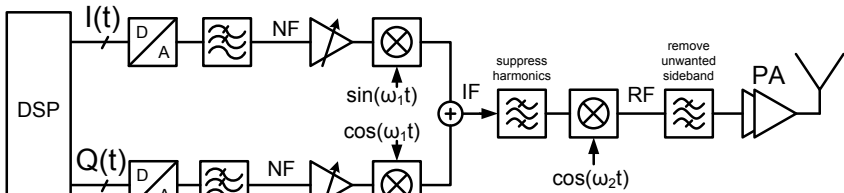
Figure 2.5: Block diagram of a two-step heterodyne transmitter.

The two-step transmitter of Fig. 2.5 is the transmitter equivalent to the heterodyne receiver architecture.

The heterodyne transmitter architecture has some advantages over the homodyne architecture. First, homodyne transmitters can suffer from so-called "VCO pulling" or "injection locking" [Raz97, p. 153 ff.]. This effect can occur, when the strong PA signal output leaks back into the VCO, if the latter one is not shielded well enough. The VCO then can be disturbed by the "noisy" modulated PA output. This problem can be reduced if the I/Q signal is generated by a factor-of-two frequency division, as the VCO then is a multiple of the PA output frequency. For heterodyne transmitters VCO pulling is no problem, as the PA output frequency may be chosen independently from the IF frequency. As the second LO frequency is different from the RF frequency, also LO feedthrough is no problem.

Second, two-step transmitters usually have a better I and Q matching, as the modulator is running at a lower frequency. A channel filter at IF may be used to reduce the transmitted noise and spurs at adjacent channels.

Nevertheless, this architecture can hardly be found in modern integrated transmitter solutions, as the large number of needed components leads to high costs. One main obstacle are the IF filters which have to be implemented as external SAW filters to get a high quality factor. Thus, they are bulky and especially expensive.

2.3.2 Polar modulator

Polar modulation originates in a technique called "Envelope Elimination and Restoration" which was first introduced by Kahn in 1952 [Kah52]. Polar modulator transmitters are based on the decomposition of the RF signal into a magnitude and phase component. The phase component then is an RF signal but has a constant envelope. The magnitude component is essentially the envelope of the modulated signal and is at LF. The RF signal reconstruction is done with an RF power amplifier stage close to the antenna. The input signal of this amplifier is the phase modulated signal, while the amplitude modulation is done by changing the supply voltage. As the RF signal component contains only phase information, a PA which linearly amplifies the input signal is not required. A nonlinear power amplifier with high power efficiency can be used. Typically, a class E PA is utilized, whose output voltage is linearly proportional to its supply voltage [RS06]. All linearity requirements are shifted to the low frequency parts, namely the supply voltage regulators, where they are much easier to achieve. The whole RF path may be nonlinear. Therefore, the power efficiency of the polar modulator architecture is relatively high, while still allowing amplitude modulation.

A possible implementation of a polar modulator is shown in Fig. 2.6. The polar
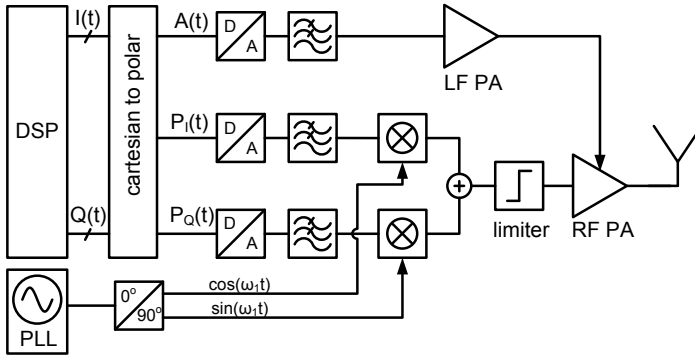
Figure 2.6: Block diagram of a polar transmitter.

signal components $P(t)$ and $A(t)$ can quite easily be generated by digital signal processing, using the CORDIC algorithm or a look-up table. The amplitude component $A(t)$ is amplified by a linear low frequency power amplifier (LF PA) or supply voltage modulator. The phase component $P(t)$ has to be modulated on the RF carrier. In Fig. 2.6 this is done with an I/Q vector modulator. The phase modulation could also be directly done with a PLL, given that the PLL bandwidth is high enough. A technique which enables relatively high PLL bandwidths is two-point modulation [The02].

Polar modulation transmitters are perfectly suited for a complete CMOS integration (including the PA, depending on the required output power) and are especially popular for relatively narrowband communication standards such as GSM/Edge [Sow+04] and Bluetooth [RS05].

Small signal polar modulation

A variant of the polar modulator described above is the so-called "small signal polar modulator". The block diagram of such a small signal polar modulator looks almost similar to Fig. 2.6; however, the amplitude modulation is not performed by the RF-PA but by a "small signal" amplifier preceding the PA. Thus, a linear PA is still required, as is the case for the I/Q quadrature modulators in Fig. 2.1 and Fig. 2.5. Thereby, the most important benefit of the polar modulator architecture, the high power efficiency, is lost.

Anyhow, the small signal polar modulator is popular for the implementation of narrowband RF transceiver chips in CMOS, where an external high output power PA is needed [Ell+04]. These PAs usually do not allow an amplitude modulation which achieves a sufficient performance and can be controlled by the

(a) LINC block diagram

(b) signal combination principle
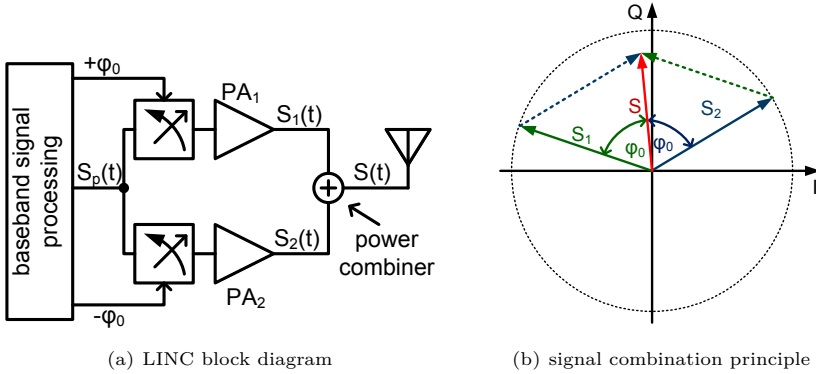
Figure 2.7: Simplified block diagram of a LINC transmitter and outphasing principle.

CMOS transceiver chip.

Although lacking a substantial power efficiency benefit compared to I/Q modulators, the small signal polar still can have some relevant advantages:

- The narrowband PLL transfer function leads to a good filtering of the upconverted noise. Thus, the filtering requirements between transceiver chip and PA may be relaxed. It is even possible to obviate the need for a SAW filter at the transceiver output if the unwanted emissions of the polar modulator are low enough.

- The required die area for the modulator may be smaller than for an I/Q modulator, as only one amplitude path is required; however, a more complex PLL is needed.

- I/Q mismatch is no issue.

2.3.3 LINC

Another transmitter topology, which can be used to build highly efficient, linear transmitters is LINC [Cox74]. LINC stands for "LInear amplification with Nonlinear Components" and is based on the outphasing technique that has been developed by Chireix [Chi35] in 1935.

The simplified block diagram of a LINC transmitter is shown in Fig. 2.7(a). It utilizes two nonlinear power amplifiers, operated with a constant envelope, and two phase shifters [Erk10] that set the outphasing angle. The outputs

are combined with a power combiner. Both amplifiers always have output signals $S_1(t)$ and $S_2(t)$ at the maximum amplitude of the PAs. As a result, the PAs are operated at their maximum power efficiency. Nevertheless, a linear amplitude modulated signal $S(t)$ can be generated by modulating the phase difference between the two output signals, therefore the name LINC. The principle operation of this outphasing technique is depicted in Fig. 2.7(b). Obviously, output powers up to twice the capacity of a single PA can be realized.

For modern CMOS technologies the phase shifters may also be implemented in the digital domain. In this case, the phase shifter resolution, however, must be high enough so that the amplitude resolution requirements can be fulfilled.

The main issue of the LINC concept is the implementation of the power combiner. The most common approach is to use a Wilkinson combiner. While providing excellent linearity and isolation between the PAs, for small needed output powers, the Wilkinson combiner sinks all excessive generated PA power. As a result, for high PAPRs this topology in fact does have a lower power efficiency than a simple class AB amplifier [NG08]

As an alternative to the Wilkinson combiner, a lossless power combiner could also be used. In this case, however, the PA outputs are not isolated, leading to some kind of active load-pulling and, as a consequence, to a nonlinear output.

Summarizing, it can be said that LINC does not have a significant power efficiency advance over linear class AB PAs, although highly efficient nonlinear PAs can be used. Nevertheless, linear PAs need to have a higher output power capacity to achieve the same linear output power as a LINC system.

The advances in CMOS technology that permit building high performance signal processing and PAs on the same chip, recently have led to an increased research in the field of LINC [Hei+09].

2.4 The OFDM technology and its use in wireless communications

Just as for wireline communications, also for mobile communications there is a trend towards ever increasing data rates. As bandwidth is quite limited for wireless communications, modulation techniques with a great bandwidth efficiency (measured as bits per second and Hertz) are therefore needed. A modulation scheme which fulfills this need and has gotten increasingly popular in recent years is Orthogonal Frequency Division Multiplex (OFDM). It is used for almost all modern broadband mobile communication standards, like WLAN (IEEE 802.11a/g/n), WiMax mobile (IEEE 802.16e), 3GPP LTE and Bluetooth 3.0. Thus, the basic principles and characteristics of OFDM and its consequences on the RF frontend shall be briefly discussed subsequently.

2.4.1 OFDM fundamentals

For common digital modulation schemes, like frequency shift keying (FSK), phase shift keying (PSK) and amplitude shift keying (ASK), the signal information is modulated on one single carrier. To achieve a high data rate, a high modulation order and high symbol rate are needed.

For OFDM, however, to achieve high data rates with a reduced symbol rate, the information is distributed among several parallel carriers, spaced evenly in frequency. Thereby, the sum of $N + 1$ narrowband modulated signals form one broadband, multicarrier signal $s_{MC}(t)$, which is located around a radio carrier signal:

$$s_{MC}(t) = \sum_{n=-N/2}^{N/2} d_n(i) \cdot e^{j2\pi f_n t} \qquad \text{for} \qquad iT_s \le t \le (i+1)T_s \qquad (2.7)$$

The principle of this multicarrier signal generation in the frequency domain is depicted in Fig. 2.8.

Obviously, interference between the signals of the neighboring subcarriers should be minimized. To achieve this, the subcarriers must be mutually orthogonal. This is assured by subcarriers which have exactly an integer number k of cycles within the symbol time. Thereby, the subcarrier spacing Δf is related to the symbol time T_s as

$$\Delta f = \frac{k}{T_s}. \qquad (2.8)$$

Each modulated subcarrier signal has nulls at the frequency of the neighboring subcarriers, as illustrated in Fig. 2.9(b), thus the subcarriers are intercarrier interference (ICI) free.

The total bandwidth of the OFDM system equals the number of subcarriers times the subcarrier spacing. The selected subcarrier spacing is constrained
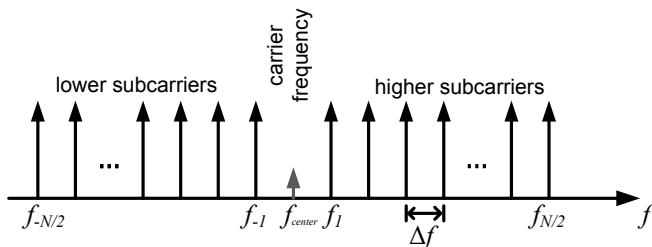
Figure 2.8: Basic principle of multiple subcarrier signal generation.

(a) single-carrier signal   (b) ODFM multicarrier signal
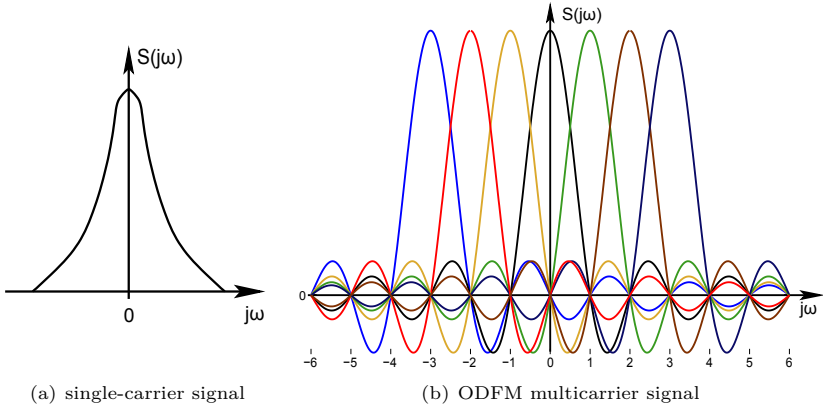
Figure 2.9: Single carrier signal vs. OFDM signal.

by two factors. A small subcarrier spacing Δf leads to a long symbol time T_s. Thereby, a better tolerance to multipath delays is achieved. On the other hand, reducing the Δf increases sensitivity to Doppler spread [Dah+08].

2.4.2 OFDM signal generation

Looking closely at equation (2.7) one can realize that it has the same structure as an inverse discrete Fourier transformation (IDFT):

$$s_{MC}\left(k\frac{T_s}{N}\right) = \sum_{n=0}^{N-1} d_n(i) \cdot e^{j2\pi nk/N} = N \cdot IDFT_N^{(n)}\{d_n(i)\}. \qquad (2.9)$$

Therefore, OFDM signals can be efficiently generated utilizing digital signal processing with the inverse fast Fourier transformation (IFFT) algorithm. This property is one of the most important advantages of OFDM, as otherwise N parallel I/Q modulators would be needed.

Fig. 2.10 shows the principle block diagram of digital OFDM signal generation. First, the serial data stream is distributed to N parallel streams and mapped to states in the constellation diagram. Hence, every single subcarrier is modulated individually, typically utilizing some kind of QAM modulation. An IFFT "mixes" each signal stream on the respective orthogonal subcarrier. Finally, the data is converted back into a serial baseband signal stream and a "cyclic prefix" is added to the signal before sending it to the RF modulator.

The frequency dependent channel causes a transient effect at the beginning of a transmitted symbol, leading to ICI as the subcarriers are not orthogonal any more during this time [Kam08]. Also, multipath propagation causes delay spread (fading), leading to inter symbol interference (ISI). Therefore, a cyclic prefix (sometimes also termed "guard interval") is added to the signal. This is done by copying the last samples of the symbol to its beginning, as illustrated in Fig. 2.11. As OFDM signals are cyclic by nature, this can be done without generating a discontinuity. The cyclic prefix must be longer than the channel impulse response. It gives time for the transient effects and thereby suppresses ICI and ISI effects. However, this obviously comes at the cost of reduced bandwidth efficiency, as redundancy is added to the signal.

The signal demodulation in the receiver is the inverse process of the above discussed signal generation scheme, utilizing an FFT algorithm.

The baseband spectrum of a 20 MHz wide 64 QAM OFDM signal which has been produced with Matlab® is shown in Fig. 2.12. The signal is generated according to the IEEE 802.11a/g/n WLAN standard. The subcarrier spacing is 312.5 kHz and the number of allocated subcarriers is 52. The total number of subcarriers is 64; the subcarriers at the edges of the spectrum as well as the subcarrier at DC are not allocated. According to the subcarrier spacing, one core symbol length is $T_s = (312.5\,\text{kHz})^{-1} = 3.2\,\mu\text{s}$. The guard interval length is $0.8\,\mu\text{s}$, leading to a complete symbol length of $4\,\mu\text{s}$.

The sampling rate of the signal shown in Fig. 2.12 is 80 MHz, hence the 20 MHz wide signal is oversampled by a factor of four. To achieve a good roll-off of the signal slope in the frequency domain, a pulse-forming is done with a raised-cosine filter in the time domain [Kam08, p. 612 ff.]. The OFDM symbol is multiplied by a raised-cosine window. The cosine roll-off factor is set to 0.0625 according to the WLAN standard.

As can be seen in Fig. 2.12 the subcarrier at $f = 0\,\text{Hz}$ is not allocated. The reason for this is, that it would require substantial effort for a typical homodyne
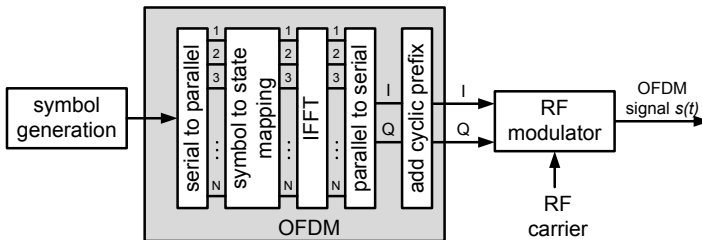
Figure 2.10: Using the inverse FFT to generate OFDM signals.
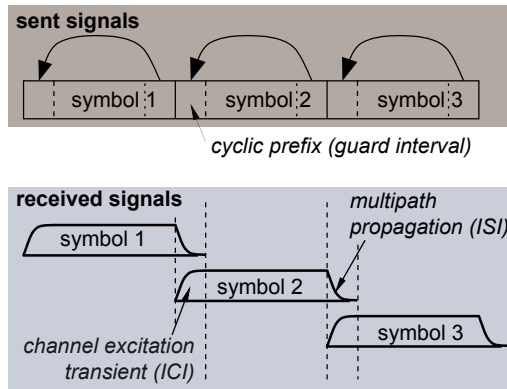
Figure 2.11: Adding a cyclic prefix to an OFDM signal helps against channel excitation transients that cause ICI and multipath propagation which leads to ISI effects.

receiver to properly receive signals at DC, owing to DC offsets.

2.4.3 Benefits- and drawbacks of OFDM systems

The way OFDM signals are generated has several advantages. The subcarriers can be flexibly allocated, thus the total OFDM bandwidth can be reconfigured. Also, an equalization of the subcarriers which suits the frequency dependent channel is possible. Furthermore, the signal processing is robust against narrowband blocker signals which only disturb single subcarriers. In addition, the cyclic prefix and the long symbol times make OFDM robust against fading effects.

OFDM has a high bandwidth efficiency when evaluated at 10 dB bandwidth. However, McCune [McC10, pp. 210–215] points out that the 60 dB bandwidth efficiency of OFDM signals is much smaller than that of Nyquist filtered single-carrier QAM signals of the same modulation order. The reason for this is that OFDM has waveform discontinuities between successive symbols, leading to a high occupied bandwidth!

Other drawbacks of OFDM signals are the low robustness against Doppler effect in moving environments, as this causes ICI. For the same reason, a good frequency synchronization between transmitter and receiver are necessary, leading to increased system costs.
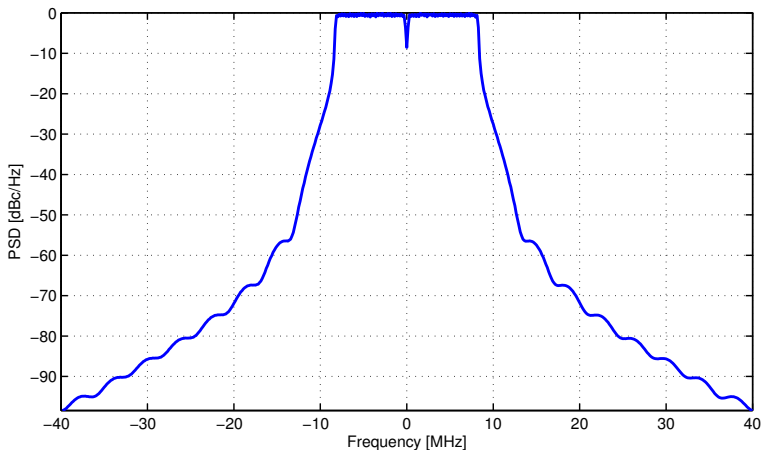
Figure 2.12: Spectrum of a 20 MHz wide WLAN 802.11a/g/n baseband signal sampled at $f_s = 80$ MHz.

Peak to average power ratio of OFDM signals

Regarding the requirements on the transmitter, the largest issue of OFDM signals is the high peak to average power ratio (PAPR).

The theoretical peak power of an OFDM signal is attained when all N independent subcarriers have a maximum magnitude A and the same phase. Then, a normalized amplitude of $N \cdot A$ volts is reached for a brief instant.

N independent subcarriers are having a total average power (supplied into a unit resistance) of

$$P_{subcar_{RMS}} = N \frac{A^2}{2}. \tag{2.10}$$

The PAPR can be calculated by dividing the signal power at the maximum amplitude by the average signal power. The theoretical maximum OFDM PAPR (in dB) thus can be calculated as:

$$PAPR_{OFDM} \leq 10 \log \left(\frac{(N \cdot A)^2}{N \frac{A^2}{2}} \right) = 10 \log(2N) \, \text{dB}. \tag{2.11}$$

As can be seen, the PAPR of an OFDM signal scales with the number of subcarriers N. The maximum PAPR vs. number of subcarriers is plotted in Fig 2.13.
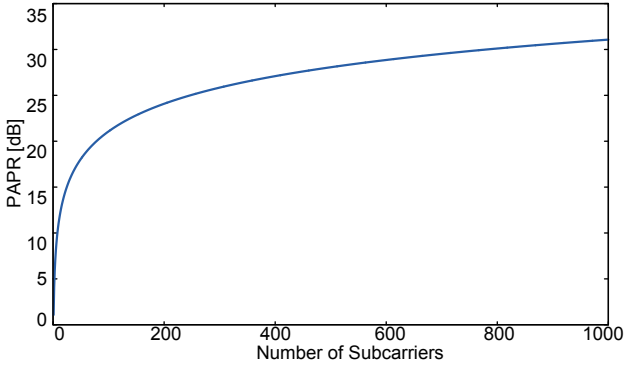
Figure 2.13: Maximum theoretical PAPR vs. number of OFDM subcarriers N.

For a large number of subcarriers, however, the probability of the event that all subcarriers are having the maximum magnitude and same phase is extremely low. Thus, normally not the maximum theoretical PAPR is given. Rather, usually the amplitude at the 10^{-4} point in the complementary cumulative distribution function (CCDF)[2] is chosen as peak amplitude [McC10]. This means that an envelope magnitude which is higher than the selected value has only an occurrence probability of 10^{-4}. Taking this measure, the PAPR of OFDM signals does not exceed 15 dB, even for higher values of N. For low values of N, however, equation (2.11) is a good approximation of the PAPR [McC10, p. 217]. CCDF curves for LTE uplink and downlink OFDM signals are plotted in Fig. 2.15.

PAPR values as high as 15 dB are still very high numbers when compared to single carrier QAM signals which have PAPRs of only about five to six dB. A high PAPR is a severe issue for the transmitter. The power amplifier must be able to deliver the full peak output power, so that the signal is not distorted. Thus, a very large and consequently costly PA is needed. For most of the time, however, the PA only has to deliver the average output power, which is around 15 dB lower. Thus, the PA is somewhat oversized for the typical operation. Unfortunately, PAs typically have a very low energy efficiency, when operated in backoff. As the PA consumes the largest portion of energy in the whole transmitter, a low PA efficiency directly translates to a low overall system energy

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[2] Depending on the source, sometimes also the 10^{-3} probability point in the CCDF curve is given, leading to much lower PAPR values. Often, it is not specified at which point the PAPR of a signal is measured, which makes it quite complicated to compare different sources.
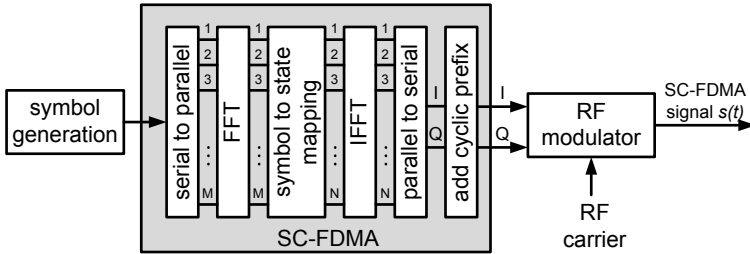
Figure 2.14: SC-FDMA baseband encoding.

efficiency. The problem of the PA is thoroughly discussed in chapter 3.

2.4.4 EVM calculations in OFDM systems

EVM calculations are a bit special for OFDM systems, as there is an own constellation diagram for each subcarrier. Therefore, EVM is first calculated separately for each subcarrier. Afterwards, the EVM values are averaged over all subcarriers and an EVM_{rms} is given [McK+04].

2.4.5 OFDM-based communications standards

Several modern mobile communication standards for high data rate transmission are based on OFDM. The most important ones are probably Wireless LAN (IEEE 802.11x), WiMAX mobile (IEEE 802.16e), and 3GPP LTE. The properties of these standards, which are relevant for the RF transmitter frontend, are summarized in Table 2.1.

LTE and SC-FDMA

3GPP long-term evolution (LTE) is the successor of the UMTS/WCDMA mobile standard. While UMTS – including the "High Speed Packet Access" (HSPA) high data rate enhancements – is based on single-carrier QAM modulation, LTE is based on OFDM.

LTE uses different modulation types for downlink (from the base station to the mobile device) and uplink (from the mobile device to the base station) transmission. The downlink uses ordinary OFDM, the uplink on the other hand uses a special signal type termed "Single Carrier Frequency Division Multiple Access" (SC-FDMA). Although it is called "single carrier", it really is a form of OFDM with some modifications in the signal processing.

The SC-FDMA signal generation is shown in Fig. 2.14. It is derived from the regular OFDM architecture, shown in Fig. 2.10. The first step in SC-FDMA modulation, however, is to perform an additional M-point DFT [Myu+06]. This step is used to "scramble" the regular QAM signal state into another set of signal states for each subcarrier. Therefore, this type of transmission scheme is also called "DFT-spread OFDM" (DFTS-OFDM). Afterwards, the size-N IDFT, with N>M, generates the regular OFDM waveform. The unused inputs of the IDFT are set to zero, hence creating unallocated subcarriers. The DFT "scrambling" leads to a reduced probability that all subcarriers align to a large signal amplitude peak.

By applying DFT-spread OFDM, the PAPR can be reduced in the order of 3 dB, as the comparison between CCDF curves of an regular OFDM and a DFTS-OFDM signal in Fig. 2.15 reveals. The dashed curves represent 16QAM modulated signals, the solid curves represent QPSK modulated signal. While the PAPR of the DFTS-OFDM signal is dependent on the modulation scheme, the (higher) PAPR of OFDM signals is relatively constant, as for the latter all subcarriers are independent, leading to an approximately exponential distribution of the instantaneous power [Dah+08, p. 76].
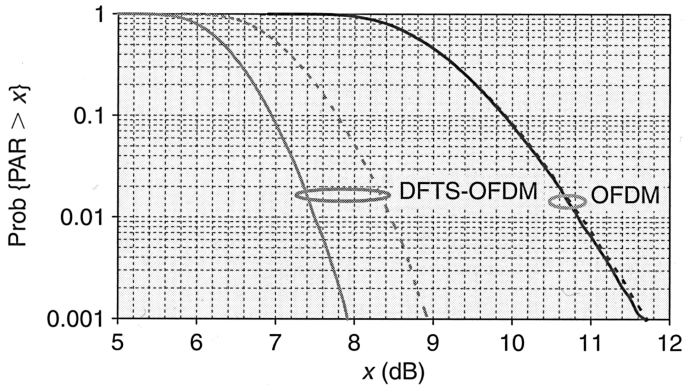
Figure 2.15: PAPR curves of OFDM and DTFS-OFDM (SC-FDMA). Solid curves are for QPSK modulation, dashed curves are for 16QAM modulation [Dah+08, p. 75].

As a result of the reduced PAPR a PA with lower maximum output power can be used, decreasing the cost of the handset and increasing the handsets energy efficiency. The SC-FDMA signal has all benefits that were discussed for OFDM signals in section 2.4.3. The most important drawback of SC-FDMA signals is

the increased digital signal processing. The largest effort, however, has to be done on the receiver side, which is the base station. As this is not battery driven, in contrast to the mobile device, the increased power consumption at this point is not too critical.

Although the PAPR is reduced by about 3 dB for SC-FDMA signals compared to OFDM, it is still much higher than for comparable QAM signals. With a PAPR of nearly 10 dB the LTE power amplifier must still be overscaled by a factor of 10. To generate a maximum average output power of +23 dBm (200 mW), it must be capable to deliver a linear peak output power of +33 dBm (2 W).

System	Wireless LAN	WiMAX mobile	LTE downlink	LTE uplink
Signal class	OFDM	OFDM	OFDM	SC-FDMA
Max. data rate [MBps]	248 (/w 4x MIMO)	30	100	50
Bandwidth [MHz]	20 and 40	1.25 to 20	1.4 to 20	1.4 to 20
Number of subcarriers	52, 104, or 114	512	1200	1200
Subcarr. spacing [kHz]	312.5	10.94	15	15
Modulation	BPSK; 4, 16, 64 QAM	4, 16, 64 QAM	QPSK; 4, 16, 64 QAM	BPSK; QPSK; 8PSK; 16QAM
Frequency bands (in Germany)	2.4 GHz ISM and 5 GHz ISM	2.1-2.7 GHz and 4.1 to 5 GHz	2.62-2.69 GHz and 791-821 MHz	2.52-2.57 GHz and 832-862 MHz
Max. average output power [dBm]	≤+20 (EIRP)	+23	no upper limit (+24 for local area BS)	+23
Min. average output power [dBm]	-	-	-	-40
PAPR [dB]	12-16	10-15	11-12	9
max. EVM	5.6%	5%	9.0% (for 64QAM)	12.5% (16QAM)
Multiple access	TDMA	TDMA	OFDMA	OFDMA
Duplex type	TDD	TDD	FDD (or TDD)	FDD (or TDD)
Committee	IEEE 802.11n	IEEE 802.16e	3GPP	3GPP

Table 2.1: Overview of important OFDM-based wireless communication standards.

3 Challenges for Integrated CMOS Power Amplifiers

3.1 Introduction

The power amplifier (PA) is one of the most important parts of every RF transmitter. Most PAs for mobile devices are based on high-performance SiGe or GaAs technologies, which leads to quite high production costs. The transceiver and baseband circuitry on the other hand are preferably designed using standard low-cost CMOS technology. Typically, for each communication standard and frequency band which the mobile communication device supports a dedicated PA is needed. For example, according to iSuppli [iSu10], Apple's iPhone 4 contains five different PA modules that are required to support the different GSM/EDGE and WCDMA frequency bands. Each PA module again potentially contains several different PA chips. This leads to an increased bill of materials and also needs a large PCB area.

PAs in standard CMOS would allow the full integration of a complete radio system on a single chip [Haj05], resulting in considerable cost and size reductions. PAs in modern sub-micron CMOS processes with performances approaching SiGe and GaAs PAs are therefore of great interest, although their design is a big challenge. As CMOS is scaled down the roadmap, the design of high performance PAs becomes more and more demanding. This is mainly due to the necessary reduction of the supply voltage, which limits the maximum power capability [Sch+06]. Until recently, few single-chip radios with integrated PAs have been demonstrated. The available fully integrated radios are mostly solutions for connectivity standards such as WLAN and Bluetooth with required output power levels far below +20 dBm. In [Kho+05] a fully integrated SOC for 802.11b is presented which has +13 dBm nominal output power. In [Beh+07] a multiband, MIMO IEEE 802.11n chip with a 1 dB compression point of +14 dBm is shown. A Bluetooth EDR chip with a nominal output power of +3 dBm is presented in [Mar+07].

Subsequently, it shall be investigated what are the power and performance limits of PAs in today's available standard CMOS technology. Thereby, it can be concluded for what kind of mobile communication system the full-integration of the PA into a single-chip radio is feasible. To achieve this goal, two different two-stage PA prototypes in 0.13 μm CMOS were developed and

manufactured [Zim+07]. The two implemented PAs mainly differ the connection between the amplifier stages. The first PA has transformer coupled stages, while the second has capacitor coupled stages.

The PAs that are presented below are intended for a PA-integration into a true single chip DECT phone, like it has been presented by Grewing et al. [Gre+07]. A major challenge of the PA design is the low breakdown voltage of standard CMOS transistors. Special care has been taken to achieve the necessary power levels, while remaining a reliable operation for supply voltages of up to 3.6 V [Zim+08a].

3.2 PA design and implementation

Simplified schematics of the two developed PAs are shown in Fig. 3.1 and Fig. 3.2. Both PAs consist of two amplifier stages. The linear PAs are biased to class AB operation. While the transistor stages and padframe are identical for both PAs, they differ in the interstage matching network. The output stages use transistors with a width of 7.8 mm each. The width of the driver stage transistors is 2 mm.

3.2.1 Differential structure

Both presented PAs are differential class AB power amplifiers. The differential design features a virtual ground, which makes it robust against parasitic inductance from the bondwires and leads to a good cancellation of the even harmonics. The differential structure is especially important for the integration of the PA into a monolithic transceiver, since it reduces the disturbance to other building blocks through large PA signals. Furthermore, the push-pull combination scheme has a 4:1 load-line impedance benefit in an equal power comparison to a simple single-ended or parallel device connection. Therefore, a lower load impedance transformation ratio can be used for the matching network, which leads to lower output currents and lower losses in the matching network. However, in comparison to a single-ended implementation, an additional RF output pad is required and a balun (balanced-to-unbalanced converter) is needed at the output of the PA, introducing additional cost and also some losses.

3.2.2 PA with capacitor coupled stages

A simplified schematic of the PA with capacitor coupled stages is shown in Fig. 3.1. The two amplifier stages are coupled by capacitors (C_2), therefore the biasing of output stage can be set independently from the driver stage. Inductors (L_2) are needed to resonate out the big parasitic capacitances of the 7.8 mm wide output stage transistors, so the first stage only has to drive a purely resistive load.
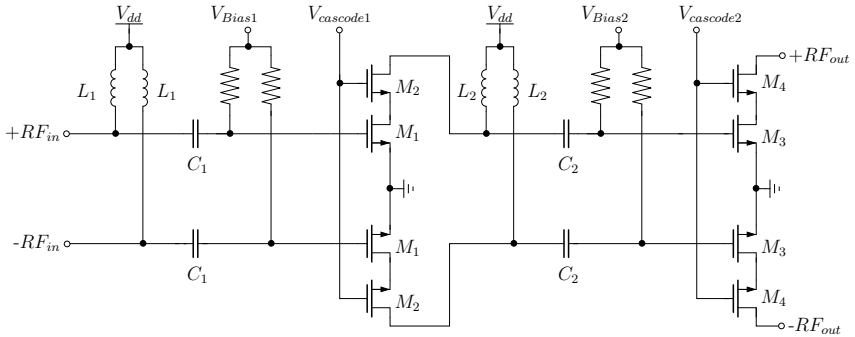
Figure 3.1: Simplified schematic of the power amplifier with capacitor coupled stages.

An interstage matching of this kind is widely used for two-stage PAs [WD97; Mat+00; Kan+06].

The coupling capacitors C_2 form a voltage divider together with the parasitic capacitances of the output stage. To minimize the voltage drop over C_2, the coupling capacitors have to be made very large. In this case, the overall input capacitance of the output stage is dominated by the parasitic capacitances. However, as the parasitic capacitances are quite large, this limits the value of the spiral inductors L_2 for a given resonance frequency. It is beneficial to use smaller coupling capacitors and larger inductances L_2. While this leads to a higher voltage drop over C_2, the overall input capacitance of the second stage is decreased and the inductance of L_2 consequently can be made larger. Thereby, the voltage gain of the first stage is increased significantly since its load impedance is higher. Optimum values for L_2 and C_2 can be found by doing some iterations in the design process.

3.2.3 PA with transformer coupled stages

The schematic of the transformer coupled PA is shown in Fig. 3.2. For interstage and input matching two on-chip transformers are utilized.

Through the magnetic coupling of the transformers, the amplifier stages are coupled while being galvanically isolated. Therefore, the biasing can be set independently for both stages and no large coupling-capacitors are needed. As can be seen in Fig. 3.2 current mirrors can be used for biasing, utilizing the transformer center taps. For the prototype design it is also possible to directly feed a biasing voltage to the transformer center taps from the outside.
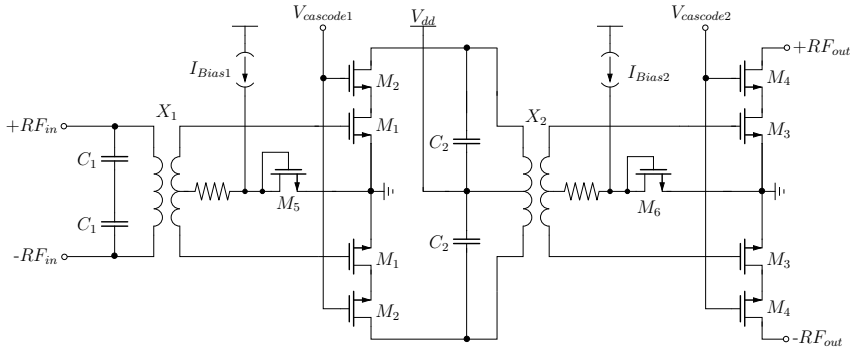
Figure 3.2: Simplified schematic of the PA with transformer coupled stages.

Integrated transformers are not so commonly used, but have been applied for RF components such as PAs [Sim+99] and mixers [Lon00]. An accurate design demands a precise modeling and for this work, a transformer model as presented in [Keh+01] has been used. The transformer equivalent circuit, which includes the inductances of the windings, coupling between the primary and secondary side, parasitic capacitances, losses through series resistances and coupling with the substrate, is shown in Fig. 3.3. The transformer inductances have to be designed in such a way that the resonant circuits comprising of the transformers X_1 and X_2, the parasitic capacitances, and the tuning capacitances C_1 and C_2, respectively, have their center frequency at the operating frequency of the PA.

By varying the transformation ratio and size – and therefore inductance – of the transformers, a good interstage and input matching can be found. The first transformer, X_1, has a winding ratio of 3:2 while the second transformer, X_2, has a winding ratio of 2:1.

However, the design space is limited by the large parasitic capacitances of the transistors. This problem is more severe with CMOS than with bipolar devices and getting even worse for higher frequencies. The cross-coupled dual resonant networks on both sides of the transformers [Que02] make it especially difficult to find the optimum values for the transformer design. This problem is tightened through the fact that transformers are not supported by many RF design tools.

In addition to the benefits mentioned above, for a stand-alone PA chip the input transformer has many useful features:

- No DC-block capacitor is needed.

- The input signal can be applied balanced or unbalanced.

- No ESD protection is needed at the input.
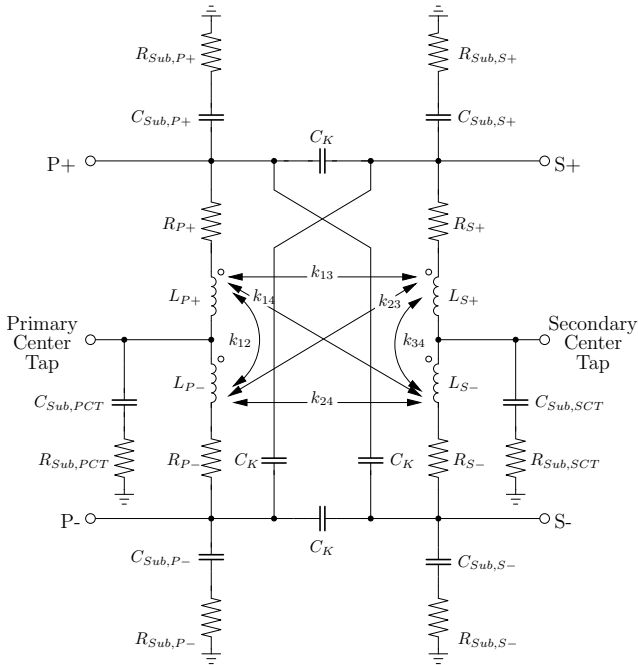
Figure 3.3: An equivalent circuit for the transformers.

- The input matching can be done without external components.

3.2.4 Design for high supply voltages

The PAs were designed for the integration into a single-chip DECT transceiver, which is operated on a two battery cell supply. The PA is directly connected to the battery. The typical battery voltage of two NiMH cells connected in series is 2.5 V, but the supply voltage can reach up to 3.6 V for very short times and up to 3.0 V for some extended time when the battery connected to a charger. This can lead to severe reliability problems. These are on one hand the threat of an immediate transistor breakdown due to overly high voltages and on the other hand long term performance degradation problems caused by electromigration and the hot carrier effect [Par+00].

Electromigration denotes an unwanted transport of ions in the metallic backend wiring of a chip. It may cause voids or even gaps in the interconnect wiring,
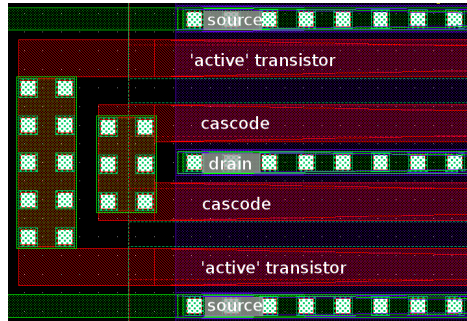
Figure 3.4: Layout of the double gate transistor.

leading to a destruction of the chip. Electromigration is especially an issue when large DC current densities are present in a circuit.

The hot carrier effect occurs when channel electrons cause damage to the Si-SiO$_2$ interface due to high electric fields near the drain. Thereby, the threshold voltage of the MOSFET is increased while the transconductance is decreased.

Finally, the CMOS transistor is threatened by an immediate breakdown of gate-oxide or PN-junction if it is exposed to overly high voltages. The gate oxide breakdown voltage in the used 0.13 μm technology lies between 4.5 V and 8.5 V depending on transistor type. The reverse-bias breakdown voltage of PN-junctions is about 7 V.

A dynamically changing environment can lead to load mismatches at the antenna, even if the antenna is perfectly matched under normal conditions. This causes reflection of the transmitted signal and finally standing waves, with high voltages at the PA output. Amplitude and phase of the reflected signal can be quantified in terms of the reflection factor ρ. If the transmitted signal has a amplitude of V_f, the standing wave has a maximum amplitude of $V_{max} = V_f(1 + |\rho|)$. Thus the standing wave can reach twice the amplitude of the transmitted wave when strong mismatches apply. A measure for the load mismatch is the Voltage Standing Wave Ration (VSWR), which is the ratio between maximum and minimum voltage of the standing wave.

$$VSWR = \frac{V_{max}}{V_{min}} = \frac{1 + |\rho|}{1 - |\rho|} \tag{3.1}$$

An earlier presented 0.13 μm CMOS PA with a comparable output power showed good performance, but had reliability problems already at low supply voltages above 1.2 V [Vas+04]. Therefore special emphasis has been placed on reliability issues for design and layout.

A class AB amplifier will generate almost $2 \cdot V_{DD}$ peak voltage at the drain outputs. A cascoded output stage configuration using 3.3 V compatible thick gate-oxide transistors with 400 nm gate length is implemented to deal with the high drain voltages at the output transistors. However, the thick gate oxide and the large required gate-length reduce the transconductance and increase the required area and thus parasitic capacitances of the transistors in comparison to normal 130 nm thin-gate oxide transistors. Hence, the PA performance in terms of gain, maximum output power and power efficiency is reduced. A "double gate" layout of the cascode, shown in Fig. 3.4, with a "drain - cascode gate - active transistor gate - source" configuration instead of two separated transistors has been used for the amplifier stages. This leads to lower parasitic capacitances compared to a separated active and cascode transistor configuration and allows a compact layout. However, as the active and cascode transistors are determined to have the same width, the design flexibility is reduced.

If the cascode gate voltage $V_{cascode}$ is connected to V_{dd}, it leads to the smallest gate-drain voltages and is therefore the best solution regarding the reliability. However, reducing $V_{cascode}$ by some 100 mV decreases the smallest drain-source-voltage in which the cascode transistor operates in the saturated region. It therefore allows a higher output voltage swing which leads to a superior performance.

The output stage uses transistors with 260 fingers each, 30 µm wide, with a total width of 7.8 mm. The width of the driver stage transistors is 2 mm. Additional estimated parasitic capacitances and inductances from the layout were added in the design.

As research shows, linear amplifiers of the class-A type generally have lower problems with hot-carrier degradation and Fowler-Nordheim stress compared to switched mode class-E amplifiers [Lin+05]. The lower reliability of class-E PAs originates from the much higher stress levels that occur because of the switching.

3.3 Experimental results

Die photographs of the fabricated power amplifiers are shown in Fig. 3.5(a) for the PA with capacitor coupled stages and in Fig. 3.5(b) for the transformer-based PA.

The chips measure $1.0 \times 1.0 \, \text{mm}^2$ and $1.0 \times 1.2 \, \text{mm}^2$ respectively, although the active area is only about $0.4 \, \text{mm}^2$ for both circuits. The on-chip transformers and coils, top-metal MIM-capacitors and feed lines for the transistor stages can be easily identified. The PAs have been fabricated in a 0.13 µm standard CMOS technology.

(a) PA with capacitor coupled stages

(b) PA with transformer coupled stages
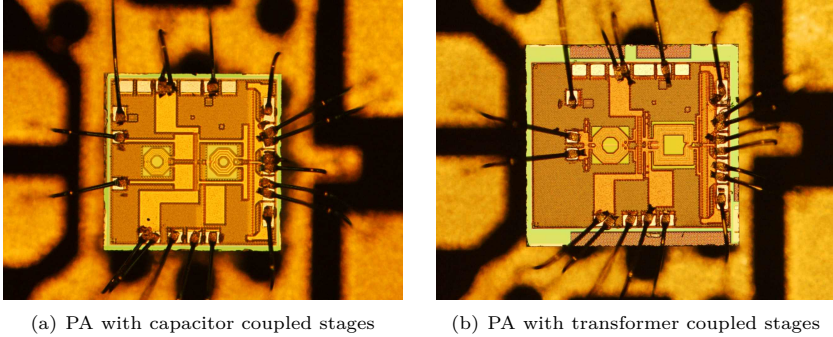
Figure 3.5: Chip photos of the two power amplifiers, fabricated in 130 nm CMOS. Utilized chipsize is $1.0 \times 1.0\,\text{mm}^2$, including pads. The dies are directly bonded onto the RF test PCB.

3.3.1 Measurement setup

For measurement of the prototype, the dies were glued to a PCB and wire bonded directly onto the PCB microstrips. For the bonding a relatively low number of output and grounding bond wires were used (see also Fig. 3.5(a) and Fig. 3.5(b)) to get a realistic impression of what can be achieved when integrating the PA into a single-chip radio with a low-cost package. The PCBs are 0.5 mm thick FR4 boards with an ϵ_r of 4.5 and a $\tan\delta$ of 0.025.

For differential-to-single-ended conversion and load impedance transformation the PCBs feature a lattice-type microstrip LC-balun as described in [Bak+02]. A principle drawing of the balun is shown in Fig. 3.6(a). With component reactances of

$$X_B = \omega L_1 = \omega L_2 = \frac{1}{\omega C_1} = \frac{1}{\omega C_2} \tag{3.2}$$

the balun transforms the single ended antenna impedance (Z_{unbal}) to a differential impedance of

$$Z_{bal} = \frac{X_B{}^2}{Z_{unbal}} \tag{3.3}$$

at the PA output.

While L_1, L_2 and C_2 are realized as microstrip lines in this design, C_1 is an SMD capacitor. Instead of an RF choke inductor, a quarter wavelength microstrip line has been utilized. A photo of the PCB is shown in Fig. 3.6(b).

The output power of the PAs is measured at the SMA connector at the single-ended side of the balun, thus signal losses in the balun and the board are
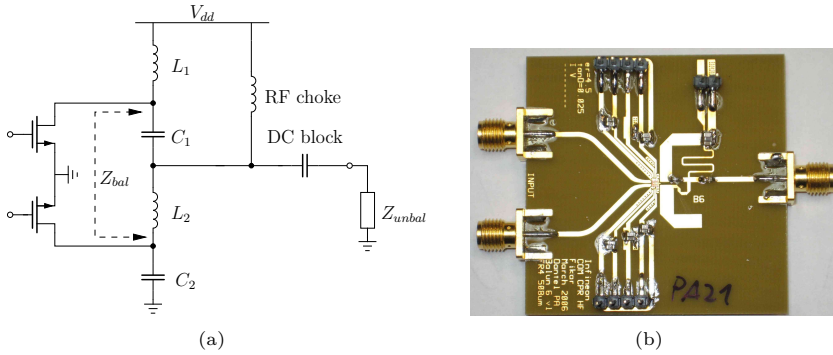
Figure 3.6: Lattice-type *LC*-balun with inherent impedance transformation.
(a) Schematic and (b) realization with microstrip lines on a PCB .

included in the measurement results. All measurements have been done under continuous-wave (cw) conditions. In pulsed mode with reduced duty cycle the heating of the PA is lower, therefore a slightly increased output power and also efficiency can be expected.

3.3.2 Measurement results

Transformer coupled PA

A plot of the measured output power and PAE vs. input power at nominal conditions of 2.5 V supply voltage and a frequency of 1.9 GHz are shown in Fig. 3.7. The PA can deliver 27.4 dBm (550 mW) with a PAE of 34%. The small signal gain is 24 dB. Fig. 3.8 shows the frequency response of the PA, also for 2.5 V supply voltage and an input power of 5 dBm. Although the center frequency is a bit lower than the targeted 1.9 GHz, the PA is well-tuned for the DECT bands 1880-1900 MHz and 1910-1930 MHz (U.S. DECT).

Capacitor coupled PA

For the capacitor-coupled PA the same measurements under the same conditions as for the transformer-based PA were done. A plot of the output power and PAE vs. input power is shown in Fig. 3.9. The PA delivers 27.2 dBm, the max. PAE is 37% and therefore slightly better than for the transformer coupled PA. The higher small signal gain of 28 dB results from the better amplification of the first stage. This is due to a higher interstage matching input impedance that could be achieved with the *LC* match. In Fig. 3.10 the frequency response of the PA
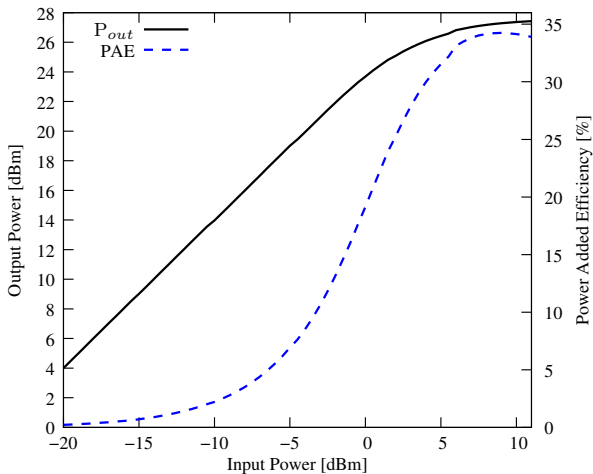
Figure 3.7: Measured output power and PAE vs. input power of the PA with transformer coupled stages, at 1.9 GHz.
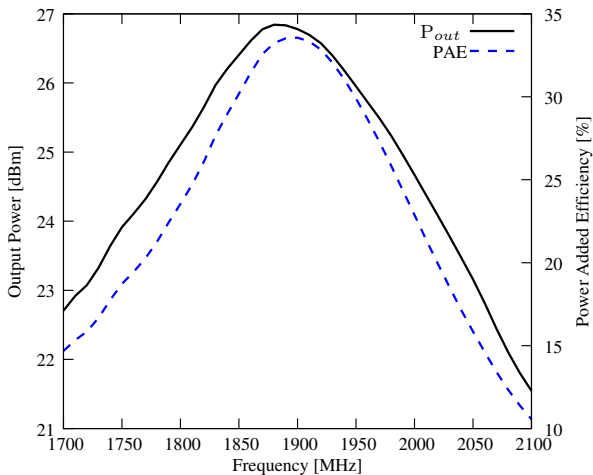
Figure 3.8: Measured output power and PAE vs. frequency of the PA with transformer coupled stages, with 5 dBm input power.
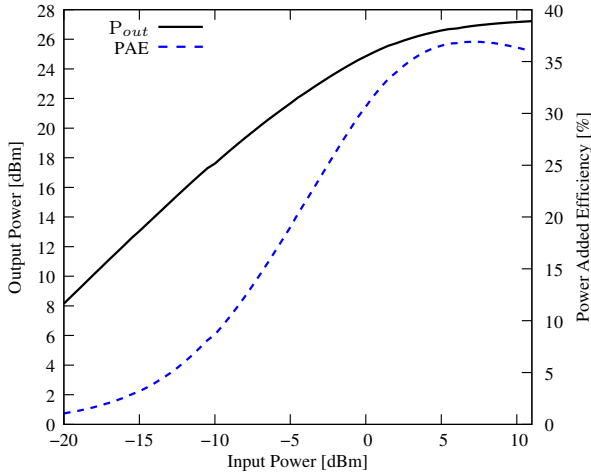
Figure 3.9: Measured output power and PAE vs. input power of the PA with capacitor coupled stages, at 1.9 GHz.
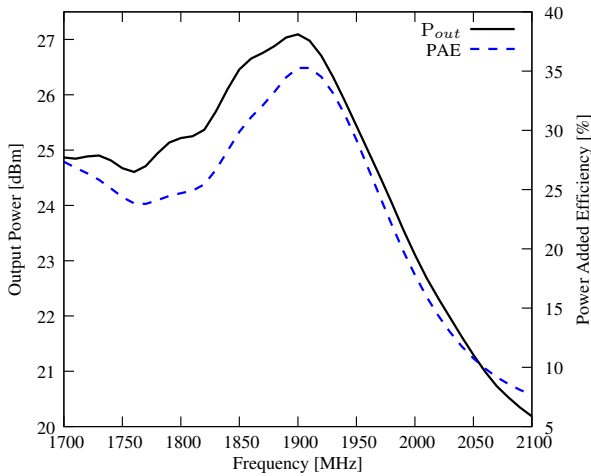
Figure 3.10: Measured output power and PAE vs. frequency of the PA with capacitor coupled stages, with 5 dBm input power.

is shown. It can be seen that the output power and PAE remain relatively high below the center frequency, but drop a bit faster for higher frequencies compared to the transformer-based PA. This is caused by a shift of the center frequency in one of the two matching circuits.

Both PAs meet the requirements for DECT, which is 24 dBm transmit signal power at the antenna, which translates to about 26 dBm at the PA output.

3.3.3 Reliability analysis

The RF performance of analog CMOS circuits can be degraded through the hot carrier effect. To evaluate the influence of the hot carrier effect, a long term measurement of the hot carrier degradation has been accomplished with the capacitor coupled PA and compared with [Vat+01], which shows an output power drop of 0.8 dB in only 80 hours of operation time. The PA was operated at 3.6 V supply voltage and biased to deliver 26.5 dBm of output power at 5 dBm input power. After 170 hours (7 days) of operation with 100% duty cycle, the PA showed no output power performance degradation, which shows the robustness of this PA design.

A ruggedness measurement has been conducted to test the sensitivity against load mismatches with a resulting high VSWR. The supply voltage has been raised in steps and an open or short condition has been applied at the SMA antenna connector. The supply voltage could be raised up to 6 V until the PA output stage broke down! This shows that the topology of the output stage described in section 3.2.4 gives a very good ruggedness against high supply voltages and VSWRs.

3.4 Active over-voltage protection circuits

The over-voltage protection, which has been discussed above, is grounded on the utilization of a high-voltage compliant thick-gateoxide transistors. Manufacturing of these devices necessitates additional process steps and therefore means additional costs. Also, RF performance of these transistors is generally inferior to standard thin-gate oxide transistors. Finally, a lot of semiconductor companies are "fabless" and manufacture at independent semiconductor foundries, making it difficult to integrate special high-voltage transistors into the processes.

Therefore, solving the issue on circuit level is a promising alternative. In [Scu+05] a voltage feedback circuit to avoid overvoltages is presented. However, this circuit is only realizable with bipolar transistors, making it unsuitable for CMOS PAs.

In [Zim+08b] a VSWR protection circuit for CMOS PAs is presented. Critically high voltages at the PA's open drain outputs are sensed by an overvoltage detection circuit. If a critically high voltage is detected, it dynamically lowers

biasing and gain of the amplifying stages, thereby immediately lowering the output voltage level back to an uncritical value.

3.5 Conclusions and discussion of the results

Two PAs intended for DECT applications were presented above. They both have an output power of more than +27 dBm and fulfill the DECT requirement. Using the presented results as a basis, a full integration of a similar power amplifier into a true single-chip DECT telephone could be realized [Gre+07]. This shows that it is feasible to build CMOS power amplifiers with almost Watt-level output powers in standard CMOS technologies and integrate them with an RF transceiver and baseband signal processing in one single chip.

3.5.1 Feasibility of single-chip radios with integrated CMOS PA for cellular standards

Subsequently, the technological limits and challenges of a PA integration into a single-chip transceiver for different communication standards are discussed. It shall be concluded for which kind of communication system, besides DECT, such a PA integration is feasible and for which it is not, assuming the utilization of state-of-the-art CMOS technology.

In literature, CMOS PAs with even higher peak output power than the above presented PAs with levels up to +35 dBm can be found [Cho+09; Aok+08]. To achieve this, their architecture is based on the power combination of N parallel PAs through a transformer, where the secondary (output) coils of N transformers are connected in series and their primary (input) coils are connected in parallel. This has got especially popular with the invention of the so-called "distributed active transformer" (DAT) by Aoki et al. [Aok+02], where the transformer is constructed out of "slab" inductors. To be able to build a low-loss integrated power combination network, however, a special chip backend with very thick metal layers is needed. This, of course, means increased production costs compared to standard CMOS solutions with a conventional wiring backend. Therefore, it is not compatible with the idea of building a fully integrated low-cost single-chip radio in digital-centric nanoscale standard CMOS.

Looking at the output power levels measured in section 3.3.2, it can be seen that peak output power levels of around 500 mW (+27 dBm) are feasible with standard CMOS. With power-combination techniques like the DAT even output levels above +30 dB are possible. However, these are always *peak* power levels where the PA is operated in strong compression. The peak output power only equals the defined *maximum average* power level for modulation schemes with a constant signal envelope. This is the case for communication standards like

DECT or GSM, which both have a GMSK modulation scheme.[1] For high-data-rate communication standards with envelope varying amplitude modulation schemes such as WLAN, WCDMA (UMTS) or LTE, however, a linear power amplifier is needed.[2] If the communication standard demands a linear signal amplification, it can be seen from the measurements in Fig. 3.7 and Fig. 3.9 that a maximum uncompressed output power of around $+24\,\text{dBm}$ can be reached. The *average* output power level is even below this level. It is reduced by the peak to average power ratio (PAPR) of the utilized modulation scheme. QAM modulation schemes that are used for WCDMA and HSPA have a PAPR of 3 to 7 dB (depending on the modulation order). OFDM modulation schemes as discussed in section 2.4.3 for WLAN and LTE even have higher PAPRs of 11 to 17 dB [McC10, pp. 392–400].

Connectivity devices such as WLAN and Bluetooth (BT) have relatively low output power levels which are significantly below $+20\,\text{dBm}$. WLAN IEEE 802.11x defines a maximum EIRP of $+20\,\text{dBm}$, BT class 1 devices – which are the devices with the highest output power defined for BT – also have a maximum output power of $+20\,\text{dBm}$. Because of the antenna gain which has to be taken into account for EIRP, the maximum average PA output power is some dB lower.

High-data-rate cellular standards, on the other hand, require a much higher (average) output power. UMTS, for example, has a defined maximum average output power of $+24\,\text{dBm}$ and LTE has maximum average output power of $+23\,\text{dBm}$.

Therefore, single chip solutions with integrated power amplifiers today can only be found for wireless connectivity radios such as WLAN or Bluetooth [Lee+10; Afs+09; Beh+07]. The 1 dB compression point of these devices is far below $+20\,\text{dBm}$. The fully integrated device with the highest reported output power is the DECT chip of Grewing et al. [Gre+07] with an output power of $+26\,\text{dBm}$. The constant envelope modulation scheme of DECT, however, allows to operate the PA in saturation. From the discussion above, it can be concluded that it is unfeasible – or at least very hard – to build a fully integrated single-chip transceiver in today's low-cost standard CMOS for high-data-rate cellular standards such as LTE or WCDMA (HSUPA).

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[1] Where DECT has a defined maximum output power of $+24\,\text{dBm}$ at the antenna and GSM has a much higher maximum output power of $+33\,\text{dBm}$.

[2] Unless a polar modulator architecture or LINC is used, which, on the other hand, limits the usable signal bandwidth as discussed in sections 2.3.2 and 5.4.1.

4 RF-DAC Fundamentals

Scope of this work is to develop a transmitter architecture, which is compatible with modern broadband high-data-rate communication standards. At the same time it must be cost efficient as it is targeted on the highly competitive mobile communications consumer market.

To achieve low production costs at high quantities of sold units, the transmitter must be highly integrated in a nanoscale CMOS process. Thereby, the number of bulky and expensive external components as well as the production cost of the transceiver chip can be minimized. Nanoscale CMOS processes are perfectly suited for digital circuits as they allow high processing speed at a low power and area consumption. However, the analog performance – besides a high transit frequency f_t of the transistors – of these technologies increasingly worsens with decreasing feature size. This is mainly due to the low supply voltages that may be applied to nanoscale CMOS transistors which have a gate oxide thickness in the low single-digit nanometer range. Also, the analog performance suffers from short-channel transistor effects. Therefore, novel circuit implementations and system architectures have to be found that allow to cope with a relatively poor analog transistor performance.

A second challenge for the development of a low-cost reconfigurable transmitter are the high performance requirements of novel high-data-rate OFDM-based communication standards such as LTE and WLAN. Still, legacy standards as GSM and UMTS have to be supported, as these will most likely be present for many years to come. To limit the hardware cost and the size of a multistandard communication device like a smartphone, the transmitter should be highly reconfigurable, thereby being able to service different radio standards with the same hardware. This demands a reconfigurable high-performance analog and RF frontend which is able to fulfill the different performance requirements of all supported radio standards.

As discussed in the previous chapter, it is not feasible with state-of-the art technology to integrate a power amplifier into a single-chip radio which is capable to deliver the high output power that is needed for cellular standards. Thus, a solution which consists of a fully integrated, flexible, low-cost modulator plus an external PA has to be found.

Subsequently, different possible solutions for multistandard, multimode transmitters are discussed. These have to be as "digital" as possible. By replacing the analog baseband processing with digital blocks, the transmitter can be made

highly reconfigurable. The most promising approach for such a "direct-digital" transmitter is the RF-DAC. Different earlier published RF-DAC implementations are presented. Also, drawbacks of RF-DAC based transmitters, namely unwanted spurious emissions, are discussed and techniques to reduce these unwanted emissions are introduced.

4.1 Basic idea of the RF-DAC transmitter

In recent years, several ideas for building reconfigurable, "direct-digital" transmitters have been published [Elo+07; JS07; Tal+08]. They are based on the direct conversion of a digital baseband signal into an analog RF output signal, by using a building block which combines D/A conversion and upconversion mixing. The first implementations of this technique were introduced by Zhou and Yuan [ZY02] and Luschas et al. [Lus+04]. The digital-to-RF converter was termed "RF-DAC". It seems to be an excellent alternative to classical analog transmitter architectures which have been used for many decades.

4.1.1 Current-steering DACs

The idea of all RF-DAC structures originates in a conventional current-steering DAC [Raz95, p. 84 ff.]. The working principle of a current steering DAC is shown in Fig. 4.1. It consists of a number of parallel switched current sources, the DAC unit cells. Each unit cell is built by a weighted fixed current source and a switching pair, which steers the current to either the output or dumps it to ground, depending on the digital input data. Alternatively to dumping the current to ground, a current steering between two differential outputs I_{out+} or I_{out-} is also possible. The weighted currents of all parallel unit cells are summed at the output and converted into a voltage by a transimpedance stage, if necessary. This D/A converter structure is especially popular for high-speed applications as it can directly drive a resistive load. No high-speed amplifier is needed at the output and hence current steering DACs are potentially faster than other DAC topologies.

The simplest construction of a N bit current-steering DAC is an architecture with N parallel binary weighted current sources as depicted in Fig. 4.1. This architecture, however, suffers from two drawbacks:

First, device matching problems can lead to nonlinearities and even a nonmonotonic behavior in the output current when switching from one output value to the next. This is especially an issue when switching from a value $2^n - 1$ to 2^n, where all currently active current sources (I_0 to I_{n-1}) have to be switched off and the next larger source I_n is switched on. Performance metrics for measuring these nonlinear effects are the *differential nonlinearity* (DNL), which is the maximum deviation in the output step size from the ideal value of one least
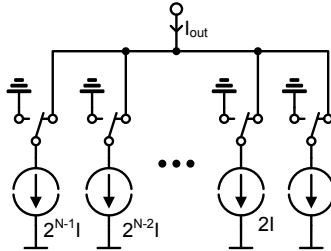
Figure 4.1: Principle of a current steering DAC. The currents of parallel, weighted current source unit-cells are summed to a total DAC output current I_{out}.

significant bit (LSB), and the *integral nonlinearity* (INL), which is the maximum deviation of the input/output characteristic from a straight line passed through its end points [Raz95, p.48 f.].

The second drawback of a binary weighted architecture are large glitches which can occur when switching between large current sources. These glitches are caused by the finite and potentially unequal rise and fall times of the current sources as well as timing skews.

A topology which remedies these drawbacks is the unary weighted architecture, consisting of $2^N - 1$ nominally identical current sources. As the digital input increases, more and more current sources are switched to the output without the need of turning off any current source. Thereby, monotonicity is guaranteed and glitch impulses are small. A thermometer decoding logic is required to convert the binary input data into control bits for each switch.

Anyhow, the number of unit cells grows exponentially with the resolution of the unary weighted DAC. Hence, for high DAC resolutions and thus high values of N, the huge number of devices and the corresponding wiring complexity make it unfeasible to implement a fully unary weighted DAC. Therefore, high resolution DACs are typically divided into a segmented structure, consisting of a unary weighted coarse sub-DAC and a binary weighted fine sub-DAC.

4.1.2 Fundamental RF-DAC structure

The term RF-DAC was coined by Luschas et al. [Lus+04]. Their RF-DAC implementation, which modifies the conventional current-steering DAC structure, is shown in Fig. 4.2. A sine wave modulates the tail current source at a frequency f_{LO}. The input of the current-steering pair is therefore not a DC current, but a sinusoidal AC current (plus some DC component needed for biasing). A
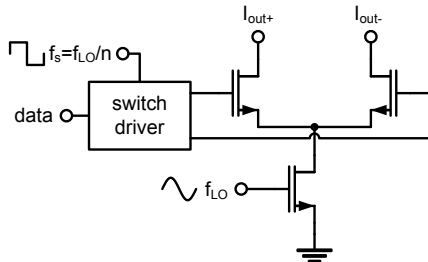
Figure 4.2: One unit element of a the RF-DAC implementation by Luschas et al.

mixing operation is accomplished which upconverts the DAC output signal to LO frequency.

To avoid glitches, switching of the data bits must occur in the zero regions of the oscillation waveform. The switching frequency f_s hence must be aligned to the frequency of the local oscillator (LO). Consequently, the data switching frequency f_s has to be an integer fraction of the LO frequency f_{LO}

$$f_s = \frac{f_{LO}}{n}, \tag{4.1}$$

and also the phase between the data switching and oscillator signals must be aligned.

Fig. 4.2 looks similar to a classical single-balanced mixer implementation, just that the baseband and LO inputs are reversed. In the RF-DAC implementation of Luschas et al. the digital baseband signal path does not include the bottom g_m stage transistor, thereby circumventing potential transconductance linearity problems.

The RF-DAC implementation in Fig. 4.2 has the drawback that it outputs substantial energy at other frequencies than f_{LO}, especially at DC. A double balanced version of the RF-DAC, developed by Eloranta et al. [Elo+07], is shown in Fig. 4.3. This differential RF-DAC was termed "digital-RF converter" (DRFC) by Eloranta et al.[1] The structure of the DRFC is very similar to a Gilbert mixer [Gil68]. The differential structure leads to a rejection of all outputs at DC and the even harmonics of f_{LO}. However, while the Gilbert cell has the baseband inputs at the bottom differential transistors and the LO inputs at the switching quad stacked on top, this is reversed for the DRFC. For a Gilbert cell, the

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[1] Although different names exist for this circuit structure in literature, for consistency reasons subsequently all architectures that combine D/A converter and upconversion mixer in a single building block are called RF-DAC.
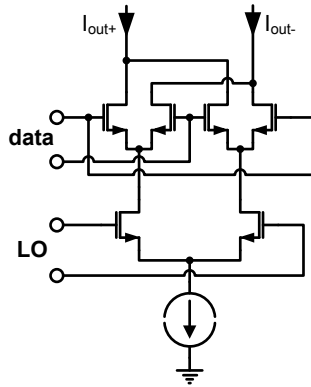
Figure 4.3: One unit element of a the double balanced RF-DAC implementation by Eloranta et al.

transconductance nonlinearity limits the signal dynamic range and generates spurs and harmonic distortion.

For the DRFC, all transistors – besides the constant current source – are operated as switches with no linearity constraints. The output magnitude is controlled by the combination of the output currents of several parallel unit cells. Thus, the linearity of the output signal is defined by the resolution of the converter. As the digital baseband signal is directly brought to the switches of the mixer, it is immune to analog DC-offsets in the baseband signal. Also, I/Q amplitude imbalance that is caused by variations in the transconductance is not an issue as all current sources are equally biased.[2] The LO leakage is hence dominated by direct coupling of the LO signal to the output.

The single- and double-balanced versions of the RF-DAC in Fig. 4.2 and Fig. 4.3, respectively, allow the realization of D/A conversion and upconversion mixing to RF within a single building block. In contrast, for classical direct conversion transmitters as in Fig. 2.1 the current output of a current-steering DAC, which converts digital baseband signals into the analog domain, first has to be converted into a voltage by a transimpedance stage before it can be applied to subsequent analog baseband circuits. After some filtering and additional amplification, this voltage controls the baseband g_m stage input of the upconversion mixer, where it is converted back into a current.

An I/Q modulator which is built out of two quadrature RF-DACs is called

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[2]Still, some imbalance can be caused by mismatch between the current sources of different unit cells.
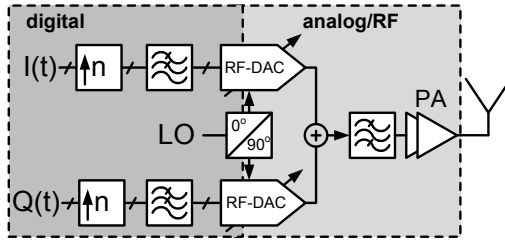
Figure 4.4: Block diagram of a direct-digital I/Q modulator utilizing RF-DACs.

"direct-digital modulator" by Eloranta et al. Fig. 4.4 shows the block diagram of a transmitter based on a direct-digital I/Q modulator which utilizes RF-DACs. As the digital baseband signal is directly applied to the RF-DAC, no analog baseband processing is needed. The VGAs and baseband filters shown in Fig. 2.1 can be removed. These analog blocks are difficult to design as they have strict linearity and I/Q matching constraints, in order to not degrade the signal quality. Also a high dynamic range is needed for the VGAs. For a reconfigurable radio with different communication standards and baseband signal settings, the analog baseband filter must be highly programmable in bandwidth, which is difficult to achieve. The design of these analog blocks gets even harder if they have to be implemented in digital-centric nanoscale CMOS processes. These processes are required to achieve low production costs for the complete system.

While the analog performance of nanoscale CMOS decreases while scaling down the CMOS roadmap, nanoscale CMOS allows high-speed digital baseband signal processing with low power and area consumption. The digital baseband blocks can therefore be made more and more complex. For example digital filters can easily be made configurable. Removing VGAs and especially analog baseband filters leads to a big area and thus cost benefit. Also, for broadband systems, the power consumption of the system can be reduced by removing the analog baseband filtering. This is especially the case for high-data-rate systems, as the power consumption of active analog reconstruction filters is proportional to the signal bandwidth for a constant dynamic range as is shown by Jerng [Jer07, p. 23 f.] and Rezzi et al. [Rez+97].

After replacing the analog baseband blocks by digital counterparts, the RF-DAC is the only remaining analog block in the modulator. As all transistors in the RF-DAC – besides the constant current sources – are operated as high-speed switches without high demands on analog properties of the transistors, it is also perfectly suited for the implementation in nanoscale CMOS.
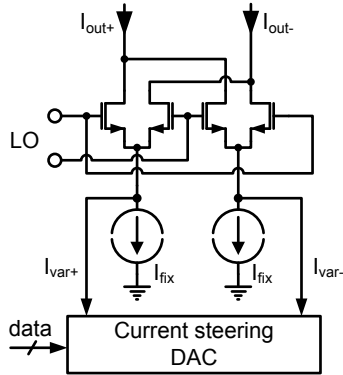
Figure 4.5: RF-DAC architecture by Zhou and Yuan.

4.1.3 RF-DAC implementation by Zhou and Yuan

Zhou and Yuan [ZY03] propose a different RF-DAC structure, which is closer related to a Gilbert cell architecture. The structure is shown in Fig. 4.5. Here, in contrast to a Gilbert cell, the transconductance stage is replaced by two fixed current sources I_{fix}, which are needed for biasing, plus variable currents I_{var}, which are generated by a current steering DAC in dependence of the digital baseband input signal. Compared to a Gilbert cell, this topology does not suffer from linearity degradation through the voltage to current conversion by the transconductance stage. Additionally, this configuration provides more headroom for the modulated RF signal, as its pseudo-differential structure requires only two stacked transistors.

The RF-DAC topologies of Luschas et al. as well as Eloranta et al. use several parallel, weighted unit cells where the output currents are summed at the RF node. In contrast, in the topology of Zhou and Yuan the currents are summed at the IF node preceding the upconversion mixing. Thereby, only one single upconversion mixer is needed.

4.1.4 Digital envelope modulator

Another RF-DAC architecture which modifies the RF-DAC idea by Luschas et al. is proposed by Kavousian et al. [Kav+08] as well as van Zeijl and Collados [vC07]. It is shown in Fig. 4.6. This architecture is even simpler than the implementation by Luschas et al. as the differential current-steering transistor pair is replaced by a single-ended structure with a digitally controlled cascode. The RF input
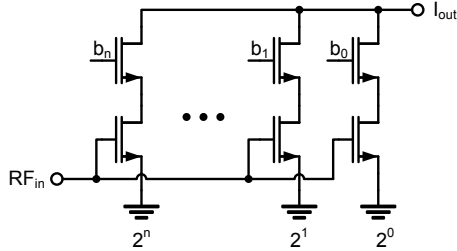
Figure 4.6: Digital envelope modulator DAC [Kav+08; vC07].

signal is applied to the binary weighted bottom transistors. By switching on or off the cascode voltages b_x the output current can be modulated.

This topology is particularly popular for broadband polar modulators. Here, the RF input signal is phase-modulated while the signal envelope magnitude is controlled. Normally, the output signal envelope of polar modulators is controlled by the supply voltage of a class-E switched mode power amplifier, as discussed in section 2.3.2. As the supply voltage must be modulated, the bandwidth of the LDO voltage regulator, which is typically used for this task, limits the total system bandwidth. By using a broadband envelope modulator DAC as in Fig. 4.6 instead of a PA, this limitation can be circumvented. Envelope modulation of 20 MHz bandwidth OFDM WLAN signals could be demonstrated with this structure [Kav+08; vC07].

The envelope modulator DAC has the benefit that it has a very simple structure and that unit cells that are switched off consume no power. On the other hand, switching on and off the cascode transistor is slower than current-steering in a differential structure. Moreover, the differential structure of Luschas et al. suppresses unwanted even harmonics of the LO signal.

4.1.5 Digitally controlled near-class-E PA

Staszewski et al.[Sta+05; Meh+10] propose a digital-to-RF-amplitude converter, as shown in Fig. 4.7, as an amplitude modulator for an all-digital PLL (ADPLL) based polar transmitter. Here, the amplitude signal b_x is multiplied with the phase modulated RF signal in the digital domain, utilizing AND gates. The resulting square wave RF signals control NMOS transistors which act as a "near-class-E PA". Staszewski et al. termed this structure "digitally controlled PA (DPA)".

Pozsgay et al. [Poz+08] use a similar topology for an I/Q modulator. For their implementation, the structure shown in Fig. 4.7 is modified by stacking
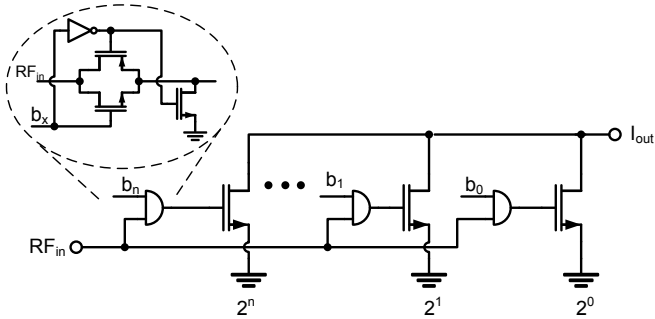
Figure 4.7: Digital-to-RF-amplitude converter, near-class-E DPA [Sta+05].

cascode transistors on top of the switch transistors. By varying the gate voltage of the cascode transistors, additional output power control of the DPA can be achieved.

4.2 Problem of the missing reconstruction filter

Of course, removing the analog baseband filtering does not come for free. In conventional transmitter architectures, the analog baseband filter behind the DAC is utilized as a so-called reconstruction filter to remove the digital signal replicas at multiples of the DAC sampling frequency. Also, it removes some of the DAC quantization noise. The combination of DAC and mixer in a single building block inhibits the application of a reconstruction filter at the DAC output. As the DAC output signal is in the current domain, a lowpass filtering would require inductive elements, making the filter prohibitively large and also very inflexible.

Thus, baseband signal replicas – centered around multiples of the DAC sampling frequency – are also upconverted to RF by the RF-DAC and emitted by the antenna. Some filtering of these alias spectra is achieved by the D/A converter's zero order hold behavior, which constantly holds the value of one sample for one sampling time-step until the next digital word is applied. The zero order hold behavior has a *sinc* frequency response

$$H(f) = \frac{sin(f/f_s)}{f/f_s}, \tag{4.2}$$

where f_s is the sampling frequency of the DAC. The *sinc* response has nulls at multiples of the sampling frequency f_s as shown in Fig. 4.8. Therefore,
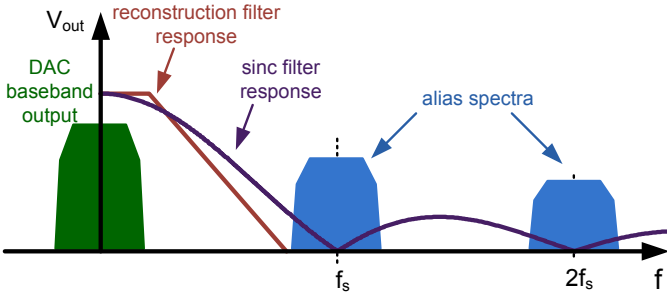
Figure 4.8: Replica spectra at multiples of the DAC sampling frequency and their suppression by an analog reconstruction filter and the first order hold *sinc* frequency response.

narrowband signals around $n \cdot f_s$ are quite effectively suppressed. But it is not sufficient to suppress the replica spectra of broadband modulated signals as well as broadband quantization noise.

4.3 Techniques to reduce unwanted RF-DAC emissions

Several techniques to reduce – or at least influence – the unwanted DAC emissions can be found in literature. They are presented subsequently.

4.3.1 Bandpass filtering

As the RF-DAC does not allow reconstruction filtering at baseband, filtering can only be done utilizing a bandpass filter at the RF output of the converter. Unfortunately, it is difficult to implement narrowband bandpass filters, especially if cost is an important factor.

Jerng [Jer07] uses a fourth order Bessel LC bandpass filter with active quality factor enhancement for his RF-DAC implementation. Thereby, a 210 MHz 3 dB bandwidth at 5.25 GHz center frequency is achieved, translating to a quality factor Q of 25. To achieve a broader frequency range at which the transmitter can be operated, tunable LC-tanks that utilize varactors are employed. Thereby, the center frequency can be tuned from 4.8 GHz to 5.4 GHz.

To improve the bandpass filtering effect, a high DAC oversampling rate should be chosen in order to move the DAC alias spectra far away from the bandpass center frequency, where the filtering is sufficiently high.

It must be noted that high-Q bandpass filtering is only possible when the RF-DAC output is connected to a high-impedance node, like an output buffer.

In this case, an analog, linear on-chip amplifier is still required. If, on the other hand, the RF_{out} node is directly connected to an off-chip component like an external power amplifier, the overall quality factor is limited by the $50\,\Omega$ system impedance that acts as a shunt resistance to the LC tank. Thereby, the Q and thus the effectiveness of the bandpass filter is reduced. Consequently, Eloranta and Seppinen [ES05] use an LC tank at the output node mainly as an output matching circuit. Their LC tank is designed to have an especially low quality factor as to allow wideband operation from $100\,\text{MHz}$ to $2.6\,\text{GHz}$.

4.3.2 Influence of DAC resolution and oversampling

In addition to the signal replicas at multiples of the sampling frequency, the DAC also emits unwanted broadband quantization noise. Quantization noise for most practical purposes can be assumed to be uniformly distributed. Thus, a constant "noise floor" is perceived when measuring the quantization noise density vs. frequency. The overall quantization noise obviously decreases with an increase in converter resolution.

The maximum signal to noise ratio (SNR) of a DAC operated at Nyquist rate for a sinusoidal input signal can be expressed as [Pla03, p. 9ff.]

$$\text{SNR}_{max} = \frac{2^N \sqrt{6}}{2} \tag{4.3}$$

where N is the number of bits of the converter. Often, the SNR is given in terms of decibels (dB). Rewriting equation (4.3) in dB yields

$$\text{SNR}_{max} = 20 \log_{10} \frac{2^N \cdot \sqrt{6}}{2} = 6.02N\,\text{dB} + 1.76\,\text{dB}. \tag{4.4}$$

Hence, the quantization noise drops by approximately $6\,\text{dB}$ for every additional bit of resolution. It must be noted, however, that the effective resolution of a converter is limited by nonlinearities and matching of the analog components. An *effective number of bits* (ENOB) of a Nyquist rate converter can be defined from an actual measured SNR by rearranging equation (4.4) [AH02, p. 617]

$$\text{ENOB} = \frac{\text{SNR}_{actual} - 1.76\,\text{dB}}{6.02\,\text{dB}}. \tag{4.5}$$

Sampling at a higher frequency than the Nyquist frequency is called "oversampling". By increasing the sampling rate, the quantization noise is randomized over a larger frequency band. Thus, the quantization noise in the signal frequency band decreases accordingly. This can be written as [Pla03]

$$\text{SNR}_{max} = 2^{n-1} \sqrt{3} \sqrt{\frac{f_s}{f_{sig}}} \tag{4.6}$$
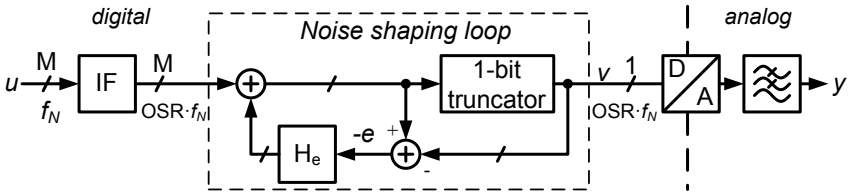
Figure 4.9: Block diagram of a single-bit $\Delta\Sigma$ DAC.

or in decibels

$$\text{SNR}_{max} = 6.02N\,\text{dB} - 1.25\,\text{dB} + 10\log_{10}\left(\frac{f_s}{f_{sig}}\right) \tag{4.7}$$

where f_s is the sampling frequency and f_{sig} is the signal bandwidth.

Thus, the SNR can be can be improved by 6 dB and the corresponding ENOB by 1 bit when increasing the sampling rate by a factor of 4. Differently said, the quantization noise floor drops by 6 dB by either increasing the resolution by one bit or by increasing the sampling rate by a factor of 4. Oversampling converters are able to achieve a high ENOB resolution and thus SNR, even if the amplitude resolution of the converter is limited by analog non-idealities.

4.3.3 $\Delta\Sigma$ modulation

$\Delta\Sigma$ modulators ($\Delta\Sigma$M) are a special type of oversampling converters. While conventional oversampling DACs emit truncation noise which is equally distributed over frequency, $\Delta\Sigma$M DACs do *noise shaping*. Thereby, large amounts of the quantization noise energy are shifted to high frequencies, far away from the signal band. Thus, the SNR in the signal band can be very high, even if the converter has a low number of actual bits. The unwanted truncation noise can be removed with an analog low-pass filter after the DAC.

Fig. 4.9 shows the block diagram of a $\Delta\Sigma$ DAC [ST04]. The input signal u at a data rate near the Nyquist frequency f_N is first upsampled to a higher frequency by an interpolation filter (IF) to allow subsequent noise shaping and suppress replicas of the input signal at multiples of the sampling frequency f_N.

Noise shaping is done by a feedback loop. The loop truncates the word-length M of the input signal to a smaller number of bits. Thereby, the resolution of the subsequent DAC can be reduced considerably. The truncation error e is filtered with the transfer function H_e and fed back and subtracted from the input signal. The name $\Delta\Sigma$ originates from the subtraction block at the input and the summation in the loop filter.

The output $V(z)$ of the noise shaping loop is given by

$$V(z) = U(z) + [1 - H_e(z)]\, E(z). \qquad (4.8)$$

Thus, the signal transfer function (STF) of the noise shaping loop is 1, while the noise transfer function (NTF) is $1 - H_e(z)$. The filter response $H_e(z)$ defines the noise shaping of the loop. The simplest filter implementation which can be used is a delay $H_e(z) = z^{-1}$, resulting in an NTF of $1 - z^{-1}$ which is a first order high-pass. Higher order feedback loops with a higher noise suppression near DC can be designed by concatenating several feedback stages. In the frequency domain, the NTF of a $\Delta\Sigma$M of order M is given by [ST04]

$$\left| NTF_M(e^{(j2\pi f)}) \right| = (2 sin\,(\pi f))^M$$
$$\approx (2\pi f)^M, \text{for} f << 1. \qquad (4.9)$$

The magnitude of the NTF of different $\Delta\Sigma$Ms is plotted versus frequency in Fig. 4.10 on a double logarithmic scale. The NTFs for three different modulator orders are shown. For this plot, the frequency axis is normalized to the sampling frequency f_s of the $\Delta\Sigma$M. As can be seen, the noise suppression at low frequencies is much better for higher order $\Delta\Sigma$Ms. The noise beyond a frequency of $f_s/(2\pi)$, however, is larger for higher order modulators because of the stronger noise shaping. The total emitted noise is the same for all modulator orders, as it is determined by the resolution of the subsequent DAC. Only the effectiveness of the noise shaping is different. For $\Delta\Sigma$M orders larger than 3, feedback loop stability can get a severe issue and therefore must be carefully examined [ST04, p. 97ff.].

As depicted in Fig. 4.9 $\Delta\Sigma$ DACs often have a single-bit output, especially for narrowband applications where a high OSR is feasible, like audio or sensor applications. The single-bit topology is quite popular as the implementation of a two-level DAC output is very simple. Furthermore, a single digital bit can be converted perfectly linear into an analog output. However, the single-bit DAC has a high slew rate and emits a large amount of out-of-band noise which requires a high quality filter at the DAC output.

Multi-bit DACs lower the requirements on the analog reconstruction filter but on the other hand need more complex circuitry. The decision on the total number of bits is usually a trade-off between required SNR, feasible OSR, complexity, linearity, chip area and overall power consumption.

The previously discussed $\Delta\Sigma$Ms have all wanted signal energy within a narrow band near DC. Therefore, they are called lowpass $\Delta\Sigma$Ms. For RF communications systems, especially for low-IF receivers, another $\Delta\Sigma$M architecture, the bandpass $\Delta\Sigma$M, is often used [Hen+02; Kim+07]. Here, the signal is not located at DC, but in a narrow band of bandwidth f_B around a center frequency f_0. As the SNR should be maximized in the signal band, the NTF consequently must have
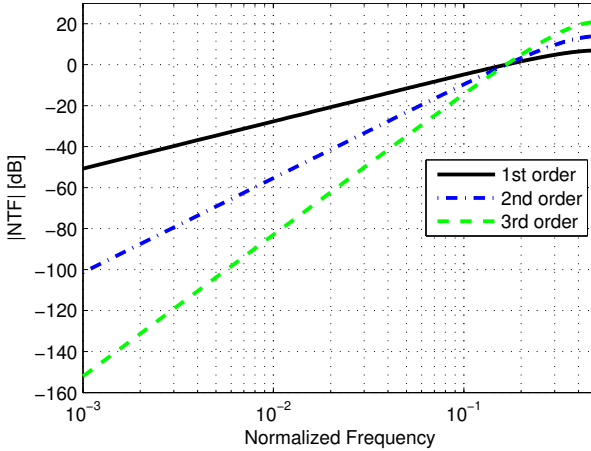
Figure 4.10: $\Delta\Sigma$M NTF over normalized frequency in dependence of the modulator order.

a bandstop characteristic with zeros around f_0. Bandpass NTFs can be derived from an equivalent lowpass NTF by a so-called N-path transformation [ST04, p. 145ff.].

Single-bit $\Delta\Sigma$ modulators in RF-transmitters

Recently, the utilization of single bit $\Delta\Sigma$Ms in RF transmitters has got an increasingly popular research topic. A single-bit digital output allows to directly use a switching-mode PA as DAC with high power output, making the transmitter especially simple and due to the utilization of a switching-mode PA potentially energy efficient. Single-bit $\Delta\Sigma$M transmitters use either a low-pass $\Delta\Sigma$M with subsequent digital upconversion mixer [Fra+09; Hel+08], or directly generate a $\Delta\Sigma$ modulated RF signal, using a bandpass $\Delta\Sigma$M [Som+04]. However, the PA must be switched at several times the frequency of the RF carrier to achieve a reasonable OSR. Also, the digital signal processing must run at these high frequencies. This is hardly feasible with today's technology, especially if power consumption is a limiting factor. The combination of a low OSR and a single-bit DAC limits the achievable SNR. The required high-quality bandpass filters at the RF output that are needed to suppress the unwanted truncation noise are bulky and very expensive. Therefore, single-bit $\Delta\Sigma$M transmitters probably will not get a commercially attractive alternative architecture in the near future, especially for mobile devices. Furthermore, as a large amount of the transmitted
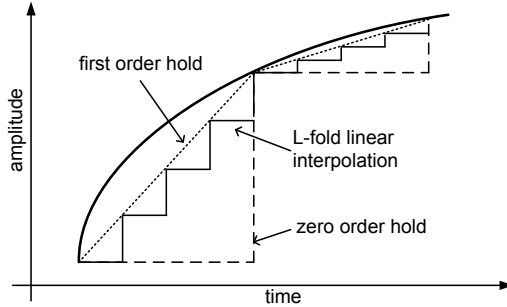
Figure 4.11: Principle of L-fold interpolation.

power is truncation noise which has to be removed by a filter, the overall energy efficiency of the system drops drastically, although it may incorporate a very efficient switching-mode PA.

4.3.4 L-fold interpolation

Instead of using a high oversampling ratio, the DAC's output signal approximation of the original signal could be improved if the DAC would not simply hold an output value until the next sample, but interpolate between concurrent samples. If the zero-order behavior of the DAC would be replaced by linear interpolation, it had a $sinc^2$ frequency response instead of a $sinc$ response. Such a first order hold behavior would much better suppress the DAC signal replica. Anyhow, the implementation of a linear interpolation DAC output is not trivial.

A technique which can be used as a simpler alternative to linear interpolation is L-fold interpolation. L-fold interpolation is a staircase approximation to linear approximation, which can more easily be implemented. The working principle of L-fold interpolation is shown in Fig. 4.11. Instead of a large step change at the sampling instances, L smaller steps are generated by sequentially activating L sub-DAC cells to approximate linear interpolation. Zhou and Yuan [ZY03] implemented a 16-tap (L=16) interpolation DAC. Thereby, the achieved frequency response is very close to the $sinc^2$ function. The required hardware effort, however, is quite large, as 16 times the number of (accordingly smaller) DAC unit cells is needed. In addition, 16 delayed clock signals have to be generated. In the implementation of Zhou and Yuan voltage controlled delay lines are used for this task.

Kavousian et al. [Kav+07] use a 4-fold linear interpolation, which can be implemented much simpler than 16-fold interpolation. Instead of using voltage

controlled delay lines, simple frequency dividers can be utilized to generate the needed quadrature clock signals.

4.3.5 Semidigital FIR filter

Another technique to suppress unwanted emissions is embedding a semi-digital finite impulse response (FIR) reconstruction filter in the digital-RF interface. Taleie et al. [Tal+08] use the 1-bit output of a $\Delta\Sigma$M whose output goes through a 6-tap digital delay line. Each output of the delay line is applied to the input of an RF-DAC. The current source of each RF-DAC unit cell is weighted with the appropriate FIR filter coefficient.

To achieve a reasonable attenuation, however, this technique needs a large number of filter taps. For example, Su and Wooley [SW93] need a 128-tap delay line to realize an attenuation which is comparable to a second order analog filter. This of course leads to high power consumption for high RF output frequencies and broadband signals with high sampling rates.

Pozsgay et al. [Poz+08] use a transmitter implementation with two multi-bit RF-DACs. The second RF-DAC is time-shifted against the first by a digital delay. Thereby, "notches" in the emitted noise floor can be generated.

4.4 Performance summary of published "all-digital" transmitter implementations

In this chapter an introduction to the idea of the RF-DAC has been given and different RF-DAC implementations that can be found in literature have been presented. Also, the problem of unwanted emissions caused by the missing analog reconstruction filter has been discussed and different techniques to reduce these unwanted emissions have been presented.

A performance summary of the different, earlier published "all-digital" transmitters that have been discussed in this chapter is given in table 4.1.

System	[Lus+04]	[Tal+08]	[Elo+07]	[Jer07]	[ZY03]	[Fra+09]	[Kav+08]
DAC structure	3 bit unary RF-DAC	1 bit, 6 tap FIR	10 bit DRFC	3 bit DRFC	10 bit	1 bit	polar, 6 bit envelope
$\Delta\Sigma M$	off-chip	4th order BP	-	2nd order MASH LP	-	3rd order LP	-
$f_{carrier}$ [GHz]	0.942	1.062	1.9	5.25	1	1	1.56
f_{sample} [MHz]	514	250	307.2	2600	50	4000	640
Bandwidth	-	-	20 MHz	200 MHz	3.3 MHz	50 MHz	20 MHz
max. P_{out}	-	-5 dBm	1.8 dBm	-8 dBm	-6.5 dBm	3.1 dBm	13.6 dBm
power consumption DAC [mW]	20	12.5	37.5	10	-	39	-
power consumption analog [mW]	NA	122	60.5	87	159.8	120	145
Supply [V]	1.8	2.5	1.2	2.5	3.3	1	1.7
Analog area [mm^2]	-	0.23	1	0.72	0.35	0.15	1.8
CMOS Process	180 nm	250 nm	130 nm	130 nm	350 nm	90 nm	180 nm
Specialty			90dB power control		16 fold interpolation	digital up-conversion	4 fold interpolation

Table 4.1: Performance summary of different earlier published direct-digital transmitters.

5 RF-DAC Transmitter System Requirements

Before the circuit implementation of the RF-DAC transmitter can be started, the system requirements, depending on the targeted communications system, have to be defined. A suitable transmitter architecture has to be found and specific requirements for the main building-blocks have to be derived from the overall system specifications.

System simulations allow to estimate the influence of different parameter and architectural choices on the overall system performance. All system simulations for this thesis have been conducted utilizing Matlab®.

5.1 Supported standards and performance requirements

The RF-DAC based transmitter should be compatible with high-data-rate, broadband communication standards such as WLAN IEEE 802.11 or 3GPP LTE. At the same time also other communication standards such as GSM, WCDMA or Bluetooth (BT) with lower data rates and bandwidths should be supported. Most modern high-data-rate communication standards are based on OFDM signal processing, as explained in chapter 2.4. Therefore, the transmitter frontend should be suited for the OFDM signal requirements, e.g. have an adequate linearity and sufficient dynamic range to support high peak-to-average power ratios. The supported signal bandwidth should be at least 20 MHz, which is the typical maximum bandwidth of LTE and WLAN signals. The most important signal characteristics of the LTE and WLAN IEEE 802.11n standards are summarized in table 2.1.

5.1.1 Supported frequency bands

Although a lot of different frequency bands are specified for the cellular standards, all existing GSM and WCDMA nets operate at frequencies below 2 GHz. The frequency bands for connectivity devices (WLAN and BT) are the ISM (industrial, scientific, medical) bands around 2.4 GHz and 5.8 GHz. The ISM band at 2.4 GHz is, however, much more popular than the 5.8 GHz band, because of the better propagation characteristics of the electromagnetic waves. Additionally, the required implementation effort and thus cost for the devices is reduced for lower frequencies.

For the 3GPP LTE communication standard, a lot of different frequency bands are specified. However, not all frequency bands are equally attractive, as they for example differ in available bandwidth, wave propagation characteristics, FDD duplex gap distance etc. Furthermore, not all of the bands are unoccupied in every country.

The first frequency bands that will be used (at least in Germany) are a frequency band around 800 MHz – which was previously used for analog television broadcast – as well as formerly unused frequency bands at around 2.6 GHz. LTE band VII is a frequency band with frequency division duplex (FDD) operation with uplink (from the mobile device to the base station) frequencies from 2500 to 2570 MHz and downlink (from the basestation to the mobile device) frequencies from 2620 to 2690 MHz. Interestingly, another frequency band (band 38) is planned with time division duplex (TDD) operation within the 50 MHz wide duplex gap of band VII.

In summary, it can be said that a transmitter that allows the operation at frequencies up to 2620 MHz may cover all relevant frequency bands for cellular and connectivity wireless communication standards.

5.1.2 Output power considerations

The maximum peak output power of mobile telecommunication devices for GSM, UMTS, and LTE is in the range of +33 dBm. These high output power levels can neither be achieved with a CMOS RF modulator directly nor with an RF modulator plus on-chip CMOS PA, as discussed in chapter 3. Therefore, an external PA is needed. Still, the output power of the RF-DAC should be as high as possible. An output power level in the range of +15 dBm would permit relatively simple, external PAs. A low required PA power gain allows the implementation of the PA with a low number of amplifier stages, lowering the off-chip component costs and improving the power added efficiency (PAE) of the PA. When the transmitter is operated in backoff at power levels much below the peak output power – where e.g. WCDMA devices are operated for most of the time – the PA could even be bypassed and switched off, to maximize power efficiency. For some connectivity devices with lower required maximum output power such as BT and WLAN an external PA could be waived completely.

On the other hand, for the circuit implementation of the transmitter it is important to note that a trade-off between output power and linearity of the RF-DAC exists. A high output power requires large currents in the RF-DAC and hence transistors with a large aspect ratio. This, however, reduces the output impedance of the RF-DAC and hence linearity.
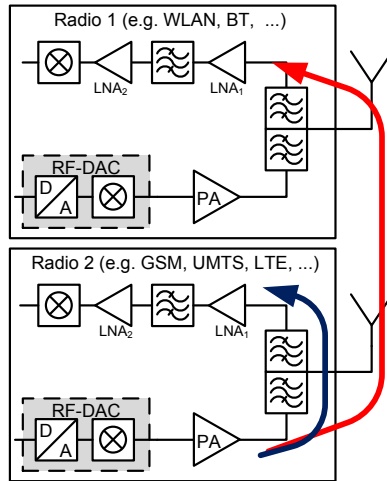
Figure 5.1: Scenario of two parallel running radios on the same mobile device. The transmit signal of radio 2 may disturb its own receiver, if it is running in FDD mode. Also, the receiver of the concurrently running radio 1 may be disturbed.

5.2 Determination of the upper limit for the unwanted emissions and calculation of the spectral mask

Most communication standards define maximum spurious emissions. Still, these emission limits may not be strict enough if there are several transceivers within the same mobile device, in close proximity, and running at the same time. Neighboring receivers shall not be disturbed by the transmitter's spurious emissions. For example, a smartphone user could want to place a phone call via a cellular standard like GSM, while he is downloading data via WLAN. The strong GSM signal must not disturb the WLAN receiver. Such a scenario with two concurrently running radios is depicted in Fig. 5.1. The running transmitter of radio 2 could either disturb the receiver of radio 1. Also, the transmitter of radio 2 could disturb its own receiver, if these are not properly isolated from each other.

Two effects can lead to a disturbance of a receiver. First, the strong transmit signal could act as an out-of-band blocker for the receiver, which is running at another frequency, driving the low noise amplifier (LNA) into compression. Band-select filters at the receiver input, however, should normally be capable of suppressing these blocking signals sufficiently. Still, chip and PCB layout have to

be done with great care to circumvent a parasitic coupling from the transmitter output directly to the LNA input, bypassing the band-select filters.

The second effect is that the transmitter could emit additional noise at other frequencies than its wanted frequency. Unwanted emissions within the receive band frequencies act as noise for the receiver, which adds up to the normally dominant thermal noise floor. Thereby, the signal-to-noise ratio at the receiver input is degraded.

Unwanted emissions are especially critical for full-duplex FDD system such as WCDMA or LTE, where the receiver is running at the same time but at another frequency as the transmitter of the same radio. The frequency spacing – the so-called duplex gap – of transmit and receive bands is typically some tens of MHz. As receiver and transmitter mostly share a common antenna, a SAW duplex filter with very high selectivity is needed to suppress unwanted emissions of the transmitter at receive frequencies.

For half-duplex TDD systems such as GSM and WLAN, receiver and transmitter run at the same frequency but at different time slots. Thereby, the transmitter can not disturb its own receiver. Anyhow, the transmitter of such a system could still disturb a simultaneously running receiver of another radio on the same device.

The communication standard's transmit specifications give valid adjacent channel and general far-off spurious emission limits. But for the receive bands of radios on the same mobile device a stricter spectral mask than the one defined by the communication standard must be used.

To estimate how big the maximum additional emitted noise in the receive bands may be, it is assumed that the receiver input sensitivity should not be degraded by more than $1\,\mathrm{dB}$, to sustain a low bit error rate. The thermal noise P_N, normalized to a bandwidth of $1\,\mathrm{Hz}$, at room temperature ($T_0 = 290\,\mathrm{K}$) is

$$P_N = k_B \cdot T_0 = 1.38 \cdot 10^{-23}\,\mathrm{J/K} \cdot 290\,\mathrm{K}$$
$$= 4 \cdot 10^{-18}\,\mathrm{mW/Hz} = -174\,\mathrm{dBm/Hz}, \tag{5.1}$$

where k_B is the Boltzmann constant.

Thus, the overall noise at the receiver input may not exceed $P_N + 1\,\mathrm{dB} = -173\,\mathrm{dBm/Hz}$. To achieve this, the additional spurious emissions at the receiver input $P_{spur_{rx}}$ must be limited to

$$P_{spur_{rx}} = 10 \cdot \log_{10}\left(10^{\frac{-173}{10}} - 10^{\frac{-174}{10}}\right)\frac{\mathrm{dBm}}{\mathrm{Hz}} = -179.8\,\frac{\mathrm{dBm}}{\mathrm{Hz}}.$$

Thus, if we restrict the receiver sensitivity degradation to $1\,\mathrm{dB}$ the additional noise must be at least a factor of four lower than the thermal noise floor!

On their way to the receiver input, transmitted spurious emissions are damped by the transmitter's (duplex) SAW filter (L_{SAW}), the receiver's band-select

input filter (L_{ins}) insertion loss, and – as far as transmitter and receiver do not have a shared antenna – the limited coupling between the transmit and receive antenna (L_{ant}). Therefore, the maximal allowed unwanted emissions at the transmitter output $P_{spur_{Tx}}$ can be written as

$$P_{spur_{Tx}}(f) = P_{spur_{Rx}}(f) + L_{SAW}(f) + L_{ins}(f) + L_{ant}(f). \qquad (5.2)$$

Especially the damping of SAW filters is very frequency dependent. UMTS and LTE duplex filters are optimized for the duplex frequency spacing, typically achieving around 45 to 50 dB isolation in this frequency region. At other frequencies more than 25 dB Tx to antenna attenuation are typically obtained [EPC07]. The insertion loss L_{ins} of a SAW filter is typically below 2 dB. Measurements on mobile phone patch antennas conducted in the lab revealed that a minimum isolation L_{ant} of 20 dB between two antennas in close proximity can be expected [Arl09]. If placed more optimal within the phone, an isolation of 30 to 40 dB is realistic [Kis09].

The maximally allowed unwanted emissions were calculated for frequency bands where radios are operated simultaneously and independently, such as WLAN, Bluetooth, GPS, and GSM. Especially critical are the receive bands of FDD systems like UMTS or LTE. The maximum allowed spurious emissions at the transmitter output are between -130 and -120 dBm/Hz depending on the frequency band. In Fig. 5.16(a) the resulting spectral mask for an LTE transmitter operating in the 2.5 GHz band is shown.

5.3 Matlab system simulations

The transmitter system, consisting of digital signal generation and modulation, digital signal processing, "direct digital modulator", as well as the mixed-signal and RF components, has been modeled with Matlab® to enable system simulations on a high abstraction level. For the RF blocks, equivalent baseband models have been used to increase the simulation speed. Nonlinearities of the transmitter have been characterized by a simple Saleh model [Jer+00, p. 218 ff.]. This kind of model characterizes consequences of nonlinearities on both amplitude (AM/AM conversion) and phase (AM/PM conversion). Also, some signal post-processing has been implemented to evaluate the quality of the simulated RF-DAC output signal, e.g. to plot the output spectrum and spectral masks or calculate the error vector magnitude (EVM).

Several simulations to determine spectrum allocation and figures-of-merit like EVM have been carried out for different standards such as WLAN and LTE, for different bandwidth settings, carrier frequencies, and modulation schemes.

The calculations of the above discussed unwanted emission limits have been conducted with Microsoft Excel® and imported into Matlab to plot the resulting spectral masks for the respective communication standard and frequency band.
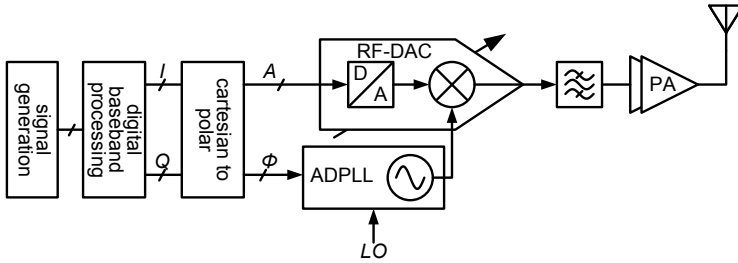
Figure 5.2: Possible implementation of a polar modulator comprising an RF-DAC and an all-digital PLL.

5.4 Transmitter topology choice

The transmitter topology has to be suited for the RF-DAC requirements and the broadband OFDM signal needs. The typical transmitter architecture choice for broadband signals is a quadrature direct-conversion transmitter, as shown in Fig. 2.1 for a conventional analog transmitter and in Fig. 4.4 for a direct-digital RF-DAC based transmitter.

5.4.1 IQ vector modulator vs. polar modulator

Alternatively to an I/Q modulator, a (small signal) polar modulator could be used, consisting of an RF-DAC for amplitude modulation and an all-digital PLL [Sta+05] to control the phase of the LO. The block diagram of such a polar transmitter is shown in Fig. 5.2. Using the CORDIC algorithm or a look-up table (LUT), the digital baseband Cartesian I/Q signal can be converted to a polar amplitude $A(t)$ and phase $\phi(t)$ signal, according to

$$A(t) = \sqrt{I(t)^2 + Q(t)^2} \tag{5.3}$$

$$\phi(t) = \arctan\left(\frac{Q(t)}{I(t)}\right). \tag{5.4}$$

The Cartesian and polar methods of generating a quadrature signal are illustrated in Fig. 5.3 for a QAM 16 constellation.

A polar architecture would eliminate one of the two RF-DACs that are needed for a Cartesian signal generation, hence saving chip area. Also, the average power consumption can be lowered as the current which is needed to generate the amplitude signal A is obviously smaller than the sum of the I and Q currents, as can be seen in Fig. 5.3. Simple arithmetic reveals that for a 16 QAM modulation
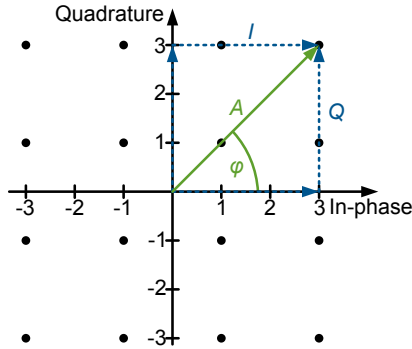
Figure 5.3: Principle of the quadrature signal generation in a Cartesian vs. polar methodology.

the Cartesian signal generation needs a factor of 1.37 higher current.[1] This factor reduces to 1.35 for a 64 QAM modulation scheme.

Nevertheless, system simulations show that the polar modulator configuration has several drawbacks. The bandwidth of the decomposed magnitude and phase signals is much higher than of the I/Q signals. The 60 dB bandwidth of an WLAN IEEE 802.11a/g/n OFDM baseband signal like shown in Fig. 2.12 is about 16.6 MHz. The bandwidth of the amplitude path in the polar modulator is increased to almost 40 MHz by the nonlinear transformation of (5.3) as can be seen in Fig. 5.4(a). This poses high challenges for the amplitude modulator. Typically, polar architectures have a signal bandwidth in the Kilohertz to Megahertz range and thus are mainly utilized for GSM and EDGE applications [Sta+05; Sow+04; RS05]. Recently, Kavousian et al. [Kav+08] as well as van Zeijl and Collados [vC07] showed that it is feasible to build 20 MHz envelope modulators for polar WLAN transmitters, utilizing a circuit structure which is similar to an RF-DAC. Thereby, high bandwidth amplitude modulation with a polar modulator is made possible (see also section 4.1.4). Still, an integrated PLL is not included in their prototypes.

Even if a structure similar to an RF-DAC permits amplitude modulated signals with a high bandwidth, the bandlimited phase path still limits the overall polar modulator performance. All-digital PLLs with two-point-modulation as presented in [Sta+05] and [Ney10] theoretically have a very high bandwidth.

---

[1]It is assumed that every symbol in the constellation diagram has the same probability of occurrence. Also, for the calculations it is neglected that the signal is moving constantly on a trajectory. Rather, the signal is only examined at the QAM constellation points at discrete sampling times.

(a) Magnitude component

(b) Instantaneous frequency component
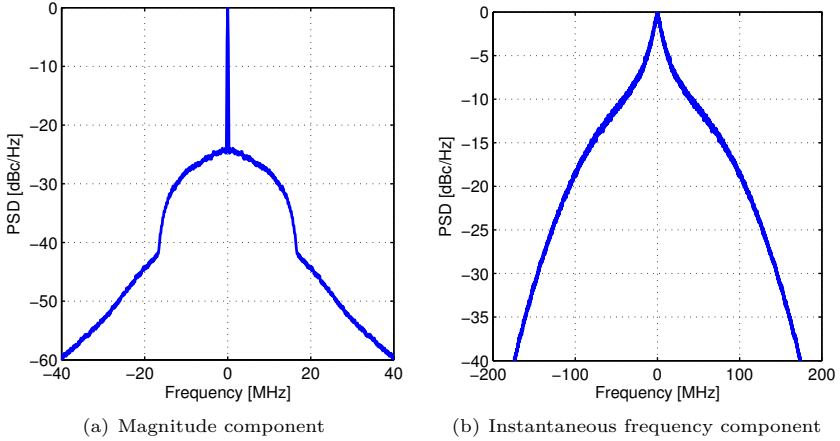
Figure 5.4: 20 MHz WLAN 802.11 OFDM signal, decomposed into magnitude
and instantaneous frequency (derivative of the phase) parts.

However, the tuning range of the voltage-controlled oscillator (VCO) is limited.
Staszewski et al. [Sta+05] report a tuning range which is 22.2% of the VCO
center frequency (± 400 MHz tuning range around 3.6 GHz). The available VCO
frequency tuning range $\Delta f_{VCO} = f_{VCO,max} - f_{VCO,min}$ is utilized for tuning
the carrier frequency as well as for modulating the phase. After subtracting
the needed carrier frequency tuning range $\Delta f_{car} = f_{car,max} - f_{car,min}$ from
the overall VCO tuning range Δf_{VCO} only a limited VCO tuning margin
$\Delta f_{margin} = \Delta f_{VCO} - \Delta f_{car}$ is left. Thereby, the maximum phase change rate
is limited. A fast change of the phase $\phi(t)$ demands a large change of the
instantaneous frequency $f(t)$, which is the derivative of the phase:

$$f(t) = \frac{1}{2\pi} \frac{d}{dt} \phi(t). \tag{5.5}$$

Fig. 5.4(b) shows a plot of the needed $f(t)$ bandwidth for a 20MHz WLAN
802.11g signal. The spectrum of the corresponding WLAN baseband signal
is shown in Fig. 2.12. It can be seen that the required bandwidth of the
instantaneous frequency is extremely high. A VCO tuning margin which is
similarly high is required. Normally, the phase change rate is restricted by the
limited VCO tuning margin. This is an effect which is somewhat similar to
the slew-rate of an amplifier. If, in the system simulation, the tuning range
margin Δf_{margin} is limited to ± 80 MHz , this leads to a distortion of the phase
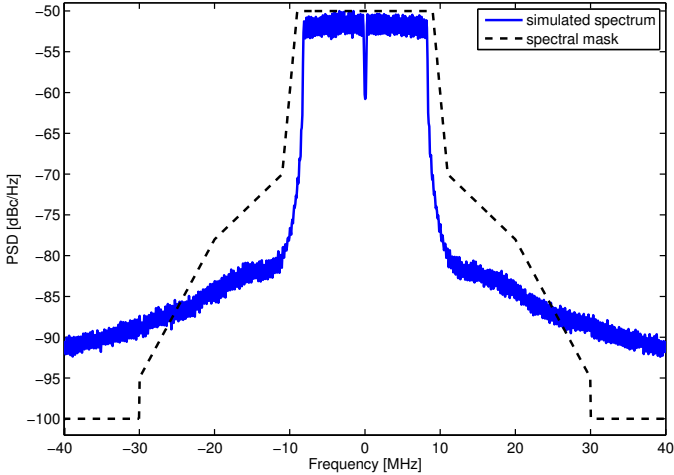
Figure 5.5: Output signal of the polar modulator with limited PLL tuning range.

modulated signal. As a result, the output signal of the polar modulator has high sidelobes, exceeding the spectral mask, as shown in Fig. 5.5. Also the signal quality (measured as EVM) is impaired by the limited phase bandwidth. In the simulation the EVM increases by about 4%.

To circumvent the limited modulation bandwidth of the PLL in Fig 5.2 it could be replaced by a solution where only the fixed carrier signal is generated with a PLL. The phase signal could be modulated on the carrier utilizing a quadrature mixer and afterwards limiting the magnitude of the modulated signal, similarly to the polar modulator in Fig. 2.6. Anyhow, this means a lot of additional effort and current consumption for the mixers and limiter, relinquishing the power efficiency benefits of the polar modulator architecture. Also, the noise performance of this topology is inferior to the previously discussed solution which utilizes a two-point modulated PLL. In the latter solution the PLL's bandpass characteristic filters large portions of the noise in the phase path. In the former solution not only the filtering is weaker. Also, the mixer generates additional upconverter noise.

Furthermore, the polar modulator is very sensitive to timing mismatches between amplitude and phase path. Such a delay will cause a misalignment when magnitude and phase signals are recombined. In the system simulation, a delay in the range of some nanoseconds (which is approximately one tenth of a percent of a OFDM signal symbol length) has a similar effect on the output
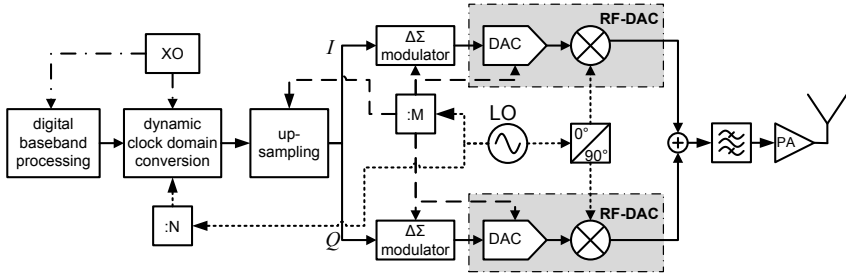
Figure 5.6: Simplified block diagram of the proposed RF-DAC transmitter, based on an I/Q vector modulator.

signal as limiting the PLL bandwidth. Of course, the relative mismatch between magnitude and phase path is also more severe for high-data-rate signals.

5.4.2 Overview of the chosen transmitter topology

As the RF-DAC based transmitter should be compatible with broadband signals – which is not feasible with a polar modulator as discussed above – a direct-digital I/Q modulator architecture as shown in Fig. 4.4 has been chosen.

A simplified block diagram of the RF-DAC quadrature modulator transmitter is shown in Fig. 5.6 [Zim+09b]. On the left hand side of the figure the digital baseband signal processing is shown. The clock frequency for the digital baseband blocks depends on the requirements of the baseband signal. It must be at least twice the signal bandwidth to fulfill the Nyquist criterion. Normally, the baseband signal is oversampled to a multiple of the Nyquist frequency. For OFDM-based signals the clock frequency must be an integer multiple of the subcarrier frequency f_{subcar}. For example, for WLAN signals with a subcarrier spacing of 312.5 kHz and a bandwidth of 20 MHz the typical baseband sampling rate is 80 MHz.

The RF-DAC clock frequency on the other hand must be a fraction of the RF carrier frequency to avoid glitches, as explained in chapter 4. Hence, the data must be transferred from the crystal oscillator (XO) derived clock domain to the LO-derived clock domain. As the LO frequency f_{LO} changes with channel-frequency, this clock domain conversion must be adjustable. Reconfigurable interpolation filters are required. The clock domain conversion should be done as early as possible in the signal processing chain, where the sampling rates are still comparatively low.

The main concern for the implementation of the RF-DAC transmitter are unwanted emissions, which can be divided into the DAC's image spectra at

multiples of the sampling frequency as well as broadband quantization noise generated by the D/A conversion. Possible techniques to reduce these unwanted emissions – including high signal oversampling ratios, high DAC resolution, $\Delta\Sigma$ modulation, bandpass filtering at the RF output, L-fold interpolation, and semidigital FIR filters – have been discussed in section 4.3.

For the chosen transmitter architecture of Fig. 5.6, to reduce the requirements on the DAC resolution a low-pass multi-bit $\Delta\Sigma$ modulator is used. Thereby, the quantization noise is shaped to frequencies where the LC bandpass filter has higher selectivity. At the same time, the noise within and close to the signal band is minimized. To obtain a good noise shaping performance, the signal has to be highly oversampled. As pointed out in section 4.3.3 and shown if Fig. 4.10 the output noise of a $\Delta\Sigma$ modulator beyond a frequency of $f_s/(2\pi)$ is even higher compared to the noisefloor without noise shaping. Therefore, f_s must be sufficiently high to allow a bandpass filtering of the noise. This is achieved by an upsampling filter preceding the $\Delta\Sigma$ modulator. Due to the oversampling not only the quantization noise is reduced but also the DAC signal replica are moved to frequencies which are farther away from the carrier frequency.

The power of the emitted quantization noise scales with the resolution of the RF-DAC. The quantization noise decreases by approximately 6 dB for every additional bit of resolution, as shown in section 4.3.2. Besides, the DAC resolution has to be high enough to achieve a good linearity and thus signal quality of QAM signals with high order modulation. The influence of the DAC resolution on the EVM measure can be evaluated with Matlab system simulations.

5.5 Architecture of the digital blocks

Subsequently, the architecture and implementation considerations for the main digital signal processing blocks, namely dynamic clock domain conversion, upsampling, $\Delta\Sigma$ modulation, and DAC mismatch shaper are briefly discussed. Within the framework of this thesis only system aspects of the digital signal processing blocks have been considered. The implementation of the corresponding circuits has not been part of this work.

5.5.1 Clock domain conversion

A conversion between two digital clock domains is normally done by first interpolating the data sampling frequency to the least common multiple (LCM) of both clock frequencies and then decimating it to the sampling frequency of the output clock domain. This technique is not suitable for the RF-DAC based transmitter, as the output clock frequency changes with the RF channel frequency. Thus, the frequency conversion ratio must be reconfigurable; a dynamic clock domain converter (CDC) is needed. Furthermore, it is not possible to interpolate first

to an LCM, as this can get very high due to the uncorrelated XO and LO frequencies. Therefore, an alternative topology is required.

In the utilized approach the XO dependent input signal is first sampled with the RF carrier frequency. This resampled signal can then be decimated to the needed fraction of the LO frequency. A simple unfiltered decimation leads to aliasing effects. The traditional solution of using a cascaded integrator-comb (CIC) filter [Hog81] is not applicable, as CIC filters can only suppress aliasing effects if there is a LCM frequency.

Using a high order lowpass FIR filter would solve the issue, but needs a high number of taps. This approach, however, necessitates a high number of multipliers driven by the high LO frequency which leads to a high power consumption and required area. It therefore is not feasible.

The number of multipliers can be reduced by determining the phase difference Δt between the XO frequency and the needed fractional LO frequency. By using Δt to choose a corresponding subset of filter coefficients from a look up table (LUT) the complexity of the FIR filter can be reduced to a low number of multipliers that are only driven with the needed fraction of the LO frequency.

More details on this approach by Thiel et al. can be found in [Thi+10]. Another computational efficient solution for fractional sample-rate conversion has been presented by Hentschel and Fettweis [HF99; HF00].

5.5.2 Upsampling and $\Delta\Sigma$ modulation

A $\Delta\Sigma$ modulator ($\Delta\Sigma$M) is used to reduce the required bit resolution of the RF-DAC. By choosing an appropriate clock frequency for the $\Delta\Sigma$ modulator, the replica spectra of the DAC can be moved to a frequency where they do not violate the spectral mask. The $\Delta\Sigma$M, however, is the most critical digital block in terms of speed due to its internal feedback loop. Thus, it limits the maximal possible clock frequency for the high-speed digital blocks.

Upsampling filters

The classical approach of implementing the input signal upsampling by an integer factor reduces the possible frequency schemes, as the output frequency also has to be an integer fraction of the carrier frequency. This limitation can be circumvented by using fractional upsampling factors. While the output frequency of the fractional clock domain converter is f_{LO}/N, as can be seen in Fig. 5.6, the output frequency of the upconverter is f_{LO}/M. Thus, the upconverter has an upsampling factor of M/N. This kind of system is basically realized by just sampling the input data with the higher output frequency. Afterwards interpolation filters are applied to suppress the alias spectra.
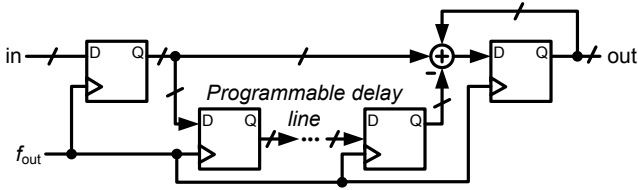
Figure 5.7: Implementation of one interpolation filter stage.
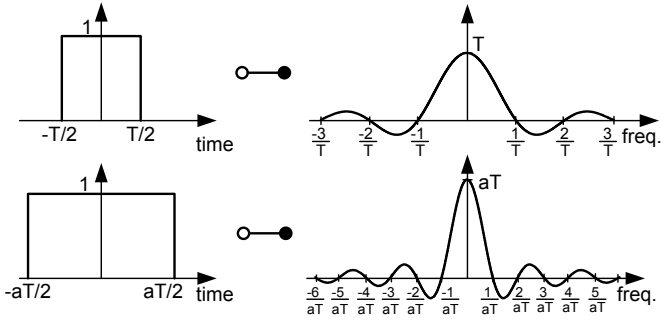
Figure 5.8: Filter response of one interpolation filter stage in the time and frequency domain for different filter length.

The interpolation filters are realized as rectangular brick-wall filters in the time domain, which have a *sinc* response in the frequency domain. A block diagram of the filter structure is shown in Fig. 5.7. The filter bandwidth can be set by programming the length of the delay line. The bandwidth of the filter is inversely proportional to the filter length T in the time domain:

$$\text{rect}\left(\frac{t}{T}\right) \circ\!\!\!-\!\!\!-\!\!\bullet\, T\frac{sin(\pi T f)}{\pi T f} = T \cdot sinc(Tf). \tag{5.6}$$

The frequency response for different filter lengths is depicted in Fig. 5.8. This type of filter has the advantage that it is simple to realize and can still be implemented for high clock frequencies. To obtain a good alias suppression, up to three filters with different filter lengths and thus corner frequencies can be applied in series. As can be seen from equation (5.6) the filter has an amplitude gain which depends on the filter length T. The output amplitude of the filter therefore has to be adjusted by a gain normalization step, to circumvent overflows in the subsequent digital circuits.
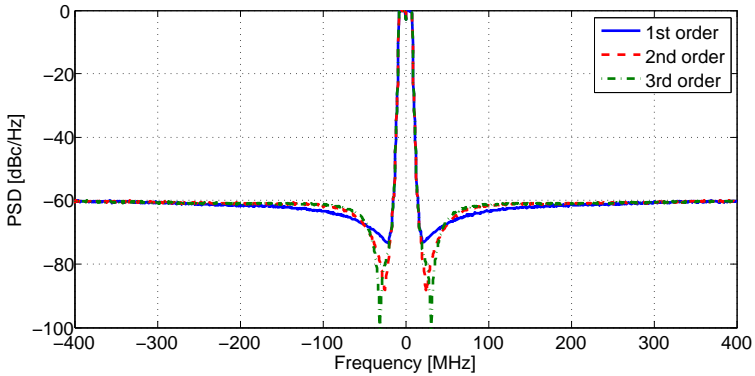
Figure 5.9: $\Delta\Sigma$ shaped spectrum of an 20 MHz wide OFDM signal for different $\Delta\Sigma$M orders. The signal is oversampled to 800 MHz, the $\Delta\Sigma$M resolution is 9 bit.

$\Delta\Sigma$ modulator

The $\Delta\Sigma$M which follows the signal upsampling can be designed using the Matlab $\Delta\Sigma$ toolbox developed by Schreier [ST04]. The $\Delta\Sigma$ toolbox allows to predict and synthesize noise transfer functions, calculate signal to noise ratios and simulate the time domain behavior of $\Delta\Sigma$ modulated signals.

The effect of different $\Delta\Sigma$M orders on a 20 MHz wide OFDM signal, oversampled at 800 MHz, with a $\Delta\Sigma$M resolution of 9 bit is shown in Fig. 5.9. The $\Delta\Sigma$ modulated signals have been simulated with Matlab in the time domain. Afterwards they have been converted to the frequency domain with an FFT to plot the corresponding spectra. It can be seen that increasing the $\Delta\Sigma$M order leads to a better SNR close to the wanted signal. For frequency offsets of above approximately 50 MHz from the center frequency, however, the emitted noise is higher for the higher-order $\Delta\Sigma$Ms. Interestingly, this frequency is significantly lower than the crossover point at $f_s/(2\pi)$ which is predicted by the simple linear model for sinusoidal input signals of equation (4.9).

The influence of the converter resolution on the output spectrum of the same OFDM signal is shown in Fig. 5.10 for resolutions of 8, 9, and 10 bits. As expected from theory (see section 4.3.2) the noise floor decreases by 6 dB per bit. Equivalently, the noise floor in the simulations also decreases by 3 dB per doubling of the sampling rate, as the total quantization noise is distributed over a larger frequency range.
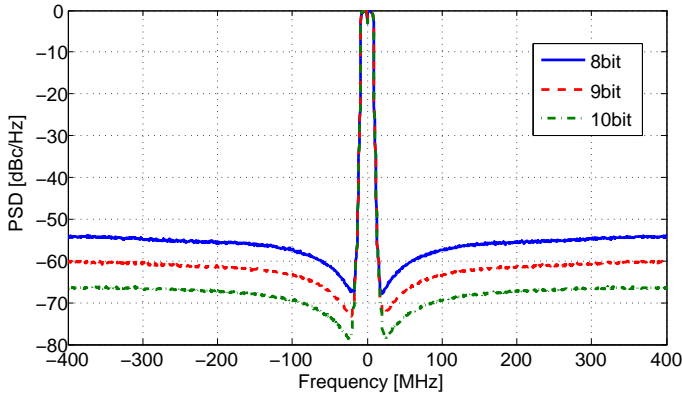
Figure 5.10: Spectrum of a 1st order $\Delta\Sigma$ shaped 20 MHz wide OFDM signal for different converter resolutions.

Introducing additional notches in the $\Delta\Sigma$ noise transfer function

Conventional lowpass $\Delta\Sigma$Ms only optimize the SNR in the signal band. Although this approach is helpful for the RF-DAC to achieve a good quality of the wanted signal, it does not solve the issue of high unwanted emissions farther away from the carrier. The emitted quantization noise has to be particularly reduced in critical frequency bands where neighboring receivers are operating concurrently, as explained in section 5.2. The most obvious solution is to increase the DAC resolution and oversampling rate sufficiently to fulfill the spectral mask. However, the required performance for RF-DAC and $\Delta\Sigma$M is not feasible, especially when taking their power consumption into account.

To get a better suppression of the noise at especially critical frequencies, additional notches can be placed in the noise transfer function (NTF) of the lowpass $\Delta\Sigma$M. For this approach, not all zeros of the NTF are placed in the signal band as it is typically done. Rather, the zeros are moved to frequencies farther away from the center frequency, where the noise has to be better suppressed. An example for this is shown in Fig. 5.11 for a 3rd order, 9 bit $\Delta\Sigma$M with notches at approximately 150 MHz offset from the carrier. Reducing the emitted noise at these specific frequencies however means additional noise at all other frequencies, as the overall quantization noise power stays constant. Consequently, the noise in the signal band increases and thus the SNR decreases. Also, the far-off noise increases drastically, as the comparison of the $\Delta\Sigma$ modulator output spectrum of Fig. 5.11 with the output spectrum of a conventional 3rd order low-pass $\Delta\Sigma$M with the same resolution in Fig. 5.9 reveals. But this does not have to be a major
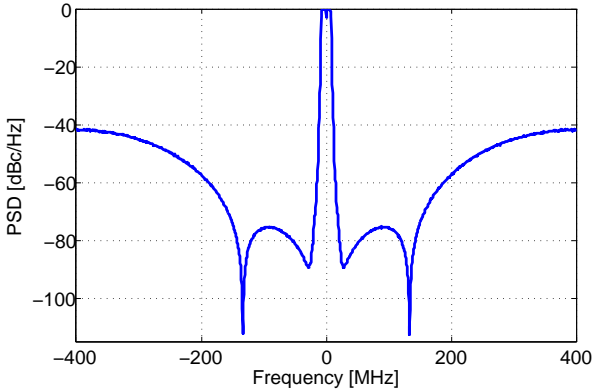
Figure 5.11: 3rd order $\Delta\Sigma$ modulated spectrum with additional notches in the noise transfer function.

concern, as the spectral mask is typically more relaxed at these frequencies.

By making the $\Delta\Sigma$M's coefficients programmable, the notches can be moved to different frequencies according to the requirements given by the current transmit frequency and communication standard. However, to simplify and speed up the internal multiplications, the filter coefficients must be restricted to integer numbers. Thereby, the frequency resolution for the placement of the notches is limited.

The notches do not have to be placed symmetrically around the carrier frequency. The quadrature signal processing allows the realization of complex valued NTFs. Thereby, even single-sideband notches can be implemented.

An example for the use of notches to suppress unwanted emissions at close-by receive bands is shown in Fig. 5.16 for an LTE transmitter operating in the 2.5 GHz band. Here, the emitted quantization noise in the nearby 2.4 GHz ISM as well as the own FDD receive band at approximately 2.6 GHz is reduced.

5.5.3 Mismatch and mismatch-shaping techniques

As every data converter, also the RF-DAC suffers from non-idealities through mismatch between the converter elements, leading to non-ideal output currents of each unit cell. While an accurate layout of the converter can reduce the mismatching problems [Pel+89], as discussed in section 6.4.2, additional digital mismatch shaping can even compensate a performance degradation caused by mismatch between the unit cells [WG02; Shu+99; Kim+08].
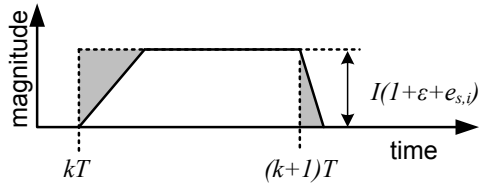
Figure 5.12: Simple model of static and dynamic mismatch errors.

Fig. 5.12 shows a simple model for the output signal of one DAC cell. Usually, this signal deviates from its ideal amplitude and its ideal rectangular pulse shape. In the case of the RF-DAC, amplitude variations are caused by inaccurate tail current sources in the unit cells. The cause of these variations can be split into two groups:

- "global" variability is caused by process variations from wafer-to-wafer, batch-to-batch, or even fab-to-fab.

- "local" mismatch is a variation between adjacent devices and may be process-induced, circuit-induced, or environment-induced.

Variations in the output magnitude from the ideal value are called *static mismatch*. The deviation of the output current $I_{out,i}$ of cell i from the ideal current I can be described as

$$I_{out,i} = I(1 + \varepsilon + e_{s,i}) \tag{5.7}$$

where ε describes the global and $e_{s,i}$ the local mismatch of unit cell i. Global mismatch affects all DAC unit cells alike and therefore does not lead to any decrease in converter resolution or performance. Only the total output current of the converter is scaled by a factor of ε, leading to a correspondingly higher or lower output power. The global mismatch thus can be neglected for the DAC analysis. Local mismatch can be modeled as a Gaussian distributed random variable with a mean of zero and standard deviation of σ_I.

Dynamic mismatch is caused by the limited slope of the output current. This leads to *glitches* when switching between different unit cells. Consider an input sequence (0, 1, 0). During this sequence, instead of the expected normalized charge 1, the charge $Q_{out,i}$ is transported, with

$$Q_{out,i} = 1 + \Delta\tau + \delta_i \tag{5.8}$$

where, equivalently to the static mismatch, $\Delta\tau$ is common deviation of all cells, whereas δ_i is the deviation of unit cell i from the common mean. When

(a) Tree shaper
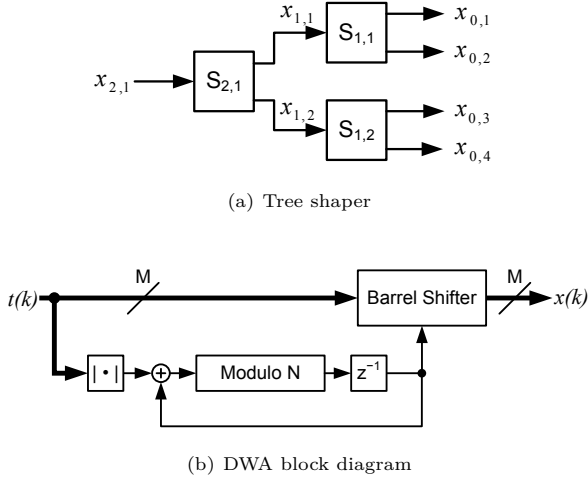
(b) DWA block diagram

Figure 5.13: Block diagrams of tree shaper and DWA.

neglecting the static global mismatch effect and assuming that the global factor $\Delta\tau$ dominates the dynamic mismatch, a simple model for the error signal $e(k)$ of a DAC with M cells can be found [Moh+10b; DM+03]:

$$e(k) = \sum_{i=1}^{M} e_{s,i} \cdot x_i(k) + \Delta\tau \sum_{i=1}^{M} |x_i(k) - x_i(k-1)| . \qquad (5.9)$$

Values for $e_{s,i}$ and $\Delta\tau$ can be found by Monte-Carlo circuit simulations. For initial simulations even typical empirical values can be assumed.

Mismatch shaping is based on a digital element selection logic (ESL) which selects a proper combination of one bit unit cell DACs. An improvement in overall accuracy can be obtained by a continuous and cyclic interchange of these nearly equal elements [Pla76]. By interchanging the different elements that vary around a common mean, a better average value can be realized.

Mismatch-shaping always needs some kind of redundant cell selection scheme. Several different mismatch-shaping algorithms can be found in literature. An overview and analysis of several popular element selection schemes is presented in [Moh+10a].

In general, the best mismatch shaping results can be realized with the so-called *tree shaper* which is shown in Fig. 5.13(a). Depending on the input word $x_{2,1}$ and pseudo-random switching sequence generators $s_{i,j}$ the required output word
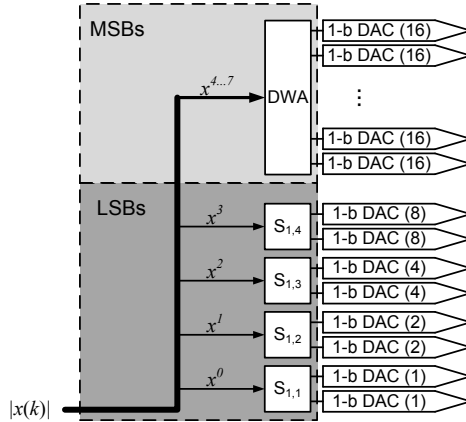
Figure 5.14: Block diagram of the mismatch-shaping ESL and segmented DAC architecture.

$x_{0,j}$ is set by different DAC cells. However, the tree shaper requires a purely unary DAC structure and has a high implementation effort, as each switching block requires its own switching sequence generator.

The *Data-Weighted-Averaging* (DWA) is a first order static mismatch shaping architecture for unary weighted DACs [WG02]. Fig. 5.13(b) shows the block diagram of the ESL for an N bit DAC with M elements. As input signal a thermometer coded signal $t(k)$ of the signal $|x(k)|$ is needed. The key element of the DWA is a barrel shifter which shifts the input vector $t(k)$ cyclic in MSB direction. As an example, equation (5.10) shows how a four element DWA processes the input sequence (2, 1, 3)

$$[0\ 0\ 1\ 1], [0\ 1\ 0\ 0], [1\ 0\ 1\ 1]. \tag{5.10}$$

The DWA requires less implementation effort and area than the tree shaper.

The above introduced mismatch shaping schemes reduce the impact of the static mismatch. However, they lead to an increased switching between DAC cells and thus increase glitches. Two different techniques exist to reduce this dynamic mismatch. A *return to zero* (RTZ) algorithm circumvents that the output of a DAC unit element is set to "one" in two successive clock cycles. Thereby, the dynamic error can be perfectly compensated. However, each DAC unit element is required twice to realize redundancy.

The *reduced glitching* algorithm just tries to reduce the switching between
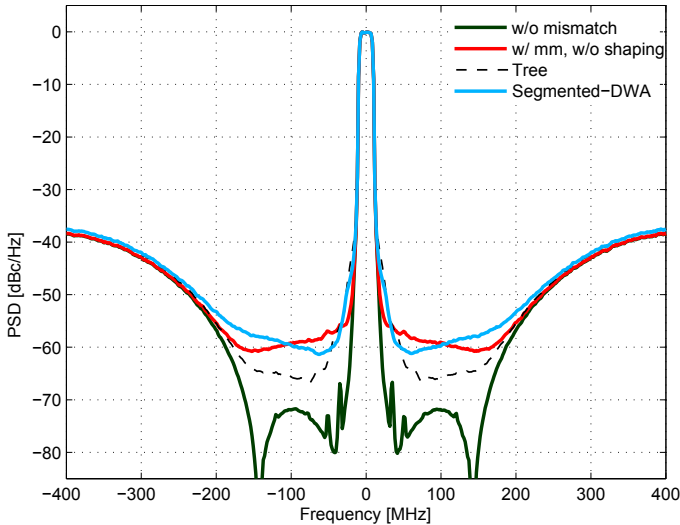
Figure 5.15: Effect of static and dynamic mismatch and different mismatch
shaping techniques on the OFDM transmitter output spectrum.

elements as much as possible. The effect is not as good as the RTZ approach, but no redundant DAC cells are needed.

For the RF-DAC based transmitter a comprehensive analysis to find the optimum mismatch shaping technique has been conducted [Moh09]. For this optimization process typical values for the mismatch of the RF-DAC unit cells have been taken into account. These values have been found by Monte-Carlo circuit simulations of the unit cells. Also, statistical signal attributes of LTE and WLAN OFDM signals have been contemplated. Particularly, it has been found that the high PAPR of OFDM signals allows an optimization of the mismatch shaping for low average output power levels, where few DAC cells are active. Thus, it is sufficient to add relatively few additional redundant DAC cells and still optimize the mismatch shaping for the most occurring output power levels.

It has been found that – under the boundary condition that the implementation and area overhead of the ESL may not be very high – an element selection scheme as depicted in Fig. 5.14 is optimum [Moh+10b]. This ESL necessitates that each binary weighted LSB unit cell is implemented redundantly, while for the unary weighted MSB cells a redundancy of only 2 additional cells is added. The LSB cells are controlled by "switching sequence generators" $S_{i,j}$, which are somewhat similar to a tree shaper, while the MSBs are controlled by a "data weighted

averaging" (DWA) ESL.

The effect of mismatch and mismatch shaping is shown in the system simulation result of Fig. 5.15. A combination of static mismatch with $\delta_I = 0.1$ and dynamic mismatch of $\Delta\tau = -0.05$ would lead to a dramatic increase of the noise floor close to the wanted signal (red curve). A tree shaper with unary weighted DACs cells (black, dashed curve) could significantly improve the matching and thus also the spectrum. However, it has a prohibitively high implementation effort. The performance of the chosen segmented-DWA architecture (blue curve) allows to reduce the unwanted emissions up to 6 dB at 45 MHz offset from the carrier while only having low additional area and power dissipation (2700 µm^2, 2.8 mW).

5.6 Final system simulation results

Several Matlab system simulations have been conducted for different communication standards and settings to determine the required system performance and specify parameters and performance requirements for the different building blocks.

It has been found, that one of the most critical scenarios in terms of unwanted spurious emissions is the operation of the transmitter in LTE band VII in the 2.5 GHz frequency band. This band is one of the first LTE frequency bands that will be used [Eri09]. It is especially critical, as the Tx band is centered between the close-by 2.4 GHz ISM band and the own Rx FDD band with a quite small duplex gap.

Fig. 5.16(a) shows the output spectrum of the transmitter in LTE mode with the larges specified signal bandwidth of 18 MHz. The carrier frequency f_{car} is 2540 MHz, which is in LTE band VII, and the Tx output power is set to 23 dBm (LTE class 3 device).

For the *LC* bandpass filter, a quality factor of 15 has been assumed.

To prevent the RF-DAC image frequencies from falling into parallel running GSM bands (DCS/PCS) the $\Delta\Sigma$ and RF-DAC clock frequency must be set to (at least) $f_{car}/3$ (=846.66 MHz). A third-order $\Delta\Sigma$ modulator with notches in the NTF at the critical neighboring receive bands, as it was introduced in section 5.5.2, has been used. The simulations reveal that the resolution of the RF-DAC must be at least 9 bit to meet the spectral mask.

Fig. 5.16(b) shows a closeup of the wanted band's spectrum. As can be seen, the adjacent channel power ratio (ACPR) is far below the allowed limit, leaving space for strong PA nonlinearities, which have not been included in the simulations. The small spurs around 20 MHz and 35 MHz offset are caused by the imperfect resampling of the dynamic clock domain conversion but are small enough to not impair the performance of the transmitter.

Besides fulfilling spurious emission limits, also the signal quality is of crucial
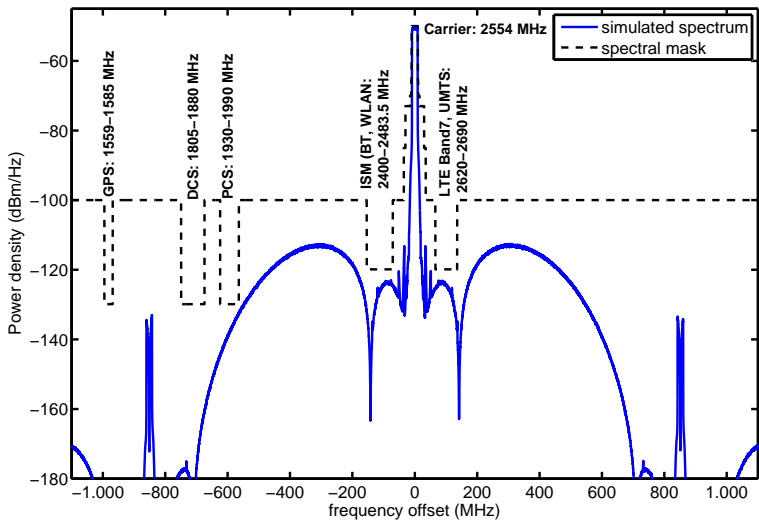
(a) wideband power spectral density
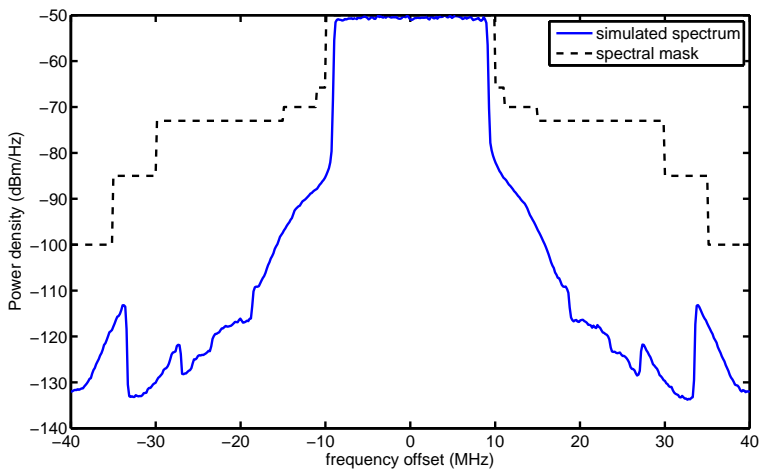
(b) narrowband power spectral density

Figure 5.16: Spectrum and emission mask of a 2.5 GHz LTE signal, simulated with Matlab
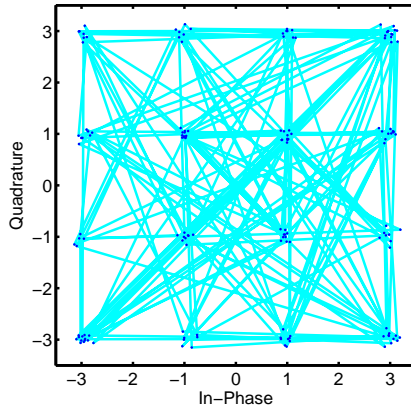
Figure 5.17: Simulated constellation plot of one 16QAM modulated OFDM subcarrier.

importance. It can be measured by the EVM, as introduced in section 2.2.7. EVM measurements for OFDM signals must be done for each subcarrier individually and then averaged over all subcarriers, as discussed in section 2.4.4. Simulations show that for the RF-DAC based transmitter with the above stated system parameters an EVM below 4 % can be expected for a QAM16 modulation scheme. The constellation plot for one subcarrier is shown in Fig. 5.17.

5.7 Summarization of the system specification

Figure 5.18 shows the final block diagram of the RF-DAC based transmitter, as it is realized in the prototype implementation.

The digital baseband signals are generated on an FPGA with a maximum sampling rate of 120 MHz and a resolution of 12 bit for each I and Q path. All high-speed digital blocks as well as the RF frontend are implemented on an RF integrated circuit chip (RFIC). FPGA and RFIC are connected via two parallel high-speed serial interfaces for I and Q which each have to support data rates up to 1.5 Gbps. The serial interface operates on low voltage differential signaling (LVDS) signals which are converted to CMOS levels on the RFIC utilizing common-mode logic (CML) to CMOS converter circuits. As no clock recovery functionality is implemented on the RFIC, the clock signal has to be transmitted in parallel to the actual data.

The serial data is deserialized to 12 bit wide parallel words. Afterwards, the input signals are resampled with a clock frequency which is derived from the RF

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	minimum	typical	maximum
Output Power			15 dBm
Output Frequency			2620 MHz
RF-DAC resolution		9 bit	
RF-DAC sampling rate (absolute)		500 MHz	870 MHz
RF-DAC sampling rate (relative to carrier freq.)	$f_{carrier}/9$		$f_{carrier}/2$
$\Delta\Sigma$M order			3
$\Delta\Sigma$M input resolution		12 bit	
CDC input sampling rate		100 MHz	120 MHz

Table 5.1: Summary of the RF-DAC based transmitter system specifications.

carrier frequency, using the dynamic clock domain converter. Subsequently, the digital signal is processed by the upsampler, $\Delta\Sigma$ modulator and element selection logic, as discussed in the previous section. Finally, the RF-DAC performs the D/A conversion and translates the baseband signal to transmit frequency. The RF-DAC output current is converted to a voltage utilizing an external LC-tank. The LC-tank also acts as a bandpass filter to suppress unwanted emissions at frequencies far from the carrier. For the prototype chip the LO signal for the upconversion mixer is generated off-chip using a signal generator. The 0/90° quadrature signals at the RF carrier frequency are generated out of this LO signal using a 2:1 frequency divider.

The programming of the reconfigurable parts of the RFIC can be done via a three wire interface which is connected to a microcontroller. The microcontroller enables the communication with a PC which controls the RFIC prototype in the measurements.

The main transmitter specifications are summarized in table 5.1.
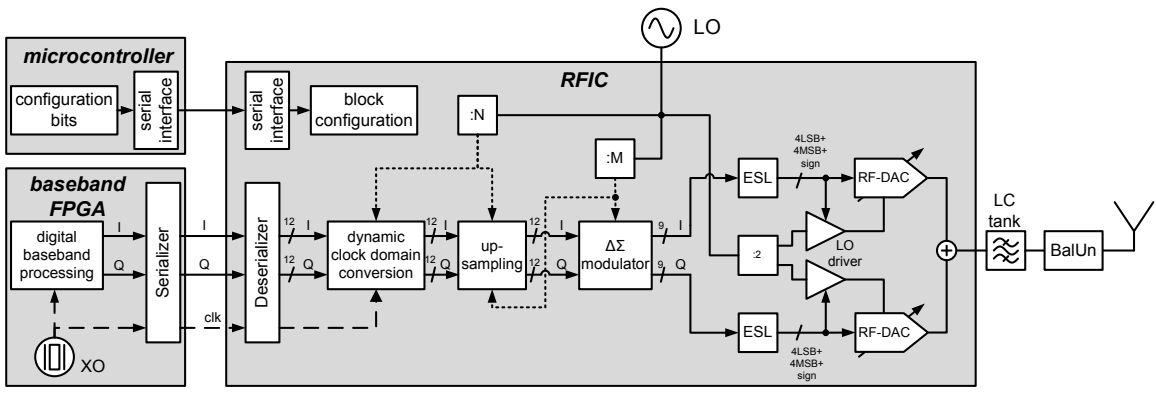
Figure 5.18: Detailed block diagram of the RF-DAC based transmitter prototype. The previously described high-performance digital and mixed-signal blocks are integrated on an RF integrated ciruit (RFIC). The digital baseband signal processing is implemented on an FPGA which communicates with the RFIC over a 1.5 Gbps serial interface. Several RFIC functionalities can be programmed via a three-wire interface by microcontroller. The *LC* bandpass filter and a balun are realized with discrete components on a test PCB.

6 Circuit Implementation of the RF Frontend

In this chapter, the circuit implementation of the mixed-signal and RF transmitter frontend will be discussed. While the purely digital blocks can be implemented with the help of a hardware description language such as VHDL or Verilog, the analog/RF and also especially critical high-speed digital blocks like the frequency dividers are full-custom designs.

After giving an overview of the transmitter frontend architecture and a short introduction to the utilized 65 nm CMOS technology, the different building blocks are explained in detail. Especially, the design of the RF-DAC unit cell is discussed. Two quadrature RF-DACs form a broadband I/Q vector modulator, as presented in the previous chapter. From the previously discussed system simulations it has been found that the RF-DAC should have a resolution of 9 bit (8 bits for magnitude and 1 bit for sign) and operate at a maximum sample rate of approximately 860 MHz to achieve the spurious emission limits and EVM requirements. The maximum LO frequency is 2.4 GHz to 2.62 GHz, when the transmitter is used for WLAN (ISM band) or LTE (band VII) applications.

Following the description of the circuit implementation of the main building blocks, simulation results of the complete frontend and an overview of the toplevel layout are given.

6.1 Basic structure of the implemented RF-DAC

Within the framework of this thesis, a novel RF-DAC unit cell structure has been developed. A principle implementation of the RF-DAC is shown in Fig. 6.1. The circuit implementation of the RF-DAC is based on a classical current-steering DAC architecture. Several weighted unit cells are connected in parallel and their RF output currents are summed at the output node. The unit cell integrates current-steering DAC and a double-balanced mixer. The RF-DAC unit cell topology of Fig. 6.1 looks quite similar to a double balanced Gilbert-type mixer and the RF-DAC implementation of Zhou and Yuan [ZY03] shown in Fig. 4.5.

In the topology of Fig. 4.5, the output current of a current-steering DAC is added to a fixed biasing current. The output current of the multi-bit DAC is upconverted to RF using one single upconversion mixer. This has the disadvantage that the voltage drop over the LO switching transistors increases with rising DAC output current. Hence, the variable DAC output current must be small compared to the fixed biasing current to guarantee a relatively constant
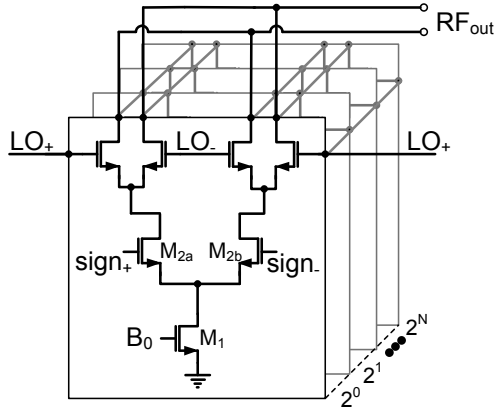
Figure 6.1: Principle implementation of the RF-DAC. The output current of N parallel weighted unit cells is summed at the RF output node.

DC voltage at the source node of the LO switching quad. A current-steering DAC output voltage that is strongly changing with the DAC output current would diminish the linearity of the DAC.

Therefore, in the RF-DAC implementation which is presented in this thesis, each unit cell consists of a digitally switched current source and a dedicated upconversion mixer for this single-bit current source. A multibit RF-DAC is formed by connecting several of these unit cells in parallel, as shown in Fig. 6.1. The fixed tail current source of each unit cell can be digitally switched on or off depending on the digital baseband magnitude B. The sign-bit is applied to a switching pair which is stacked on top of the switched current-source.

Depending on the digital input word, the current I_{out} of a unit cell is turned on or off completely. The current consumption of the converter directly scales with the output magnitude. Thus, this architecture has a high power efficiency even when operated in backoff. This is a big advantage compared to previously presented architectures [Elo+07; JS06; Tal+08] which have an RF-DAC bias current that is independent from the output magnitude. However, turning on and off the current source is slower than steering a constant current to different branches. Thereby, the maximum switching speed of the unit cell is limited.

In contrast to classical analog architectures, which require a Gilbert-cell mixer which has an analog baseband voltage as input, no highly linear and high-speed transconduction stage is needed. All transistors in the RF-DAC configuration are working as switches. Therefore, this topology is perfectly suited for modern
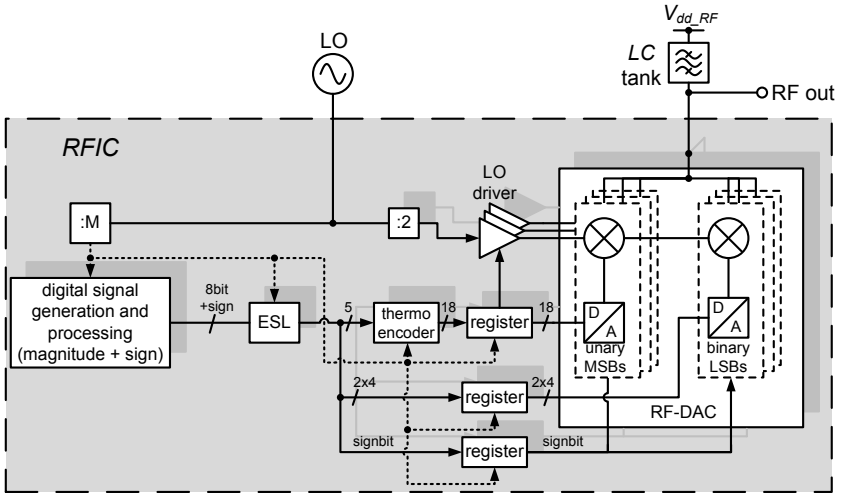
Figure 6.2: Block diagram of the RF-DAC based I/Q vector modulator. Only the inphase part is shown, the quadrature part is indicated by the shaded blocks.

nanoscale CMOS processes that provide excellent high-speed switches but only transistors with inferior analog properties.

6.2 I/Q vector modulator architecture

In Fig. 6.2 the realized I/Q modulator architecture consisting of two parallel RF-DACs and auxiliary building blocks is illustrated. Only the inphase part is shown, the quadrature part is indicated by shaded blocks. Fig. 6.2 gives a more detailed view of the RF-frontend compared to the transmitter blockdiagram of Fig. 5.18.

The digital signal generation blocks, including $\Delta\Sigma$ modulator, mismatch shaper and thermometer encoder are designed using the VHDL hardware description language and can be automatically synthesized. All other blocks in Fig. 6.2 are custom design blocks, developed on transistor level. The *LC* tank is realized off-chip with discrete components to reduce the complexity of the prototype chip.

The modulator has a magnitude resolution of 8 bit plus 1 bit for the sign per path, for both I and Q paths. The converter features a segmented architecture,
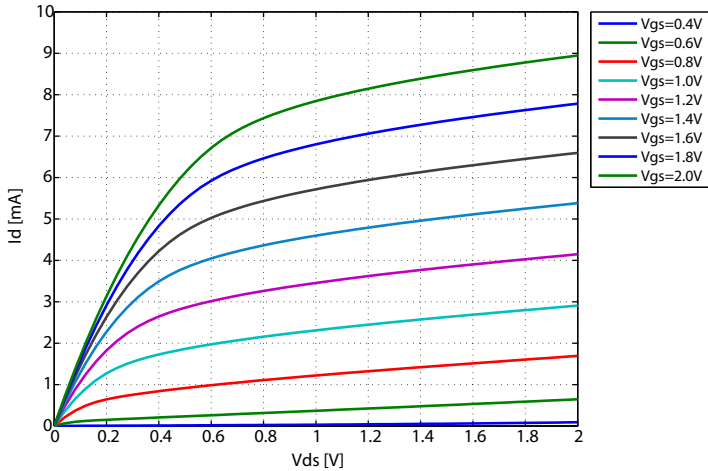
Figure 6.3: NMOS *I-V* device characteristics for a 60 nm gatelength transistor with an aspect ratio of 100.

the 4 least significant bits (LSBs) are realized as binary weighted cells, while the most significant bits (MSBs) are realized as unary weighted cells. Thereby, glitches are reduced while retaining a reasonably low complexity for wiring and control logic [Pla03]. A thermometer encoder is utilized to convert the MSBs from binary to unary representation. The thermometer encoder functionality is included in the element selection logic (ESL) block (see section 5.5.3).

The implementation of the LO buffers that amplify the LO carrier signal and drive the LO switching quads of the RF-DAC unit cells is based on an inverter chain. Each MSB unit cell has its own buffer. To save power, a buffer can be deactivated if the corresponding RF-DAC unit cell is also inactive. The implementation of the LO driver chain is described in section 6.5.

Registers are used to synchronize the switching of all blocks with a common clock signal. Also, they act as driver circuit for the RF-DAC switches. The registers consist of two consecutive latches. Details on the implementation of the latches can found in section 6.6.

6.3 Survey of the utilized 65 nm CMOS technology

The RF-DAC transmitter has been implemented in TSMC's CMN65LP 65 nm CMOS technology. The technology is optimized for low power consumption of

digital circuits. It features three different thin gate-oxide transistor types with standard, high and low threshold voltage. The thin gate-oxide transistors are compatible to 1.2 V supply voltage. In addition it provides thick gate-oxide transistors for I/O devices which are compatible to a supply voltage of 2.5 V. The technology features one polysilicon and nine metal layers that are made of copper. The top metal layer has a thickness of 3.4 μm. Capacitors can be realized using the MIM-capacitor option with a capacitance density of $2\,fF/\mu m^2$. A deep N-well option allows to place sensitive circuits in their own well with an isolated substrate contact.

In Fig. 6.3 the *I-V* device characteristics of an NMOS transistor with 60 nm gate length are shown. Short channel effects of the nanoscale CMOS transistors are very evident. The drain current only increases linearly with increasing gate-source voltage, instead of the classical quadratic behavior which can be observed for long-channel transistors. Also, the output resistance of the 60 nm transistors is very low, leading to a strong dependence of the drain current on the drain-source voltage.

6.4 Implementation details of the RF-DAC unit cell

Fig 6.1 shows a simplified schematic of the implemented RF-DAC unit cell. The biasing and control circuitry of the current source and sign function are not depicted. The current output DAC, which is controlled by the digital baseband input signal, consists of a switched tail current source M_1 and a transistor pair M_{2a} and M_{2b} which is stacked on top of the current source and steers the current to the positive or negative output, depending on the sign-bit of the digital input signal. The sign-bit changes relatively seldom compared to the sampling rate of the DAC. Therefore, the transistor pair acts as a cascode for the tail current source transistor. The cascode configuration has a very high output resistance, thereby minimizing the sensitivity of the output current to variations of the output voltage.

The control voltages of the transistors M_1, M_{2a} and M_{2b} have to be switched between zero and some biasing voltage, which allows optimum performance of the RF-DAC. Subsequently, an optimum biasing strategy for the RF-DAC unit cell is developed.

6.4.1 Biasing of the unit cell

The best way to accurately define the output current of each unit cell is by means of a current mirror. As the transistors M_{2a} and M_{2b} act as cascodes for M_1, a cascode current mirror is the topology of choice. Fig. 6.4(a) shows a simple cascode current mirror configuration. For finding the optimum biasing of

(a) Cascode current mirror

(b) Small signal equivalent circuit of M_1 and M_2
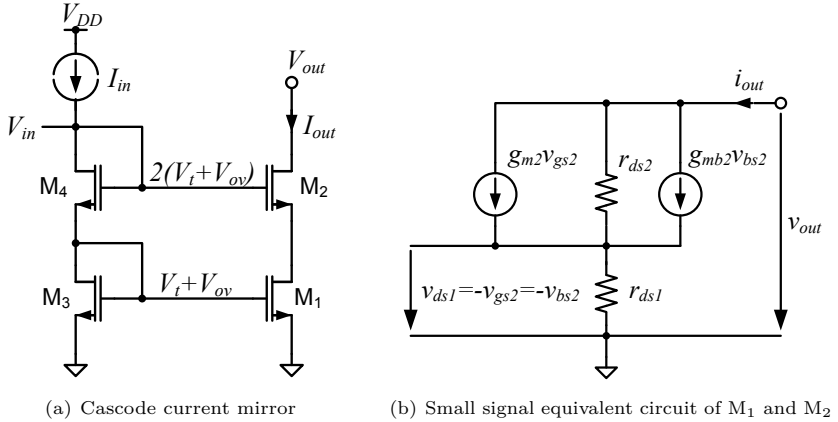
Figure 6.4: Cascode current mirror and its small signal equivalent circuit to determine r_{out}.

the transistors of the output brach, the transistor pair M_{2a} and M_{2b} is treated as a single transistor M_2.

Cascode current mirror

To achieve a high linearity of the current-output DAC, the output current should be as independent as possible from the output voltage. Thus, the output resistance of the current mirror must be maximized. The small signal equivalent circuit for determining the output resistance r_{out} of the output branch, consisting of M_1 and M_2, is shown in Fig. 6.4(b). From this equivalent circuit the (small signal) output resistance of the cascode current mirror can be found as

$$r_{out} = \left.\frac{v_{out}}{i_{out}}\right|_{v_{g1}=v_{g2}=0} = r_{ds2}\left[1 + (g_{m2} + g_{mb2})r_{ds1}\right] + r_{ds1}. \qquad (6.1)$$

The output resistance of a cascode current mirror has an output resistance which is much higher compared to a simple current mirror. Adding a cascode transistor increases r_{out} approximately by a factor of $(1 + g_{m2}r_{ds2})$.

Furthermore, it can be observed that the output resistance increases, when the (large signal) output current decreases. This, however, also decreases the maximum operation speed [Gra+01, p. 254].

To function properly, all transistors of the current mirror have to be operated in the active (saturated) region. This limits the minimum input voltage $V_{in,min}$

as well as the minimum output voltage $V_{out,min}$ and therefore the output voltage swing.

To be in the active region, the drain-source voltage of a transistor has to be greater than the overdrive voltage $V_{gs} - V_t$:

$$V_{ds} \geq V_{gs} - V_t = V_{ov}. \tag{6.2}$$

The minimum input voltage V_{in} for the cascode current mirror in Fig. 6.4(a) where both M$_3$ and M$_4$ are operated at the edge of the active region is therefore

$$
\begin{aligned}
V_{in,min} &= V_{gs3} + V_{gs4} \\
&= V_{t3} + V_{ov3} + V_{t4} + V_{ov4}.
\end{aligned} \tag{6.3}
$$

Assuming that all transistors have equal overdrives and ignoring the body effect[1], the minimum current mirror input voltage is

$$V_{in,min} = 2V_t + 2V_{ov}. \tag{6.4}$$

To operate M_1 in saturation $V_{ds1} \approx V_{ds3} = V_{gs3}$. For M_2, $V_{ds2} \geq V_{ov2}$. Therefore, the minimum output voltage $V_{out,min}$ for which both transistors of the output branch M_1 and M_2 are in the active region is

$$
\begin{aligned}
V_{out,min} &= V_{ds1} + V_{ov2} = V_{gs3} + V_{ov2} \\
&= V_{t3} + V_{ov3} + V_{ov2}.
\end{aligned} \tag{6.5}
$$

If all transistors have equal thresholds and overdrives,

$$V_{out,min} = V_t + 2V_{ov}. \tag{6.6}$$

Transistor M_2 operates in the triode region if $V_{out} < V_{out,min}$ and both M_1 and M_2 operate in the triode region if $V_{out} < V_{ov1}$. To allow high output amplitudes, the minimum output voltage $V_{out,min}$ at which M_1 and M_2 are still in the active region must be as small as possible.

For a given current I, the required overdrive voltage can be made small by using a large transistor aspect ratio. The threshold term in equation (6.6) however limits minimum output voltage and thus the maximum possible output swing.

Further investigating the circuit of Fig. 6.4(a), it can be found that the drain-source voltage of M_1 is

$$V_{ds1} = V_{in} - V_{gs2} = V_t + V_{ov}. \tag{6.7}$$

---

[1] The body-effect further increases the threshold of all transistors with $V_{SB} > 0$. In the cascode current mirror of Fig. 6.4(a) the transistors M_4 and M_2 would be effected, as far as they are not placed in their own p-well.

(a) Circuit that forces M_5 to operate in triode region

(b) Sooch cascode current mirror
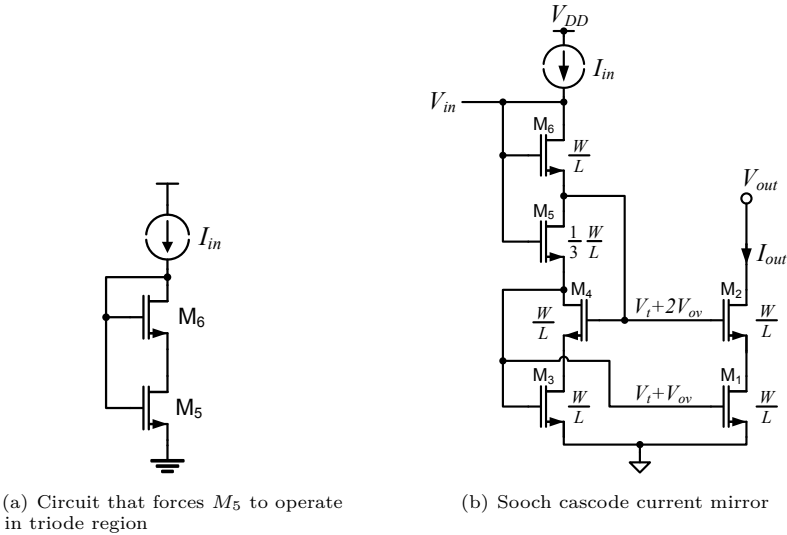
Figure 6.5: High swing Sooch cascode current mirror.

Hence, the drain-source voltage of M_1 is one threshold voltage larger than necessary to operate M_1 in saturation. Consequently, the gate voltage of M_2 has to be reduced by one threshold voltage to get an optimum biasing.

This can be achieved by introducing an additional intermediate branch with a transistor that does a level-shift of one gate-source voltage drop [Gra+01, p. 269 f.]. The transistors of the input branch have to be dimensioned in a way that the gate voltage of the level-shift transistor is $2V_t + 3V_{ov}$ as to achieve the optimum voltage of $V_t + 2V_{ov}$ at the gate of M_2. This kind of level shift circuit, however, has the drawback that it requires a quite high input voltage and also it introduces a considerable systematic gain error as the drain-source voltages of the input and output branch are not equal.

Sooch cascode current mirror

A more elegant circuit which enables a high-swing output is the cascode current mirror which was invented by Sooch [Soo85]. It is shown in Fig. 6.5(b).

The required difference in the gate voltages of M_1 and M_2 is one threshold voltage V_t. This difference can be generated by the voltage drop over a transistor in the triode region. In the circuit topology of Fig. 6.5(a) transistor M_6 forces

transistor M_5 to operate in the triode region.

To achieve the exact drain-source voltage drop of V_t the right aspect ratio of M_5 has to be found. M_6 operates in the active region, thus

$$I_{in} = \frac{k'}{2} \left(\frac{W}{L}\right)_6 (V_{gs6} - V_t)^2. \tag{6.8}$$

M_5 operates in the triode region, therefore

$$I_{in} = \frac{k'}{2} \left(\frac{W}{L}\right)_5 \left(2(V_{gs5} - V_t)V_{ds5} - V_{ds5}^2\right). \tag{6.9}$$

Assuming that V_{ds5} equals one overdrive voltage V_{ov} it can be concluded that

$$V_{gs5} = V_{gs6} + V_{ds5} = V_t + 2V_{ov}. \tag{6.10}$$

Equating (6.9) and (6.8) and substituting (6.10) leads to

$$\frac{k'}{2} \left(\frac{W}{L}\right)_5 \left(2(2V_{ov})V_{ov} - V_{ov}^2\right) = \frac{k'}{2} \left(\frac{W}{L}\right)_6 V_{ov}^2. \tag{6.11}$$

Equation (6.11) can be simplified to

$$\left(\frac{W}{L}\right)_5 = \frac{1}{3} \left(\frac{W}{L}\right)_6. \tag{6.12}$$

The circuit of Fig. 6.5(a) is used in the Sooch cascode current mirror of Fig. 6.5(b). All transistors except for M_5 have the same aspect ratio. By setting the drain-source voltage of M_5 to V_{ov} the gate voltage of M_2 is set to the optimum voltage $V_t + 2V_{ov}$. Thus, M_1 is biased at the edge of the active region which leads to the highest output voltage swing. The additional transistor M_4 is needed to set the drain-source voltage of M_3 equal to M_1, thereby eliminating the systematic gain error.

The above calculations use the equations for long-channel transistors and neglect body-effect. The calculated aspect ratio of M_5 therefore has to be checked by circuit simulations and optimized if necessary.

The major drawback of the Sooch cascode current mirror of Fig. 6.5(b) is the high required input voltage $V_{in,min}$, which limits the input voltage headroom.

$$V_{in} = V_{gs3} + V_{ds5} + V_{gs6} \geq 2V_t + 3V_{ov} \tag{6.13}$$
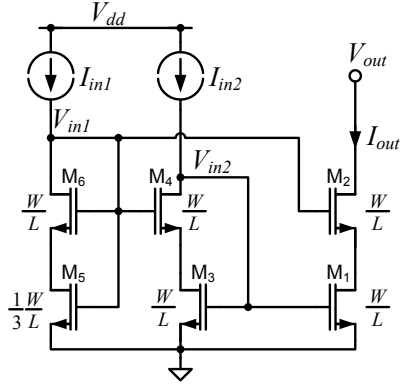
Figure 6.6: Sooch cascode current mirror with two input branches.

Sooch cascode current mirror with two input branches

A configuration which requires little input and output voltage headroom is the modified Sooch cascode current mirror with two input branches [Gra+01, p. 273f.]. Here, the transistors $M_3 - M_6$ of the input branch are not stacked, but distributed over two input branches. The corresponding schematic is shown in Fig. 6.6.

The minimum required input voltage V_{in} is by $V_t + V_{ov}$ lower compared to the normal Sooch cascode current mirror with one input brach.

$$V_{in1} = V_{DS5} + V_{GS6} \geq V_t + 2V_{ov} \tag{6.14}$$
$$V_{in2} = V_{GS3} \geq V_t + V_{ov} \tag{6.15}$$

Hence, it is well suited for low supply voltages of 1.5 V and below. Of course, two biasing branches also require twice the input current. On the other hand, the two input branches make it feasible to have a low supply voltage. Thereby, the overall power consumption of the biasing is hardly increased compared to a biasing structure with only one input branch.

M_5 and M_6 can even be collapsed into one diode-connected transistor whose source is grounded. The aspect ratio of this new transistor should be a factor of four smaller than the aspect ratios of M_1 to M_4 to maintain the bias conditions as in Fig. 6.6 [Gra+01]. This, however, is only feasible when the original aspect ratios of transistors M_1 to M_4 are sufficiently high.
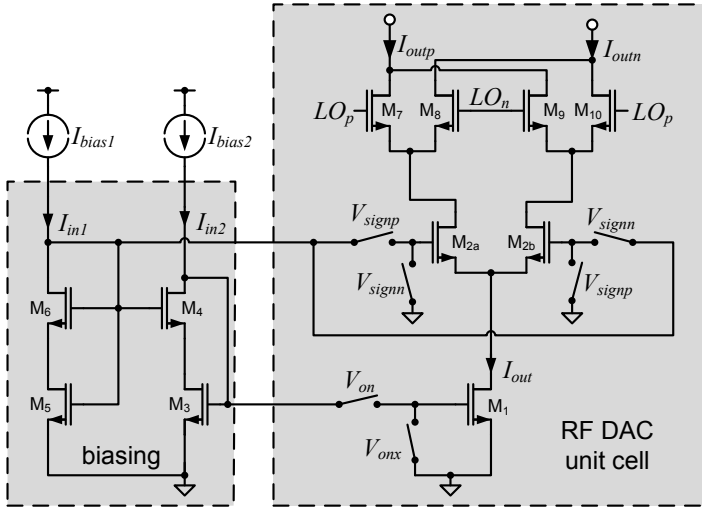
Figure 6.7: Circuit implementation of RF-DAC unit cell and biasing.

6.4.2 Final implementation of the RF-DAC unit cell with biasing

Fig. 6.7 shows the schematic of the finally implemented unit cell including biasing circuitry [Zim+09a]. Basis for the biasing of the unit cell is the formerly discussed Sooch high swing cascode current mirror. Transistors $M_{2a,b}$ act as a cascode for the transistor M_1 and steer the current to the positive or negative output, depending on the applied signbit. The gate voltages of M_1 and $M_{2a,b}$ are switched between V_{ss} and the corresponding bias voltage. The implementation of the switches is depicted in Fig. 6.8. The serial switches are implemented as transmission gates (M_{12}, M_{13}) to guarantee a low resistance of the switch, independent of the bias voltage. The parallel switches, which discharge the gate to V_{ss}, can be implemented as a simple NMOS transistor (M_{11}). This switching of the transistor M_1 has to be very fast as the clock rate can be up to 860 MHz.

On top of the cascode current mirror an LO switching quad (M_7 - M_{10}) is stacked to translate the DAC's baseband output signal to transmit frequency. The transistors are implemented as 2.5 V compatible thick gate oxide transistors. While the other analog blocks can be operated from a supply up to a 1.5 V the output branch can thus be connected to a high output voltage V_{out}. A high V_{out}, low required voltage headroom of the Sooch cascode mirror and utilization of an LC-tank as load enable high output voltage swings and thereby high output

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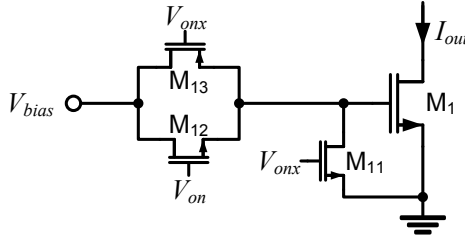
Figure 6.8: Implementation of the data switches with transmission gates.

		M_1	$M_{2a,b}$	M_3-M_4, M_6	M_5	M_7-M_{10}
MSB unit cell	W [μm]	48	48	2.4	0.96	32
	L [nm]	120	120	120	120	280
LSB unit cell	W [μm]	3	3	2.4	0.96	2
	L [nm]	120	120	120	120	280

Table 6.1: Transistor sizes in the LSB and MSB RF-DAC unit cells with biasing.

power.

The linearity of the RF-DAC is mainly determined by the output impedance z_{out} of the unit cells. Increasing the gate length of the transistors increases r_{ds} and thus z_{out} at DC but also leads to additional parasitic capacitances, lowering z_{out} at high frequencies. The output impedance of a cascode current mirror in dependence of the output frequency is plotted in Fig. 6.9. An optimum transistor gate length, depending on the needed switching rate, can be found. As the switching rate is typically in the range of a few hundred Megahertz for the RF-DAC implementation of this thesis, a transistor length of 120 nm has been chosen.

Furthermore, a trade-off between output impedance and maximum achievable output power exists. Increasing I_{out} necessitates larger transistor widths which again lead to higher parasitic capacitances.

Two different RF-DAC unit cells with different transistor sizes were used for MSB and LSB cells. The sizes of all transistors are given in table 6.1. The layout of one MSB unit cell (without biasing) is shown in Fig. 6.10. The large transistors in the center are the transistors of the output branch which have been laid out around a common symmetry axis. Dummy transistor fingers have
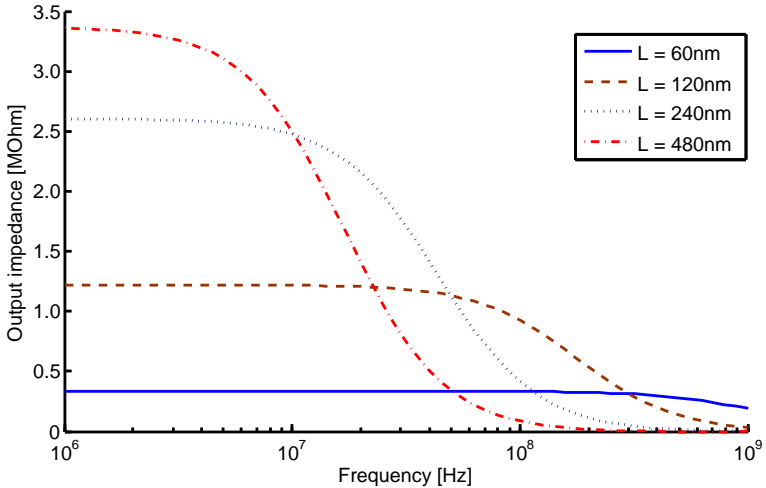
Figure 6.9: Output impedance (absolute value) vs. frequency of a Sooch cascode current mirror for different gate lengths with constant (W/L) ratio.

been placed left and right of the output branch transistors to improve matching. The smaller transistors at the sides are the digitally controlled switches.

The 65 nm TSMC process offers a deep (buried) n-well option. The deep n-well is a bit similar to a triple-well process option. It allows to create isolated p-wells that are enclosed by an n-well around and below the p-well. Each unit cell has been placed in its own p-well to achieve a good isolation of the unit cells.

The layout of the LSB unit cells looks similar to the MSB unit cell layout. The transistors of the unary weighted MSB cells, however, have an aspect ratio which is a factor of 16 larger compared to the smallest LSB cell. The binary weighting of the least significant four bits has been realized by using parallel unit cells for the higher order LSBs. The binary weighted LSB cells were laid out in a common centroid manner to improve matching as sketched in Fig. 6.11.

Because of the digital mismatch shaping, as described in section 5.5.3, some redundant MSB and LSB cells are needed. As a consequence of the utilized element selection scheme, all LSB cells are placed twice and three additional MSB cells are used for the two quadrature RF-DACs in the I and Q path.

While all LSB RF-DAC unit cells share one common biasing block, each MSB cell has its own biasing circuit. Although this increases complexity and area consumption it reduces disturbances to the biasing voltages which are caused by the switching of the unit cells. This disturbance could otherwise influence the

Figure 6.10: Layout of one MSB RF-DAC unit cell (without biasing and local LO driver). The size is approximately $29\text{x}26\,\mu\text{m}^2$.

Figure 6.11: Common-centroid layout and wiring of the control signals V_{on} of the binary weighted LSB RF-DAC unit cells. The subscripts indicate the order of the binary weighted cells.

output current of the unit cells, thus reducing the signal quality of the output signal. To further stabilize the bias voltages, capacitances were added at the drain nodes of M_4 and M_6, utilizing dummy transistor gates.

In addition to switching on and off the unit cells, the output power can also be regulated by means of the input biasing currents I_{in1} and I_{in2}. These biasing currents are generated with current mirrors out of a common reference current I_{ref}. Thus, the output power can either be regulated by changing I_{ref} or by changing the current mirror ratio. The implementation of the programmable current mirror is discussed in section 6.7.

To maximize the switching speed of regular current steering DACs, the output current of the unit cells is usually not switched on and off. Instead, the current in the output branch of the unit cell of these DACs is either switched to the output or is dumped to GND or V_{DD}. This, of course, has the drawback of a high and constant current consumption, independent of the output amplitude and the respective current level. To lower the average current consumption and improve power efficiency the here presented design features an on/off switch for the gate voltage of transistor M_1. Thereby, the output current I_{out} can be switched off instead of dumping the current to ground, as it is done for classical current-steering architectures. Switching off the input bias currents I_{in1} and I_{in2} of the respective DAC unit cell in a similar manner would further reduce the current consumption. However, such a ramping of the biasing circuit proved to be too slow for a sample rate of several hundred Megahertz.

The functionality of the RF-DAC core has been simulated with sinusoidal test signals. As digital input signals are needed for the RF-DAC, an analog sinusoid signal was sampled with an ideal 9 bit A/D converter which has been modeled in the Verilog-A circuit description language. The resulting binary weighted digital signal has been converted to a signal which is suited for the segmented DAC architecture using a thermometer encoder.

Fig. 6.12 shows the differential output current waveform of one 8 bit plus sign-bit RF-DAC for a digital sinewave input signal. The signal has a frequency of 2 MHz and is sampled at 800 MHz which is one third of the RF carrier frequency. The simulated output signal envelope has an almost ideal quantized sinusoidal form. However, when looking closely it can be recognized that the output current envelope sometimes drops slightly for a short moment. This is caused when additional RF-DAC unit cells are activated. When switching on a unit cell it takes some time until the correct output current has settled. Nevertheless, this should not degrade the DAC resolution, as the received signal is sampled at the middle of each symbol, where the output amplitude has settled to the correct value.
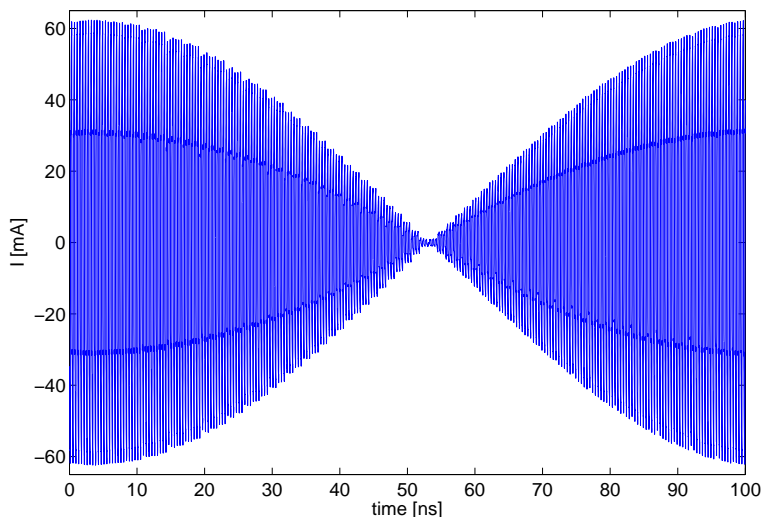
Figure 6.12: Differential output current waveform of one RF-DAC with a resolution of 8 bit plus sign-bit. The plot shows half a period of a 5 MHz sinewave test-signal, sampled at 800 MHz. The carrier frequency is 2.4 GHz.

6.5 Implementation of the LO driver chain

The quadrature local oscillator signals which are driving the upconversion mixer are generated out of an reference oscillator signal at twice the carrier frequency using a frequency divider, which is discussed in section 6.8.1. For the prototype implementation, the reference oscillator signal at twice the carrier frequency is generated off-chip with an RF signal generator.

In every transmitter, the LO switch drivers amount perceptible to the total power consumption. Also, mismatch in the switching quad transistors of the mixer leads to an unwanted LO signal feedthrough to the RF output. The RF-DAC transmitter does not feature a monolithic upconversion mixer but rather one which is distributed over all RF-DAC unit cells. Therefore, the overall mismatch is smaller as opposed mismatches in different unit-cell switching quads can compensate for each other. On the other hand, LO feedthrough gets more of an issue when operating the transmitter in back-off as the signal magnitude decreases while the LO amplitude and thus the feedthrough stays the same. In a conventional analog architecture, as shown in Fig. 2.1, this is not a problem if
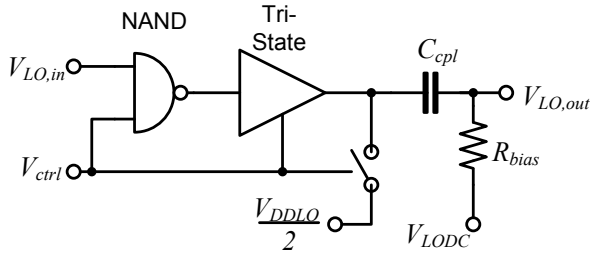
(a) Block-diagram of LO driver with control logic
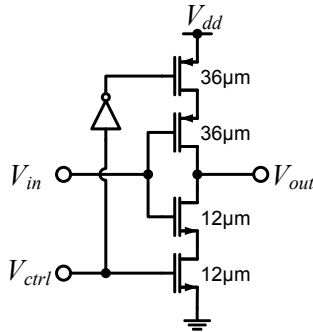
(b) Schematic of the tri-state inverter

Figure 6.13: Single-ended block diagram of LO driver with control logic.

the output power is controlled by an RF variable gain amplifier (VGA) placed after the upconversion mixer which equally scales both wanted signal and LO feedthrough amplitude.

The LO driver realization is based on a chain of inverters. In combination with the LO DC reference level V_{LODC}, the LO driver's supply voltage can be used to control the amplitude of the switching signal and thus optimize power consumption as well as linearity of the mixer [Lee03].

To further improve power consumption and LO feedthrough for small signal amplitudes not all RF-DAC unit cells share one single LO driver but rather a group of RF-DAC unit cells gets its own LO driver. Thereby, the respective LO driver can be switched off when the whole group of unit cells is inactive. In the presented design, all unary weighted MSB unit cells have their own LO driver, while all LSB cells share a common LO driver block.
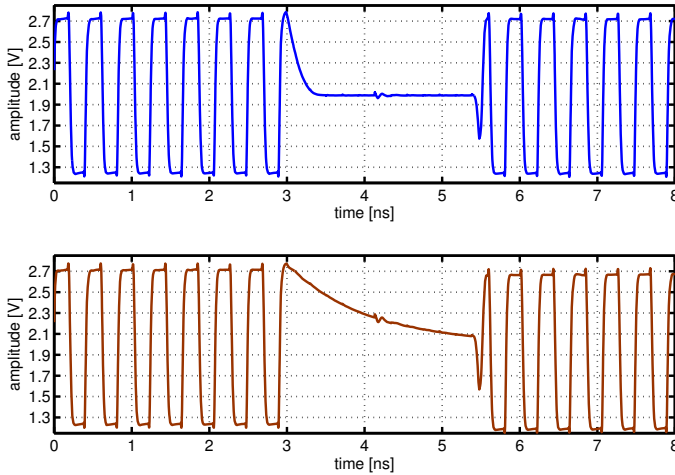
Figure 6.14: Output voltage waveform $V_{LO,out}$ of the LO driver with control logic. The figure on top shows the signal when the tri-state output is pulled to $V_{dd,LO}/2$. Below, the signal with floating tri-state output is shown.

Fig. 6.13(a) depicts how the control logic for the LO driver building block is realized. When the RF-DAC unit cell is in "on" state ($V_{ctrl} = 1$), NAND gate and tri-state operate just like ordinary inverters and amplify the LO signal. When $V_{ctrl} = 0$, on the other hand, the output of the NAND gate is forced to "high" and the output stops oscillating with the frequency of the LO signal. At the same time, the tri-state switches into high-impedance output mode. This permits setting the voltage at the left side of the coupling capacitor C_{cpl} to half the LO supply voltage, which is also the average voltage in "on" state. This mechanism of keeping the DC voltage constant is necessary to circumvent reloading transients of the $V_{LO,out}$ voltage which is applied to the switching quad transistor gates.

The effect of deactivating the oscillating output signal is plotted in Fig. 6.14. In the upper figure, the output signal $V_{LO,out}$ of the implemented LO driver is shown. When the signal is turned off the output of the tri-state buffer is pulled to half its supply voltage. Thereby, the signal $V_{LO,out}$ directly reaches its correct DC level V_{LODC}.

When the tri-state output is not pulled to the correct DC level at the moment that the buffer is switched off, relatively slow transients are caused on the right

hand side of the coupling capacitor C_{cpl}. This is depicted in the bottom picture. Thus, the DC level may not identical to V_{LODC} when the LO driver is switched on again. In Fig. 6.14 this shift in DC level is roughly 60 mV. It is much worse when the off-period of the LO driver is shorter. The inverted LO driver signal V_{LOn} experiences a similar transient, but with a phase-shift of 180°. Thereby, the difference between DC voltage levels of the V_{LOp} and V_{LOn} signals for the example of Fig. 6.14 is approximately 120 mV when switching on the LO drivers, leading to distortions of the output signal.

The logic operation of the tri-state is the same as of a combination of tri-state plus NAND gate. Anyhow, without the NAND gate preceding the tri-state the RF signal input of the tri-state would be always active, leading to a considerable feedthrough of the LO signal to the output node $V_{LO,out}$ even if the tri-state is switched to high-impedance output mode.

As the transistors of the LO switching quad in the RF-DAC are relatively large, quite big coupling capacitors C_{cpl} are needed. These coupling capacitors are realized as MIM-capacitors. Each capacitor C_{cpl} has a size of 1.8 pF. To save chip area, the coupling capacitors have placed in the higher metal layers above the active RF-DAC circuitry in the layout.

6.6 Implementation of the latches and registers

Registers are used to synchronize the switching of all RF-DAC unit cells. In addition, they act as driver circuit for the RF-DAC switches. The registers consist of two consecutive latches. For a good RF-DAC performance the latches have to be designed in a way that the RF-DAC's serial and parallel switch transistors (M_{11} - M_{13} in Fig. 6.8) are not on at the same time. Otherwise, a current would flow from the biasing branches to V_{ss}, discharging the bias voltage nodes V_{bias}. On the other hand, the transistors also should not simultaneously be turned off for a too long time. To make sure that both switches are simultaneously in the off-state for a short instance, the rising edge of the control signal V_{onx} should not go up until the falling edge of V_{on} has occurred. In other words, the crossover point of these two signals has to be at a low amplitude.

A differential latch as presented by Bosch et al. [Bos+01] has been used for this purpose. The schematic of the latch is depicted in Fig. 6.15. This type of latch can achieve a very high speed operation. Also, it allows to set the crossover point of the control signals by using different rise and fall times for the differential output of the latch. The rise and fall time of the output signals can be controlled by changing the width ratio of the PMOS to NMOS transistors. If the ratio is similar to the μ_p/μ_n electron mobility ratio, the crossover point is located at half the supply voltage. In addition, the cross coupled NMOS transistors M_5 and M_6 increase the discharging speed, thus lowering the crossover points.
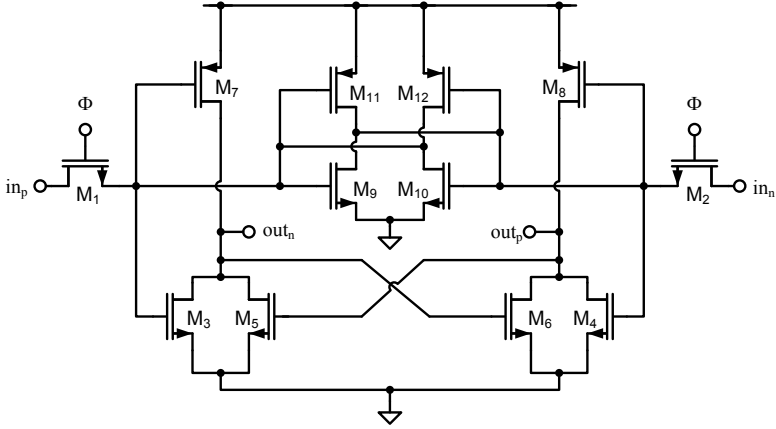
Figure 6.15: Schematic of the latch driving the RF-DAC unit cell.

	M_1, M_2	M_3–M_6	M_7, M_8	M_9, M_{10}	M_{11}, M_{12}
transistor widths MSB latch [µm]	2	6	12	2	1
transistor widths LSB latch [µm]	0.6	1.2	2.4	0.24	0.48

Table 6.2: Transistor width in the latches driving the LSB and MSB RF-DAC unit cells. All transistors have the minimum length of 60 nm.

The latches are optimized for low required voltage headroom. Only two stacked transistors are needed. To achieve this, the input signals are sampled by transfer gates (pass transistors M_1 and M_2). The clock feedthrough of the pass transistors is suppressed by small inverters (transistors M_9 to M_{12}). Furthermore, these inverters stabilize the synchronized inputs. Making the aspect ratio of the inverters too large, however, can hinder the toggling of the latch.

As the MSB and LSB RF-DAC unit cells have different input capacitances, two differently sized latches were used for driving the unit cells. The transistor sizes of the implemented latches are given in table 6.2.

Figure 6.16: Schematic of the programmable bias current DAC. Transistor sizes are given in micrometers.

6.7 Realization of the bias current DAC

The biasing currents I_{bias1} and I_{bias2} of the RF-DAC unit cell bias structure in Fig. 6.7 are generated with current-mirrors out of a reference current I_{ref}. For this prototype implementation I_{ref} is generated by an external current source. If needed, the reference current generation could be integrated into the transmitter chip, by means of a bandgap reference circuit.

The output power level of the RF-DAC transmitter scales with the biasing currents I_{bias1} and I_{bias2}. Hence, the current mirror has been implemented as a bias DAC, enabling a programmable power control. In this design, a 5-bit DAC implementation has been chosen. Thereby, the current mirror ratio from reference current I_{ref} to output current I_{out} can be programmed from 0.5 to 15.5. For the prototype design the reference current of the external current source can be modified in the measurements, to achieve an even better power control. For a product, a bias DAC with sufficient resolution for the power control requirements of the the targeted communication standard is needed. This can be quite challenging, as e.g. WCDMA requires an output power control of more than 70 dB which has to be variable in 1 dB steps [3GP10]. However, Eloranta et al. [Elo+07] showed that a power control of 90 dB is possible with an RF-DAC based transmitter.

The schematic of the bias DAC is shown in Fig. 6.16. Only one bias current output is shown. In the real implementation, the output side of current mirror is needed twice, as two bias currents I_{bias1} and I_{bias2} are required for the Sooch cascode current mirror with two input branches.

The bias DAC uses switch transistors which are stacked at the drain of the current mirror transistors. This configuration acts as cascode for the current

Figure 6.17: Block diagram of the 0°/90° LO frequency divider.

mirror, thus increasing the output resistance. Also, it leads to a relatively simple layout. Alternatively, the control switches could also be implemented as gate switches. Thereby, the required output voltage headroom of the bias DAC could be reduced. This, however, would also dramatically increase the required layout effort. To improve matching, the transistors were laid out in a common-centroid fashion and dummy transistors were placed at the borders of the transistor array.

6.8 Implementation of the frequency dividers

Several frequency dividers are utilized to generate the required clock frequencies from a common local oscillator (LO) signal. For the RF-DAC transmitter prototype the LO signal is generated off-chip using an RF signal generator. For a fully integrated transmitter chip the LO signal would be generated by an on-chip PLL.

6.8.1 LO frequency divider

The LO input signal in Fig. 6.2 has twice the frequency of the RF carrier signal which is fed to the upconversion mixer switching quad. Thereby, I/Q signal components with an accurate 0°/90°phase shift can be generated with a divide-by-two (2:1) frequency divider. Several different digital and analog frequency divider architectures (e.g. regenerative frequency divider, injection locked mixer) can be found in literature [Raz97; Lee03]. For the maximum required input frequency of approximately 5 GHz a digital divider should be sufficiently fast, as it is implemented in a high-speed 65 nm process. A popular

Figure 6.18: Schematic of the self-biased LO input buffer. The transistor length is 60 nm.

topology incorporating two latches in a negative feedback loop, as shown in Fig. 6.17, has been chosen.

The differential sinusoidal LO input signal (denoted as CLK and $\overline{\text{CLK}}$) is first amplified and shaped to a square wave by two parallel pseudo differential self-biased input buffers. The buffered LO input signal is used as a clock signal for a fed back master-slave register. Note, that the clock input signals of both latches have to be inverted.

The schematic of one LO input buffer is depicted in Fig. 6.18. The input signal is AC-coupled via capacitor C_1, which permit the application of an external LO voltage source with zero DC offset. The feedback resistor R_1 leads to a very simple self-biasing structure, as it pulls the DC gate voltage of the transistors M_1 and M_2 to half the supply voltage V_{dd}.

The 2:1 frequency divider of Fig. 6.17 has four signal outputs at half the input frequency, each with a phase shift of 90°. A precise 90° phase shift is important to achieve a good image signal suppression of the I/Q modulator. Truly complementary CLK and $\overline{\text{CLK}}$ signals and a good matching of the latches are therefore required. The output signals of the latches are buffered by inverter chains and then used as input signals for the LO driver circuit discussed in section 6.5.

The circuit implementation of the differential latches is shown in Fig. 6.19. Due to the feedback loop in the frequency divider and the very high frequency at which it operates, this circuit has to be very fast. Speed can be increased by using large transistor sizes. Anyhow, a trade-off between transistor speed and power consumption exists.
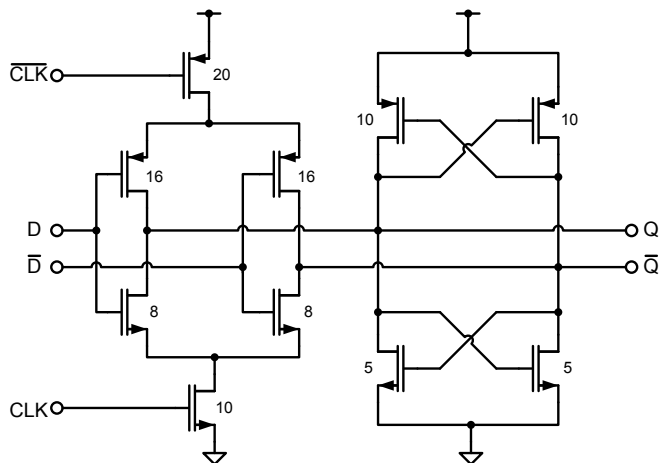
Figure 6.19: Schematic of the latch for the LO frequency divider. Transistor widths are given in μm, all transistors have minimum length.

6.8.2 Programmable frequency dividers

The clock signals for the digital signal processing blocks are derived from the RF carrier frequency as discussed in chapter 5 and shown in Fig. 5.18. Two different clock frequencies are required, a slow running clock clk_{slow} at approximately the sampling rate of the baseband input signals and a fast running clock clk_{fast} which determines the clock rate of $\Delta\Sigma M$, ESL and the sampling rate of the DAC unit cells. In Fig. 5.18 the clock divider for the slow clock is labeled as ":N", while the divider for the fast clock is labeled as ":M".

Divide-by-two frequency dividers can be realized by a D flip-flop with positive

(a) 3:1 frequency divider

(b) programmable 2/3 frequency divider
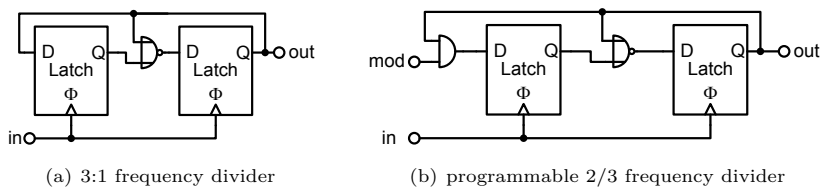
Figure 6.20: Realization of a multi-modulus frequency divider.
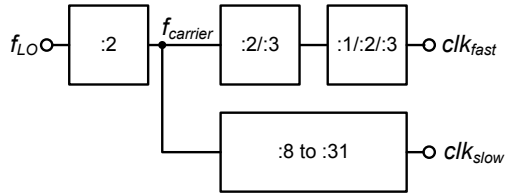
Figure 6.21: Overview of the programmable, LO derived clock generation.

feedback, as presented in the previous section. Cascading n divide-by-two frequency dividers enables divider ratios of $n \cdot 2$. A frequency division by $2 \cdot n - 1$ can be realized by combining the output of the first and the last register of the divider using a NOR gate, as shown in Fig. 6.20(a) for a 3:1 frequency divider. Thereby, a Johnson counter is realized; the NOR gate inhibits one of the four states of the state machine that is realized by the two consecutive latches. Due to the timing-critical feedback, 3:1 dividers can only operate up to frequencies far below the maximum operating frequencies of 2:1 dividers. Also, it must be noted that integer-N dividers with an uneven divider ratio do not have a 50% duty cycle. This could be an issue, if both the rising and falling edges of the clock signal are needed for the digital signal processing in "double data rate" applications.

To be as flexible as possible, the frequency dividers should be programmable to different integer-N divider ratios. Fig. 6.20(b) shows how a programmable multi-modulus clock divider that divides the frequency by either a factor of two or three can be realized [Raz97].

The clock generation scheme for clk_{fast} and clk_{slow} is shown in Fig. 6.21. The LO input frequency is first divided by a factor of two, using the LO frequency divider presented in section 6.8.1, to achieve the carrier signal frequency $f_{carrier}$. clk_{fast} and clk_{slow} are subsequently derived from the carrier frequency. The fast clock is created by two consecutive multi-modulus dividers and can be set to be 1/2, 1/3, 1/4, 1/6 and 1/9 of the carrier frequency. To achieve the 1/2 and 1/3 divider settings the second frequency divider must be bypassed. Thus, for a carrier frequency of 2.4 GHz RF-DAC sampling frequencies between 267 MHz and 1.2 GHz can be set. However, the speed of the digital signal processing circuits, especially the $\Delta\Sigma$ modulator and the dynamic clock domain conversion, does not permit clock frequencies far beyond 860 MHz.

The block diagram of the frequency divider for clk_{slow} is shown in Fig. 6.22. This divider can be programmed to all integer values between 8 and 31. Thus, for a 2.4 GHz carrier frequency, clk_{slow} could be set between 77.4 MHz and 300 MHz.

The upsampling block in Fig. 5.18 requires clock signals clk_{fast} and clk_{slow}
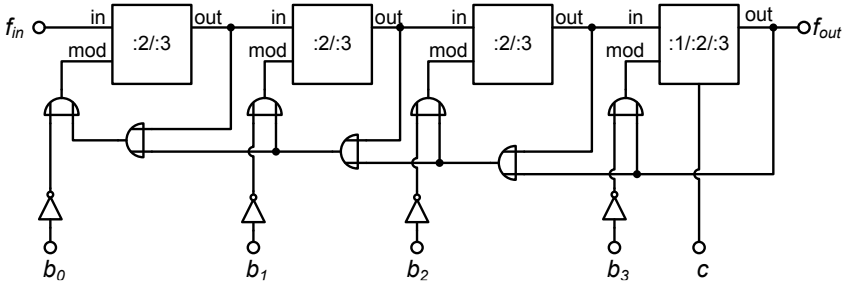
Figure 6.22: Programmable frequency divider with divider ratios from 8 to 31.
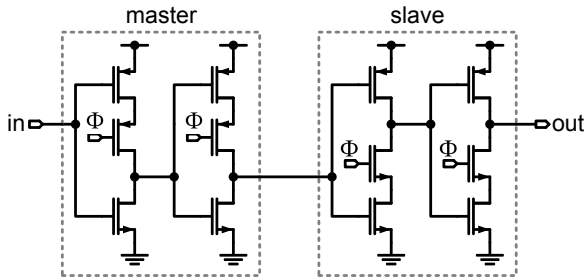
Figure 6.23: Schematic of a positive edge triggered TSPC register.

with aligned rising clock edges. Therefore, the edges of these two clock signals are synchronized with the help of registers that are clocked with the $f_{carrier}$ signal.

Circuit simulations revealed that standard static latches are not fast enough for high input frequencies of up to 2.5 GHz. The speed limitation of static latches is caused by a feedback structure which is used to store the applied information as long as power is supplied to the latch. Dynamic latches on the other hand do not store their information using a feedback loop. While this limits the minimum input signal update rate – which is no real issue for the application as a high-speed clock divider – it makes them much faster compared to static latches. True single phase clock (TSPC) latches [YS89] have been used to implement the dynamic registers. Fig. 6.23 shows the schematic of a positive edge triggered TSPC register as it has been utilized for the implementation of the frequency dividers. The TSPC architecture does not require a differential clock. This reduces skew problems and reduces the clock load as the clock buffers
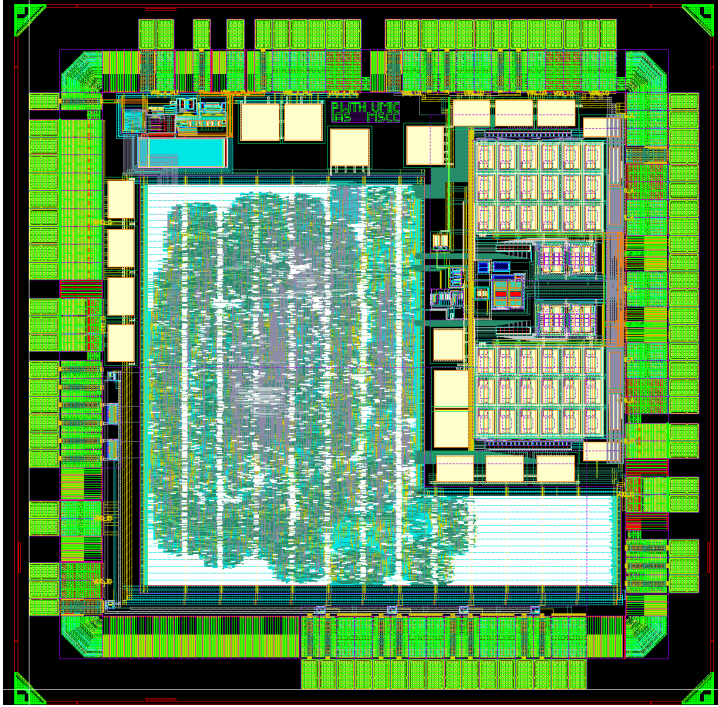
Figure 6.24: Toplevel layout of the complete transmitter prototype chip.

have to drive fewer transistors. Thereby, a very high speed operation can be achieved.

6.9 Toplevel layout

Figure 6.24 shows the toplevel layout of the complete RF-DAC based transmitter prototype with full-custom mixed-signal and RF blocks as well as a synthesized digital block. The complete chipsize including pads and sealring is $1.9 \times 1.9 \, \text{mm}^2$.

The analog and RF frontend is located in the top right corner. The L-shaped layout of the digital circuits that were implemented in VHDL and then automatically placed and routed can also be identified easily.

The chip was bonded into a QFN48 package. The pinout of the package is shown in Fig. 6.25. All high-speed digital and RF inputs and outputs are laid
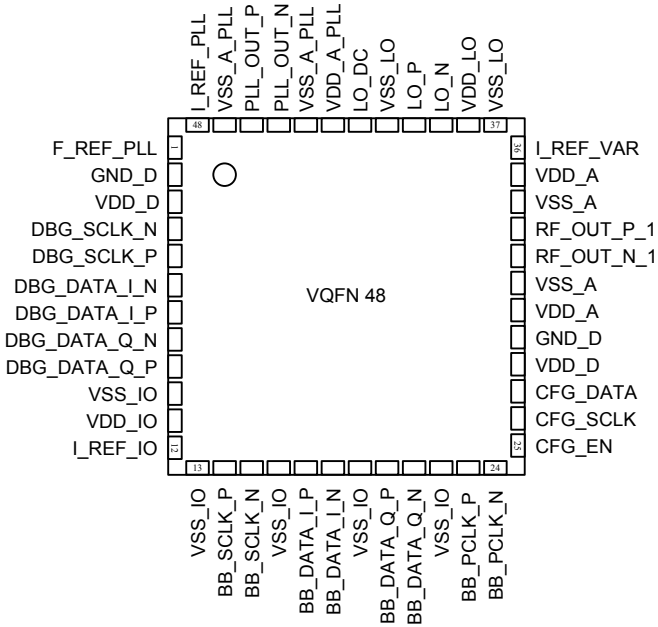
Figure 6.25: Pinout of the QFN48 package.

out differentially. A high number of ground pads with short downbonds to the exposed diepad of the QFN48 package was used to achieve a good grounding with low inductance to ground.

The pads for RF output, LO input and serial digital interface were placed at different edges of the chip to minimize coupling and disturbance between these signals.

Each RF output node is connected to two parallel pads and thus two parallel bondwires to reduce the bondwire inductance. Furthermore, the RF output pads do not have any electrostatic discharge (ESD) protection. The ESD diodes would introduce additional parasitic capacitance at the output, thereby reducing the RF performance. Even more important, they would limit the maximum RF output amplitude to the supply voltage $V_{dd,RF}$ plus one diode voltage drop. With an external inductive load, however, the voltage at the open-drain output of the RF-DACs swings around $V_{dd,RF}$. At high output magnitudes the output voltage swing is much larger than a diode voltage drop.
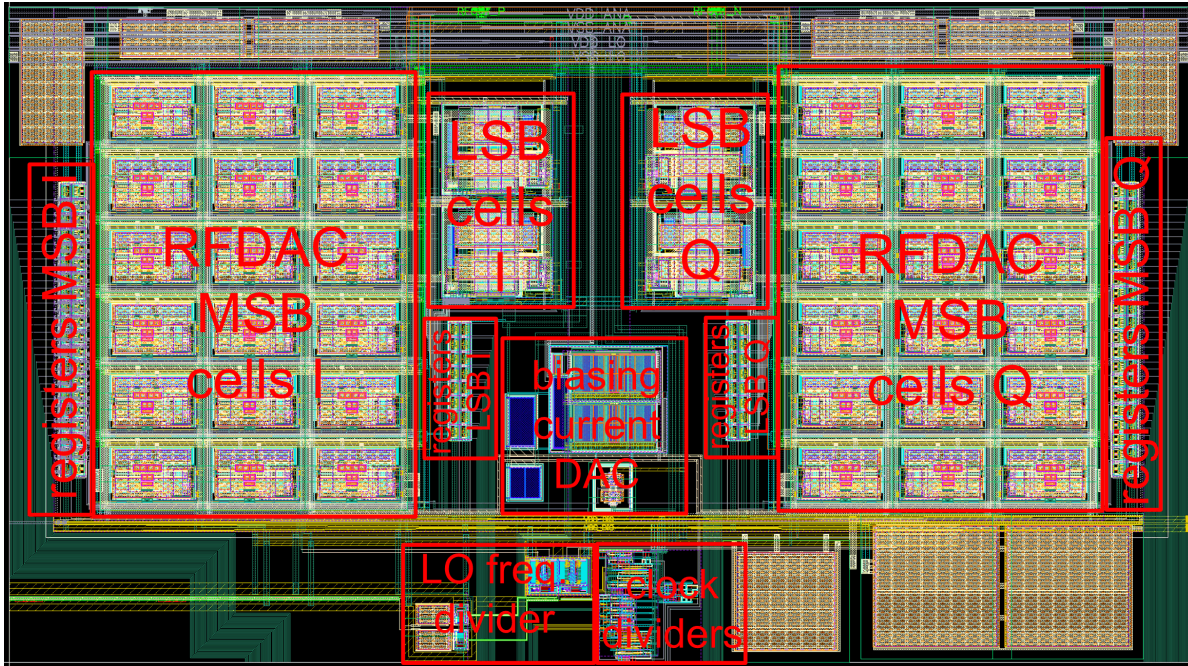
Figure 6.26: Layout of the analog and mixed-signal circuits.

As most of the transistors in the transmitter operate as digital switches, peak currents that are much higher than the average current can occur. As the switching frequencies are quite high, such currents lead to a severe voltage drop over the bondwires to ground. Hence, so-called ground bouncing and ripples on the supply lines can occur. Depending on the bondwire inductance, the ground bouncing can be up to several hundred millivolts. A good grounding and a stabilization of the supply voltages with on-chip decoupling capacitors is therefore essential. In the layout plot of Fig. 6.24 the MIM-capacitors that are used as decoupling capacitors can be identified as large beige rectangles that are located around the RF frontend and the digital blocks. The decoupling capacitors have an overall size of approximately 100 pF.

A close-up view of the RF frontend blocks is shown in Fig. 6.26. The active area of the modulator frontend is approximately $0.4\,\mathrm{mm}^2$. The inphase and quadrature RF-DAC cells are symmetrically placed around the common biasing block. Also, the LO frequency divider output is supplied very symmetrically to the inphase and quadrature RF-DAC cells to achieve a low phase imbalance. A very dense mesh of ground wires is routed between the RF-DAC unit cells to achieve a low-inductance path to the ground pads.

6.10 Simulation results of the RF-frontend

6.10.1 Simulation setup

All analog and RF blocks have been simulated on transistor level using the Cadence Virtuoso Spectre® circuit simulator. For the transistor level simulations of the RF-frontend, the signal generation and digital processing of the input signal have been modeled with the help of Matlab and Verilog-A.

Because of the high number of (parallel) building blocks and the high ratio between baseband signal frequency and RF output frequency, the simulation effort is tremendous, especially when simulating with modulated input signals. Simulations with complete extracted parasitics are almost impossible, due to the high complexity.

Even worse, true mixed-signal simulations need two different simulators for the digital and analog parts. SPICE-like analog simulators have to solve differential equations, while digital simulators are event driven. The required communication between the parallel running simulators makes this type of simulation very slow. To be able to verify the functionality of the complete chip, mixed-signal toplevel simulations have been performed with a simple behavioral model of the analog frontend. This approach is described in section 6.10.3.
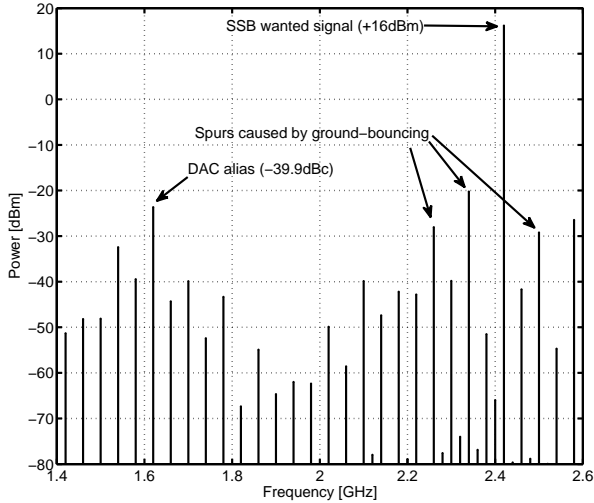
Figure 6.27: Output spectrum of the transmitter for a 20 MHz sinewave SSB input, simulated on transistor level.

6.10.2 Toplevel simulations on transistor level

In Fig. 6.27 the wideband output spectrum of the I/Q vector modulator, observed at node RF_{out} of Fig. 6.2, for a single-sideband sinewave input with a frequency of 20 MHz is shown. The analog sinewave input was translated to a digital input word using an ideal ADC, modeled in Verilog-A. The sampling rate in the simulation is 800 MHz, which is one third of the carrier frequency of 2.4 GHz. The output power of the single-sideband (SSB) wanted signal at 2.42 GHz is +16 dBm into a 100 Ω differential load. Although a mismatch of the LO transistors of 3% has been assumed in the simulation, LO feedthrough at 2.4 GHz and image signal at 2.38 GHz are suppressed by more than 66 dBc. The largest spurious emissions are caused by the DAC alias frequency 800 MHz below the wanted signal at -39.9 dBc. Groundbouncing effects caused by bondwire and package influences lead to unwanted spurs at 80 MHz offset from the wanted signal. To minimize these effects, special care has to be taken to lower ground inductance for layout and packaging, as discussed in the previous section. The total power consumption of the modulator is 211 mW, whereof 133 mW are consumed by the RF-DAC output branch and 66 mW by the LO driver chain.
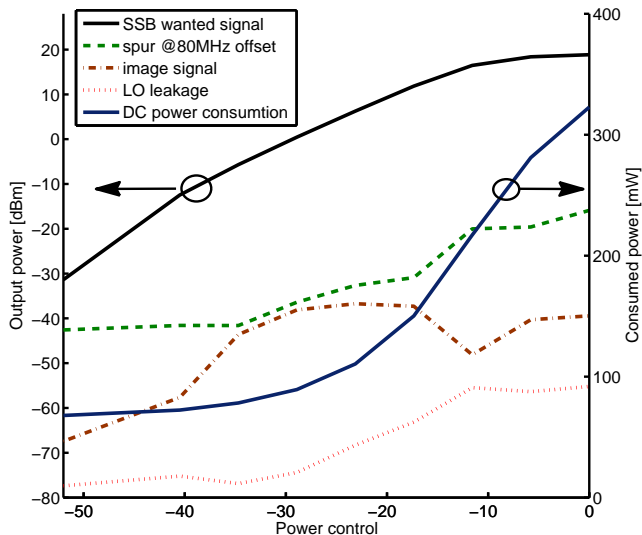
Figure 6.28: Simulated output power of SSB 20 MHz sinewave, LO leakage, image signal and DC power consumption vs. power control.

Fig. 6.28 depicts output power of the SSB signal, LO leakage, image signal and DC power consumption versus power control setting. The input signal is again a 20 MHz sinewave input. Power control is realized by varying the reference currents I_{in1} and I_{in2}. To get a realistic impression of the LO feedthrough, a 3% mismatch of the transistors in the LO switching quad has been assumed. It can be seen that the peak simulated output power is +19 dBm. Thus, the output power is high enough to directly drive an external single-stage PA. The analog/RF part consumes about 300 mW at +19 dBm sinewave output. Power consumption drops to 67 mW for -30 dBm output power.

Fig. 6.29 shows the output spectrum for a 20 MHz OFDM WLAN 802.11g signal, calculated from a 50 µs long transient simulation. The average output power is 0 dBm. Fig 6.29(a) shows the spectrum within a span of 80 MHz around the carrier. It can be seen that the modulator is capable of processing these broadband modulated signals. In Fig. 6.29(b), the wideband spectrum of the same signal is shown. The signal replica at multiples of the 800 MHz sampling frequency can be clearly identified. The second harmonic of the carrier frequency
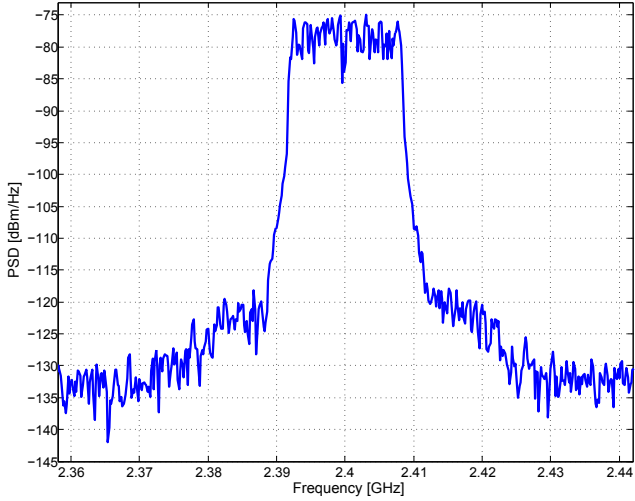
(a) narrowband plot
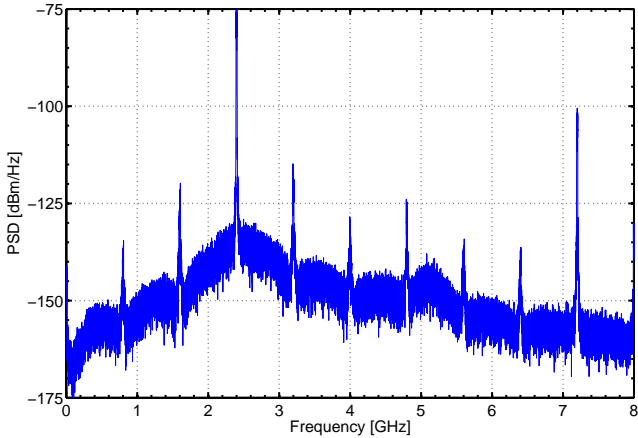
(b) wideband plot

Figure 6.29: Simulated output spectrum of a 20 MHz wide OFDM 64QAM WLAN signal at 0 dBm output power. The RF-frontend has been simulated on transistor level, while the digital input signals have been generated with Matlab and Verilog-A.

at 4.8 GHz is well suppressed due to the differential RF output of the modulator.

To conduct this simulation of the complete RF frontend, the digital modulated input signal has been generated with Matlab and read in from a text file. The simulation time for this simulation was approximately 2 days.

6.10.3 Behavioral simulations

For a mixed-signal chip with high complexity it is indispensable to do sign-off simulations of the complete design before tapeout. The complete functionality and interaction between the digital part, written in VHDL, and the analog frontend have to be examined. However, as it already takes very long to simulate the complex digital or analog blocks alone, it is almost impossible to simulate them together using a mixed-signal simulator. Mixed-signal simulations are quite complicated, as both an event-driven digital simulator and a continuous-time analog simulator, which solves differential equations, are needed. Both simulators have to be synchronized; the analog simulator must be able to trigger events of the digital simulator and vice versa.
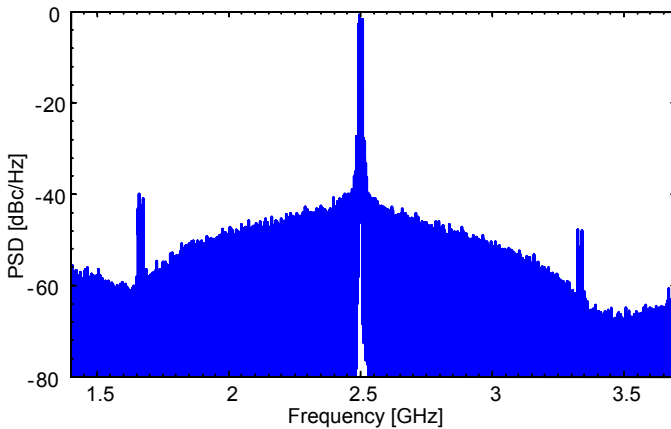
Figure 6.30: Simulated output spectrum of the transmitter for a 20 MHz wide OFDM signal simulated with Verilog-AMS behavioral models.

In order to increase the simulation speed, behavioral models of all analog and RF circuits have been developed. These have been written in Verilog-AMS and lead to a dramatic increase of the mixed-signal simulator speed. The behavioral models enable a functional verification of the interaction between RF frontend and digital building blocks. This type of simulation does not enable

real performance measurements. However, it allows to investigate the effects of different settings for the digital signal processing on the RF output spectrum. One simulation run of the real valued behavioral model with a mixed-signal simulator takes only three hours. It is estimated that one simulation run of the complete chip with the analog frontend modeled on transistor level would require approximately 1360 hours (57 days) to finish. The simulated output spectrum of a behavioral simulation of the complete transmitter for a 20 MHz OFDM signal with a sampling rate of 833 MHz is shown in Fig. 6.30.

Furthermore, a high-level abstraction of the complete RF-frontend using the Verilog-AMS "wreal" datatype as a real-valued model has been developed. The "wreal" datatype permits the utilization of 32 bit floating point numbers for the event-driven simulation. Thereby, the "wreal" datatype has the same amplitude resolution as analog simulations, however, because of the event-driven modeling, they are only calculated at discrete points in time [Joe08]. This enables even faster functional verifications that require the digital simulator only.

7 Measurement Results of the Fabricated Chip

7.1 Fabricated prototype chip

A prototype test chip has been fabricated in TSMC's CMN65LP 65 nm standard low-power CMOS process with analog/RF process options. A micro photograph of the prototype chip is shown in Fig. 7.1. The ASIC has a size of $1.9 \times 1.9 \, \mathrm{mm}^2$. The custom designed mixed-signal RF frontend is located on the right side of the chip. The array of RF-DAC unit cells as well as the RF output wiring and MIM-capacitors for supply voltage decoupling can be clearly identified. The mixed-signal RF frontend has an active area of approximately $0.4 \, \mathrm{mm}^2$.
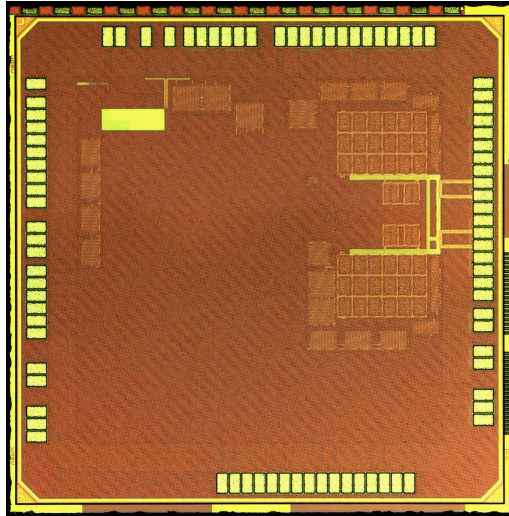
Figure 7.1: Chip photograph of the RF-DAC transmitter protoype in 65 nm CMOS. Chipsize is $1.9 \times 1.9 \, \mathrm{mm}^2$.

The IC has been packaged in a VQFN-48 package with exposed ground paddle. The QFN package has small lead inductances, allowing to bring high-speed digital signals as well as the RF input and output signals in and out of the chip.
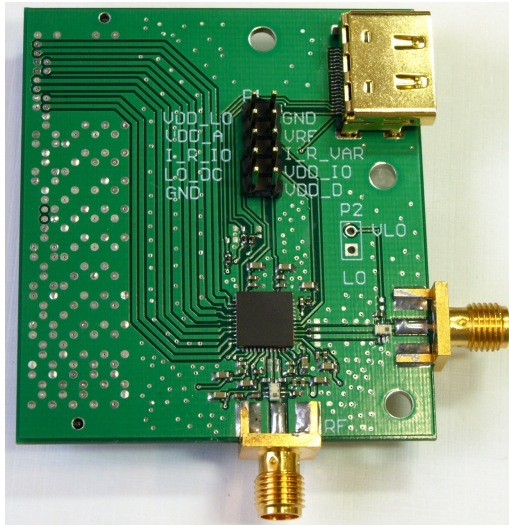
Figure 7.2: Photo of the RF test PCB.

Multiple ground pads of the chip were bonded down on the ground paddle to achieve short ground connections with low inductance. Good ground connections are especially important to reduce unwanted ground bouncing.

7.2 Measurement setup

The test chip has been soldered on a test PCB, which is a standard 4-layer FR4 board with a size of $5.2 \times 5.8 \, \text{cm}^2$. The test PCB is constructed as an FPGA daughterboard, which can be connected via an "FPGA Mezzanine Card" (FMC) connector. A photo of the test PCB is shown in Fig. 7.2. RF output and LO input signals are connected via SMA connectors. The FMC connector is located on the backside of the PCB.

A block diagram of the measurement setup is depicted in Fig. 7.3. The chip requires a relatively low number of external components. All required discrete components are surface mounted devices (SMD) which are soldered on the RF test PCB. Main SMD components are the inductors and capacitors that form the external LC-tank, which acts as load and bandpass filter for the RF-DAC. A balun (balanced-to-unbalanced converter) converts the differential RF-DAC transmitter output signal to a single-ended signal which can be applied to a spectrum analyzer.
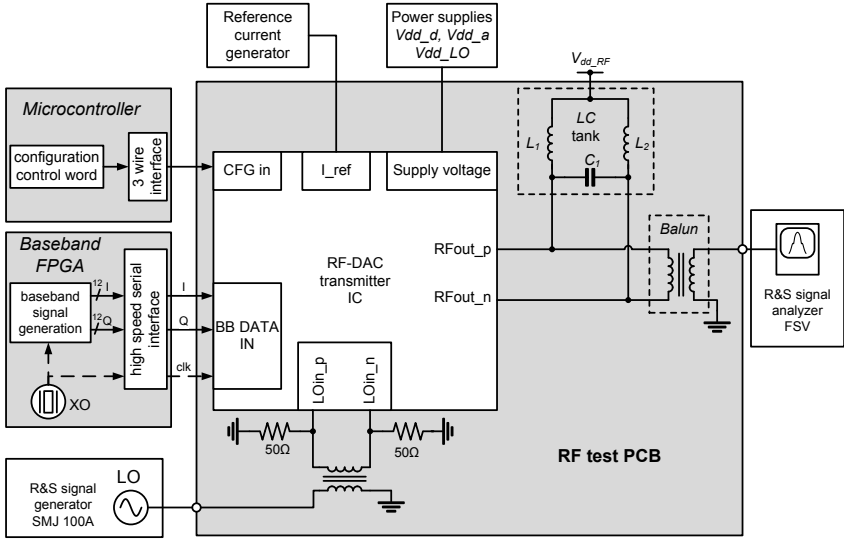
Figure 7.3: Structure of the measurement setup. The RFIC is soldered on a PCB which also contains the required external SMD components. The digital baseband signals are generated on an FPGA.

The local oscillator (LO) signal at twice the RF carrier signal is generated by a signal generator. The single-ended output of the signal generator also has to be converted to a differential signal with a balun, as the RFIC features a differential LO input.

The digital baseband input signals are supplied by a Xilinx Virtex®-6 FPGA. The baseband signals have been generated in Matlab beforehand, and are stored in a lookup table on the FPGA. The FPGA has enough memory to store several tens of thousands 12 bit samples. It communicates with the RFIC over a 1.5 Gbps serial data link, utilizing LVDS signals. As the RFIC chip does not feature a clock recovery PLL, in addition to the I and Q signals, the corresponding clock signal also has to be transferred from FPGA to RFIC. RFIC testboard and FPGA board are connected via an FMC high pin count (FMC-HPC) connector.

All reconfigurable building blocks of the RFIC chip, like the frequency dividers, biasing, digital filters etc., can be programmed using a three-wire configuration interface. The configuration settings are generated using Matlab and subsequently send to a microcontroller via a USB interface. The microcontroller converts the sent data to the right protocol and voltage levels for the three-wire interface and

writes the configuration data to the RFIC.

Apart from the above described components, only power supplies for the different supply voltages and a reference current source are needed for the measurements of the prototype chip. SMD decoupling capacitors are placed close to the RFIC to stabilize the supply voltages.

7.3 Measurement results

Measurements have been conducted with sinusoidal signals as well as modulated signals. Measurements with sinusoidal signals are important as they allow determining the performance of the analog frontend very well and also identifying non-ideal behavior in terms of I/Q mismatch, LO feedthrough and nonlinearities. Measurements with modulated signals allow to test the compatibility with the requirements of actual communications standards. The RF-DAC transmitter prototype has been tested with broadband OFDM signals similar to WLAN and LTE.

7.3.1 Measurements with sinusoidal signals

The measured spectrum of a single-sideband 5 MHz sinusoidal signal with an output power of +15 dBm is shown in Fig. 7.4(a). For this measurement the carrier frequency has been set to 1 GHz and the sampling rate is 500 MHz. The power has been measured with extracted balun and cable loss of 1.8 dB. The LO leakage is -40.6 dBc, image suppression is -30.1 dBc. All other unwanted spurs that can be identified in Fig. 7.4(a) are suppressed by more than 39 dBc. All relatively large spurs are located at multiples of the 5 MHz baseband signal and are caused by intermodulation due to nonlinearities as discussed in section 2.2.4 and also by ground-bounding effects.

The measurement results for the same 5 MHz sinusoidal signal with a reduced output power of +10 dBm are shown in Fig. 7.4(b). The output power is decreased by lowering the biasing currents in the RF-DAC cells. Because of the better linearity and reduced ground-bouncing at this lower output power level the unwanted emission are clearly reduced to levels below 45 dBc. The only exception is the image signal, whose strength is determined by the mismatch between inphase and quadrature path and which remains almost unchanged at -30.6 dBc.

In the two measurements of Fig. 7.4 it can be seen that the noise floor is below -110 dBc. The measured noisefloor is limited by the resolution bandwidth and the high input attenuation of the spectrum analyzer, which is required for the strong input signals of more than +10 dBm. The truncation noise of the RF-DAC is even below this level and exceeded by the noise floor of the spectrum analyzer.
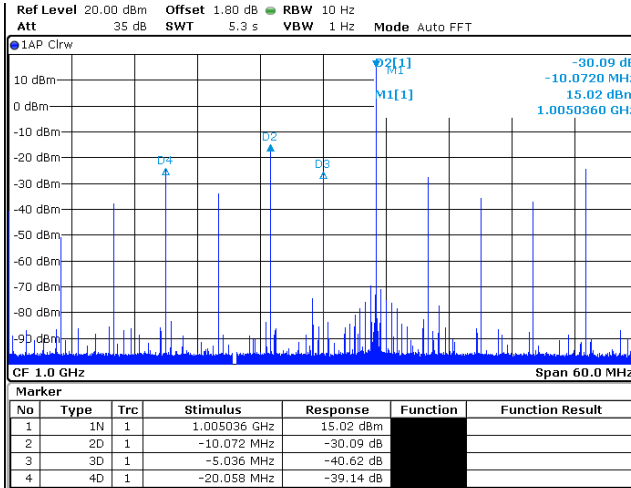
(a) +15 dBm sinewave
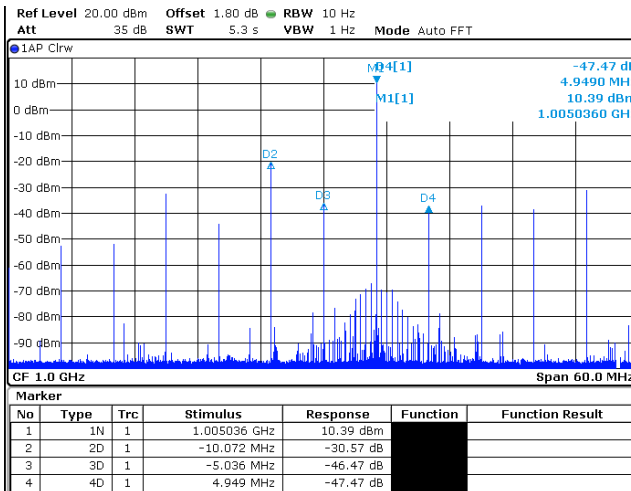
(b) +10 dBm sinewave

Figure 7.4: Output spectrum of a 5 MHz sinusoid at 500 MHz sampling rate with different output power settings.
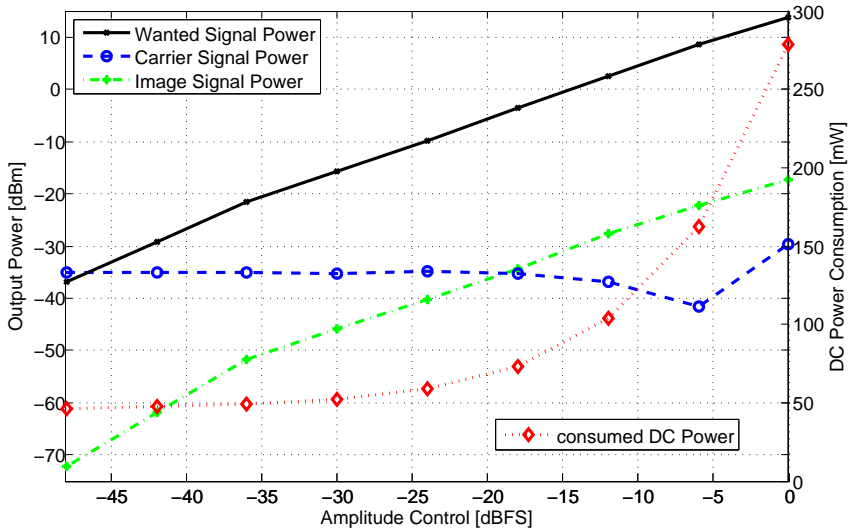
Figure 7.5: Measured output power of a 5 MHz single-sideband sinusoid, image signal and LO feedthrough versus baseband signal amplitude. Also, the DC power consumption of the modulator is plotted. The carrier frequency is 1 GHz.

The relatively small spurs which are most prominent around the wanted signal and suppressed by more than 80 dBc are caused by the noise which is generated within the measurement setup. For example, DC-DC converters on the FPGA board generate quite strong disturbances with frequencies of several hundred Kilohertz. These low frequency disturbances are picked up by the supply lines of the analog voltage and RF-DAC reference current and upconverted to RF by the RF-DAC. These interferences could probably be further reduced by an improved measurement setup with better shielded supply lines and a better separation between FPGA board and RFIC testboard. This, however, is not possible with the current measurement setup where the RFIC testboard is directly attached as a daughterboard to the FPGA board, connected via the previously mentioned HPC connector.

Measurements vs. amplitude control

In Fig. 7.5 the behavior of the 5 MHz sinusoidal signal in dependence of the digital baseband signal amplitude is shown. For this measurement, the signal

	Power consumption [mW]			
	Digitally contr. LO driver		LO driver always on	
	0 dBFS	-48 dBFS	0 dBFS	-48 dBFS
RF-DAC output branch	214.3	0.8	214.6	0.8
Biasing	23	23.3	23	23.3
LO driver chain	41.3	22.3	57.3	56.4
total	**278.6**	**46.4**	**294.9**	**80.5**

Table 7.1: Power consumption of the analog and RF blocks at different digital baseband signal magnitudes for a fixed biasing and +13.8 dBm output power with full scale amplitude.

amplitude is scaled by shifting the digital word by one bit towards the LSB for each amplitude control step. With each step the digital baseband signal amplitude is reduced by a factor of two. The wanted signal output power scales very linearly by 6 dB per amplitude control step over a dynamic range of 48 dB, as expected for an amplitude resolution of 8 bit. The biasing conditions have been set to a peak output power of 13.8 dBm for a full-scale sinusoidal signal. The image signal scales correspondingly to the wanted signal and is suppressed by approximately 30 dBc over the complete amplitude control range. The LO leakage remains relatively constant at a power of approximately -35 dBm. It is increased to -22 dBm (not shown in Fig. 7.5) if the LO drivers of inactive RF-DAC unit cells are configured to be constantly in "on" state, instead of being controlled by the output magnitude, as described in section 6.5.

The DC power consumption of the modulator drops from 278 mW for a full scale sinusoidal output to 46 mW at -48 dBFS, which shows the effectiveness of the power saving mechanisms for low signal magnitudes, namely completely turning of the current-flow in inactive RF-DAC cells as well as deactivating the corresponding LO driver cells. The power consumption of the different modulator building blocks – RF-DAC output branch, biasing circuits, and LO driver chain including the 2:1 frequency divider – for different amplitudes and different LO driver control settings is summarized in table 7.1. As can be seen, the RF-DAC output branch dominates the total power consumption for large signal amplitudes, while biasing and LO driver chain dominate for small amplitudes.

	Power consumption [mW]		
	P_{out}=+16 dBm	P_{out}=0 dBm	P_{out}=-20 dBm
RF-DAC output branch	358	42	3.7
Biasing	29.9	5	2.1
LO driver chain	29.2	29.5	29.4
total	**403.7**	**76.5**	**35.2**

Table 7.2: Power consumption of the analog and RF blocks at different output power settings for a full-scale sinusoidal signal. The power control is done by scaling the bias currents of the RF-DAC unit cells.

Power control measurements

Besides reducing the digital baseband signal magnitude, the output power of the RF-DAC transmitter can also be controlled by changing the bias currents in the RF-DAC unit cells, without having to sacrifice converter resolution. The implementation of the RF-DAC bias control has been described in section 6.7. The power control of the transmitter is not fast enough to do amplitude modulation. Rather, it is typically used to set the average output power level, e.g. in dependence of the distance and channel quality between handheld device and basestation.

In Fig. 7.6 the output power of the RF-DAC versus power control is shown for a 5 MHz single-sideband, full-scale sinusoidal signal at 1 GHz carrier frequency. Also, the image signal and LO feedthrough, as well as the power consumption of the modulator are shown. In Fig. 7.6(a) the signal power is measured while the LO driver is dynamically controlled by the digital signal magnitude, in Fig. 7.6(b) all LO driver cells are constantly running.

The peak output power which could be measured with a sinusoidal signal is more than +16 dBm, which is the highest reported output power for an RF-DAC based modulator. It is about 14 dB more than reported in [Elo+07] and 24 dB more than in [JS07]. At the same time, the active area of the analog blocks is only 0.4 mm^2 and thus distinctively smaller than the values reported in [Elo+07] and [JS07].

The power control has a dynamic range of almost 90 dB; the wanted signal power can be decreased down to -70 dBm. The image signal power scales with the wanted signal power until it reaches -80 dBm. The minimum LO feedthrough levels that can be achieved are -32 dBm if the LO is dynamically controlled, or -24 dBm if it is constantly running.
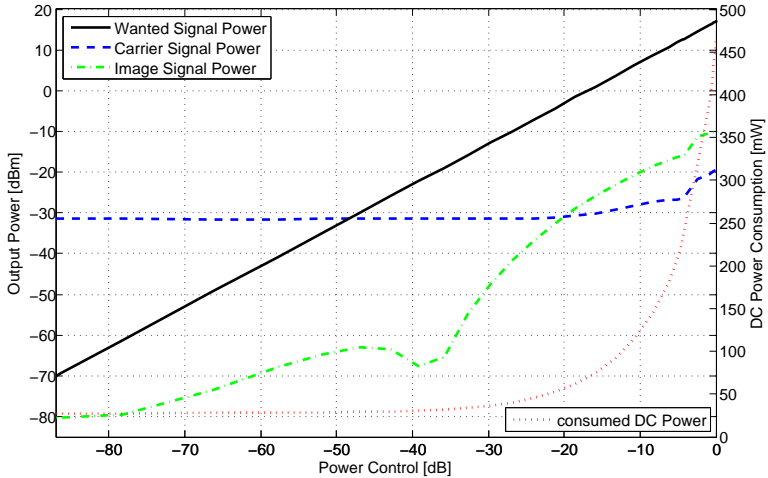
(a) with amplitude controlled LO buffer
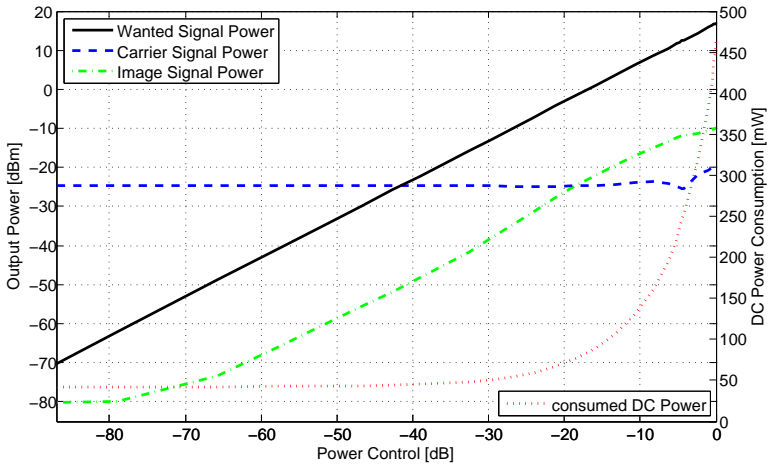
(b) LO constantly running

Figure 7.6: Measured output power of a 5 MHz single-sideband sinusoid (full-scale), image signal and LO feedthrough versus power control. Also, the DC power consumption of the modulator is plotted. The carrier frequency is 1 GHz.

In table 7.2 the measured power consumption of the different modulator blocks is given for different output power levels. The total power consumption drops from approximately 400 mW at the peak RF output power of +16 dBm to 35 mW at -20 dBm output power. In difference to the case of Fig. 7.5 and table 7.1, where the digital signal magnitude is scaled, here the LO driver power consumption stays constant, while the power in the biasing blocks scales with power control. The overall power efficiency of the modulator at +16 dBm output power is more than 10%.

If all LO drivers are continuously running it limits the minimum modulator power consumption to 42 mW. By switching off the LO driver of inactive RF-DAC unit cells, the power consumption can be reduced by 15 mW.

Issues detected during the measurements

The LO input 2:1 frequency diver can be operated up to input frequencies of approximately 5 GHz and respective output frequencies up to 2.5 GHz which is slightly lower than the maximum simulated output frequency of 2.7 GHz. This degradation is caused by underestimated parasitic capacitances at the LO driver output network which increase the load of the frequency divider. Unfortunately, the LO frequency divider also does not work as expected for input frequencies between approximately 2.8 GHz and 3.6 GHz. Measurements reveal that the frequency divider either oscillates or divides by a factor of four instead of the wanted factor of two in this input frequency range. This behavior is probably caused by disturbances due to ground-bouncing and an imperfect, slightly unsymmetrical load at the output of the differential frequency divider. Improved ground wiring, a more symmetrical load, additional buffer stages and better decoupling of the power supplies should solve this problem. However, it is difficult to reproduce this unwanted behavior in the circuit simulations.

Because of issues in the implementation of the dynamic clock domain conversion (CDC) block, one of the quadrature I/Q paths does not work properly above RF carrier frequencies of 1.8 GHz. Thus, only double-sideband sinusoidal signals can be transmitted at these frequencies, making a comprehensive analysis of the RF frontend performance at these high frequencies impossible. A modified CDC implementation should fix this issue for future implementations.

Furthermore, a perturbation of the digital blocks for high modulator output power levels and high RF carrier frequencies can be observed. These are caused by ground-bouncing and substrate noise. An even better shielding by putting sensitive circuits into deep n-wells and reducing the ground-bouncing by even more bondwires, wider and possibly shorter ground wires on the chip, and better decoupling of the supply voltages should reduce this issue.
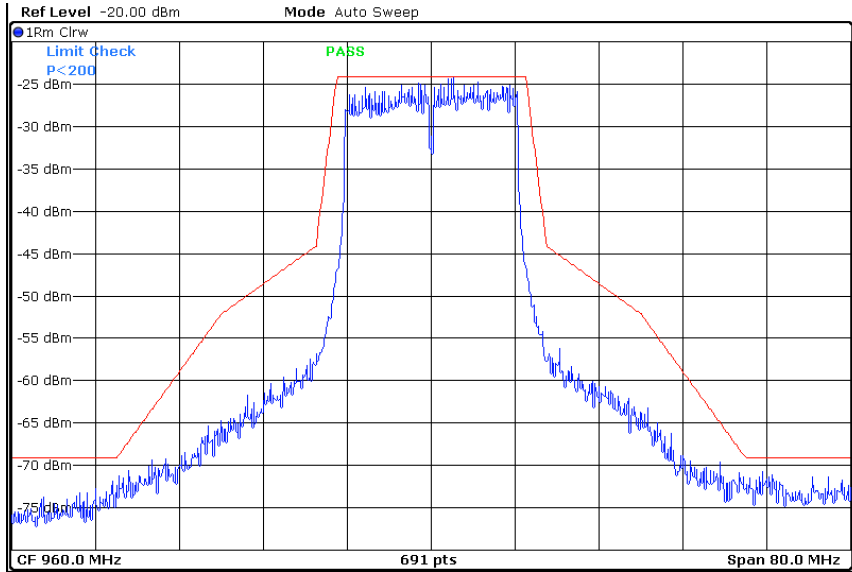
Figure 7.7: Output spectrum of a 20 MHz wide 64QAM OFDM signal at 480 MHz sampling rate. The IEEE 802.11n spectral mask is fulfilled.

7.3.2 Measurements with modulated signals

The transmitter is capable of processing broadband high data rate signals up to 40 MHz wide 64QAM OFDM signals as shown in Fig. 7.7 and Fig. 7.9.

Fig. 7.7 shows the output spectrum of a 20 MHz OFDM WLAN signal. The total analog power consumption for this signal at approximately -3 dBm output power is 65 mW. This relatively low power consumption for a high peak-to-average power ratio signal can be achieved by using the techniques for power savings at low signal magnitudes, as described in sections 6.4.2 for the RF-DAC and in section 6.5 for the LO driver chain. The IEEE 802.11n spectral mask is fulfilled. The adjacent channel sidelobes between 10 and 20 MHz offset from the carrier signal are around 12 dB below the spectral mask, allowing for nonlinearities of an external PA subsequent to the RF-DAC modulator IC.

The wideband output spectrum of the same signal is shown in Fig. 7.8. The DAC signal replica at 480 MHz offset is quite well suppressed by more than 50 dBc. In addition to the replica signal, a narrowband clock signal feedthrough which is about 10 dB higher than the replica signal can also be recognized.

The unwanted emissions requirements of the WLAN spectral mask, however,
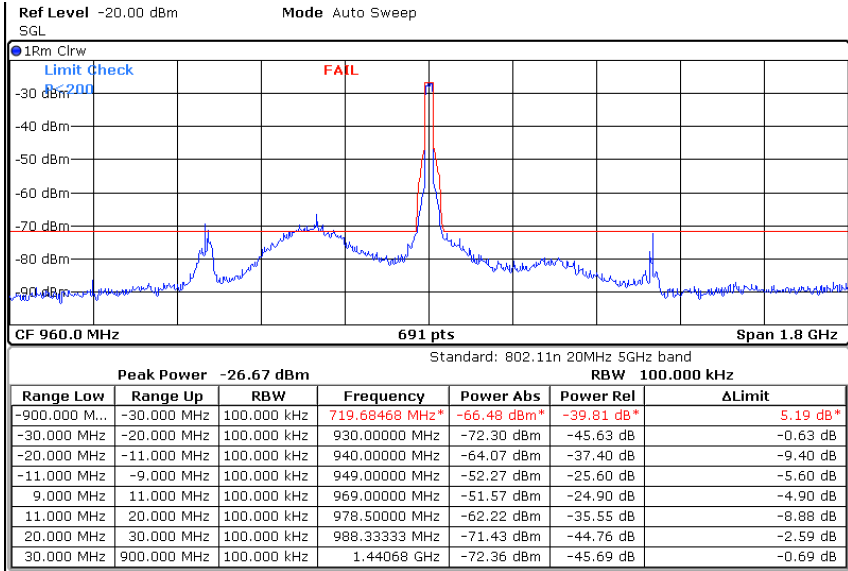
Figure 7.8: Wideband spectrum of the same 20 MHz wide 64QAM OFDM signal.

are not met by some dB at some frequencies which are located below the wanted frequency. The overly high unwanted emissions at these frequencies are caused by the LO-derived clock signals for the digital signal processing blocks. These strong clock signals, running at 120 MHz and 480 MHz for the measurements of Fig. 7.8, lead to crosstalk to the biasing blocks of the RF-DAC and the supply voltages of the analog blocks as well as an increased ground-bouncing. The feedthrough of the 480 MHz RF-DAC clock signal to the RF output can be clearly seen in the measurements. A mixing of these disturbances with the OFDM signal leads to unwanted broadband emissions which can be identified around 720 MHz. If the clock rates are lowered in the measurements, the power level in the frequency region with the highest unwanted emissions is reduced as the impact of ground-bouncing and crosstalk scales with clock frequency. On the other hand, a reduced RF-DAC clock rate also leads to signal replica closer to the wanted signal and an increased quantization noise floor, as expected from theory. The problem of unwanted emissions due to groundbouncing and crosstalk of the clock signals could be solved in future implementations by further improving the grounding of the circuits and a shielding of the clock signal wires in the layout.
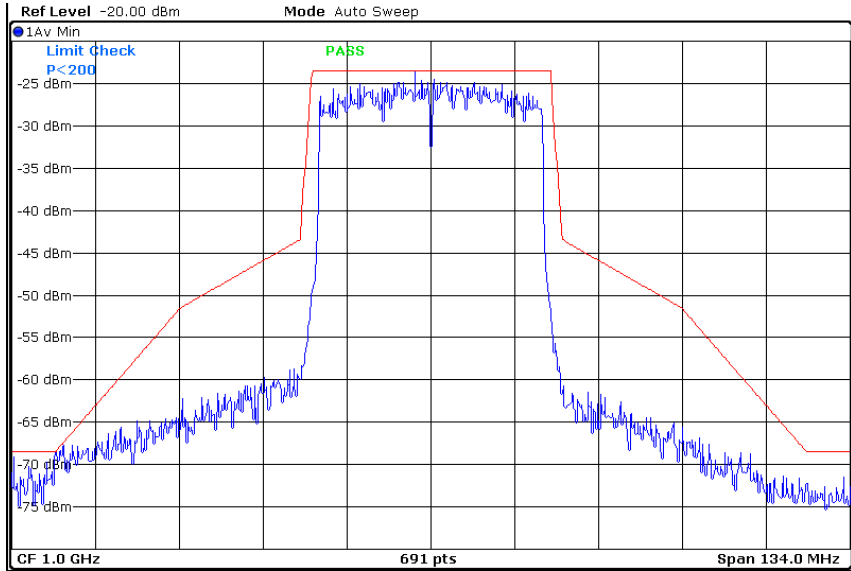
Figure 7.9: Output spectrum of a 40 MHz wide IEEE 802.11n "turbo-mode" WLAN signal at 500 MHz sampling rate.

The unwanted emissions above the wanted signal frequency are well below the WLAN spectral mask, with the exception of the LO frequency at 1920 GHz. An overly strong signal at this frequency is caused by an insufficient shielding between the LO reference input and the RF output on the RF test PCB. This issue could be relatively easily solved by an improved PCB design.

Fig. 7.9 shows the output spectrum of an OFDM IEEE 802.11n "turbo-mode" WLAN signal with a doubled channel bandwidth of 40 MHz, proving the transmitter's capability of processing very broadband signals. The maximum signal bandwidth of the prototype implementation is mainly limited by the maximum datarate of the serial interface between FPGA and RFIC. For this measurement, the 12 bit wide baseband signal has been generated with a sampling rate of 100 MHz, yielding a oversampling rate of only 2.5. For such a broadband signal, the *sinc* frequency response of the interpolation filters which are required for the conversion from 100 MHz to 500 MHz sampling rate, as discussed in section 5.5.2, already lead to a significant damping of the wanted signal by some dB at the channel edges. Furthermore, a relatively slow roll-off of the output noise leaves very little margin from the spectral mask limit at around 60 MHz

137

below the carrier frequency.

The spectral shape of the measured signals indicates a good signal quality. However, EVM measurements of OFDM modulated signals could unfortunately not be conducted with the existing measurement setup. Enhanced signal generation and signal measurement equipment is required for this task. Conducting EVM measurements hence remains part of future investigations.

8 Conclusions and Outlook

8.1 Conclusions

In this thesis a "direct-digital" transmitter for wireless communications, based on an RF-DAC has been presented. The RF-DAC unites D/A converter and upconversion mixer functionality in a monolithic building block which features a digital baseband input and an analog RF output. Thereby, the RF-DAC based transmitter allows to eliminate all analog baseband blocks like filters or VGAs. As digital signal processing blocks can be much easier reconfigured for different requirements compared to analog circuits, this approach enables the implementation of a transmitter which supports different communication standards, different modes (e.g. signal bandwidths) and operation in different frequency bands. It therefore is a step towards a software defined radio.

The implemented transmitter shall support broadband, high-data-rate communication standards such as WLAN and 3GPP LTE. These modern standards are based on OFDM. The modulated signals are distributed on several parallel subcarriers which are equally spaced around a common RF carrier signal, thereby creating one broadband signal. This technique, in connection with high order modulation schemes, leads to very high data rates as well as good bandwidth efficiencies. However, as discussed in chapter 2, OFDM poses exacting demands on the performance of the RF transmitter frontend as high linearity is needed and very large peak to average power ratios (PAPR) of more than 10 dB have to be supported.

The transmitter frontend of a communications device for consumer applications should be as highly integrated into a monolithic chip as possible to gain low production costs and low required area in a mobile device. Today's transmitter implementations typically feature an external power amplifier (PA) which is implemented in a specialized GaAs or SiGe technology to obtain the high required output power and linearity. Within the framework of this thesis it has been investigated what output power levels can be realized with a singe-chip nanoscale CMOS PA solution. Therefore, two PAs with different architectures have been implemented in a 130 nm standard CMOS technology. The implementation details are presented in chapter 3. It is found that saturated peak output powers of more than 27 dBm can be achieved. These power levels are sufficient for connectivity standards with either relatively low output power levels like Bluetooth or WLAN or with low requirements on the RF frontend linearity, like

DECT. Nonetheless, it is concluded from the obtained results as well as from literature that it is not possible to achieve the requirements of cellular standards such as UMTS or LTE that demand high linear output power levels in the order of +33 dBm with a PA which is integrated into the transceiver IC in today's standard CMOS technology.

Hence, for a transmitter which is intended to support cellular standards an architecture with a fully integrated modulator plus an external PA has to be chosen. An RF-DAC based topology seems to be an excellent architecture for broadband, reconfigurable transmitters in nanoscale CMOS. Several earlier published digital-RF architectures, which are akin to the RF-DAC approach, are reviewed in chapter 4. As the RF-DAC unites D/A converter and upconversion mixer in a single building block and eliminates all analog baseband signal processing it is not possible to implement an analog reconstruction filter at the DAC output. Therefore, unwanted DAC output signal replicas at multiples of the DAC sampling rate are upconverted to RF and emitted by the antenna. These unwanted emissions must be very small in order to not disturb parallel running radios operating at the respective frequencies. Various techniques such as a high DAC oversampling ratio, high DAC resolution, and $\Delta\Sigma$ noise shaping in connection with bandpass-filtering at the RF output may help to reduce the unwanted emissions. In addition, the zero-order hold behavior of the DAC has a *sinc* frequency response which creates notches at multiples of the sampling rate, thereby helping to suppress DAC signal replicas.

A transmitter architecture has to be found which may achieve the performance that is required by the different supported communication standards and frequency bands and takes into account the special characteristics of the RF-DAC. Maximum spurious emission limits have been calculated and a Matlab system simulation has been set up to evaluate the influence of architectural choices and the behavior of different building blocks on the overall transmitter performance. In chapter 5 it is found that a polar modulator architecture does not provide enough bandwidth for very broadband signal transmission. Instead, a quadrature I/Q modulator is needed. The RF-DAC modulator must have a resolution of 9 bit for each quadrature path to attain the system requirements. Preceding the RF-DAC the digital input signal has to be oversampled up to 800 MHz. A $\Delta\Sigma$ modulator allows to do noise shaping to improve SNR in the signal band. Moreover, additional notches in the noise transfer function of the $\Delta\Sigma$ modulator reduce the noise at especially critical frequency bands, such as the duplex frequency band in FDD systems. An element selection logic allows to do mismatch shaping and thereby reduces the transmitter performance degradation caused by analog non-idealities.

The circuit implementation of the mixed-signal and RF frontend is discussed in chapter 6. Particularly, a novel RF-DAC implementation is presented. The RF-DAC consists of several parallel unit cells. It is implemented as a segmented

architecture with four binary weighted LSBs and four unary weighted MSBs. Thereby, low glitches can be obtained while remaining a relatively low wiring complexity. The sign of the output signal can be set by a differential transistor pair which steers the output current either to the positive or negative DAC output. The presented RF-DAC architecture is optimized for especially high output power levels up to +16 dBm. This is achieved by a circuit architecture which requires very low voltage headroom and thus leads to a high output voltage swing. Furthermore, when operated at small signal amplitudes this novel architecture consumes less current than previously published implementations, as unit cells which are inactive can be completely switched off. Also, the LO driver chain which amounts perceptible to the total power consumption of the RF frontend is optimized for reduced current consumption at small signal amplitudes. This can be achieved as every RF-DAC MSB unit cell has its own LO driver. If a unit cell is inactive, also the corresponding LO driver can be deactivated.

The RF-DAC transmitter has been implemented in a 65 nm standard CMOS technology. The size of the prototype chip is 1.9x1.9 mm^2. The analog and mixed-signal parts have an active area of approximately 0.4 mm^2.

Measurements of the prototype chip reveal that a peak output power up to +16 dBm for a single-sideband sinusoidal signal is possible with the implemented RF-DAC based transmitter. This is the highest reported output power for a direct-digital transmitter. The LO carrier leakage is less than -40 dBc, the image signal is suppressed by more than 30 dBc. The power consumption of the modulator for the +16 dBm sinusoidal signal is 400 mW.

The amplitude of the RF-DAC output can be varied linearly over the complete dynamic range of 48 dB, as expected for 8 bit amplitude resolution. Due to the previously described power saving techniques of RF-DAC and LO driver at low output amplitudes, the power consumption decreases by a factor of six for -48 dBFS amplitudes. In addition to the amplitude control, the output power can be controlled via the biasing current of the RF-DAC over a dynamic range of almost 90 dB. However, at very low output signal power levels, the LO feedthrough is larger than the wanted signal.

The RF-DAC transmitter is capable of processing 64QAM-modulated high-data-rate OFDM signals up to 40 MHz channel bandwidth and fulfills the WLAN IEEE 802.11n spectral mask around the carrier. Due to the high resolution and sampling rate of the transmitter, spurious emissions at multiples of the DAC sampling rate are well suppressed in the measurements. The first signal DAC signal replica for a sampling rate of 500 MHz is suppressed by more than 50 dBc. However, due to high ground-bouncing and clock-feedthrough, unexpectedly high spurious emissions at multiples of the clock signals of the digital circuits can be identified in the output spectrum.

8.2 Outlook

A further improved layout could help to decrease ground-bouncing and clock-feedthrough to the RF-output and biasing circuits. Also, the LO feedthrough could be further decreased by an improved shielding of the LO driver chain circuitry and signal wires.

The presented RF-DAC transmitter architecture could gain from a technology scaling from the 65 nm CMOS node to even smaller feature sizes such as 40 nm, 28 nm or even below. The main benefits can be expected in the digital blocks, as their area and power consumption decreases with transistor scaling, while their speed increases. This enables even more complex digital signal processing and also higher sampling rates of the RF-DAC. The performance of the RF-DAC will not suffer from the feature size shrink as most transistors in the RF-DAC architecture act as switches, preventing a performance degradation which could be expected for analog circuits. The sampling rate of the DAC could even be increased. A much smaller area of the RF-DAC itself, however, cannot be expected for smaller technology nodes as the linearity of the DAC is largely determined by the chosen transistor length, as discussed in section 6.4.2.

The RF-DAC still contains some truly analog components like the current mirror based biasing circuitry, which permits an accurate definition of the unit cell output currents. An even more digital RF-DAC implementation, looking somewhat similar to the architectures that have been presented in section 4.1.4 and section 4.1.5, would eliminate these remaining analog circuits and, as a result, simplify the circuit implementation and the portability to different technology nodes. The lower accuracy and thus resolution of a fully digital implementation of the RF-DAC, however, somehow must be compensated, e.g. by some kind of digital predistortion.

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