Testing Report

Title：ADF4106 Testing Report

Date：Jan, 2011

Author：CAST

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1. Testing Purpose

Be Familiar with the performance of ADF4106.
Test the performances of phase noise and lock time.
Compare the testing results with simulation results of ADIsimPLL.

2. Testing Conditions

Indoor laboratory environment

3. Testing System Frameworks

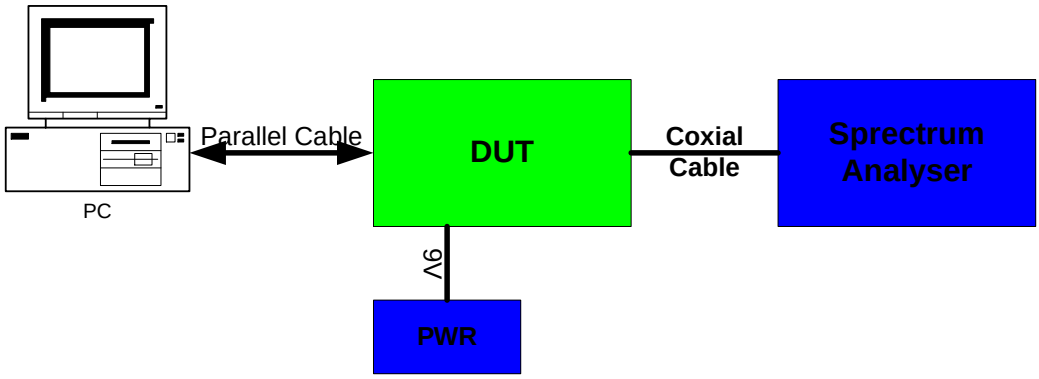

Figure 1 Testing System Frameworks

4. Testing Equipments

Equipment	Model	Manufacturer	Quantity
PC	OS: Windows XP Professional Version 2002, Service Pack 3	DELL	1
Spectrum Analyzer	PSA Series, E4443A	Agilent	1
Digital Oscilloscope	DS1204B	RIGOL	1

Table 1 Testing Equipments

5. Testing Schematics

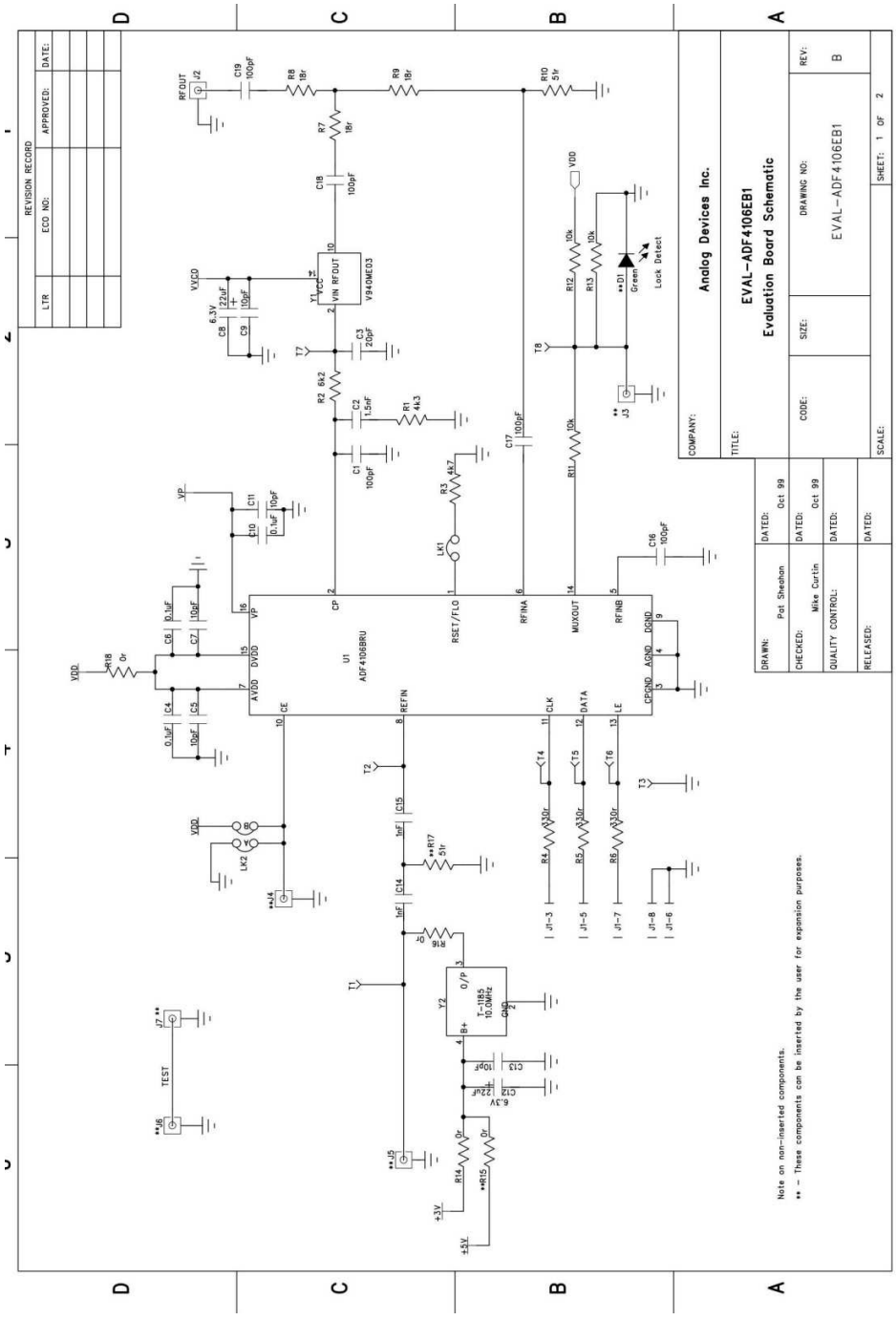

Figure 2 Testing Schematic_1

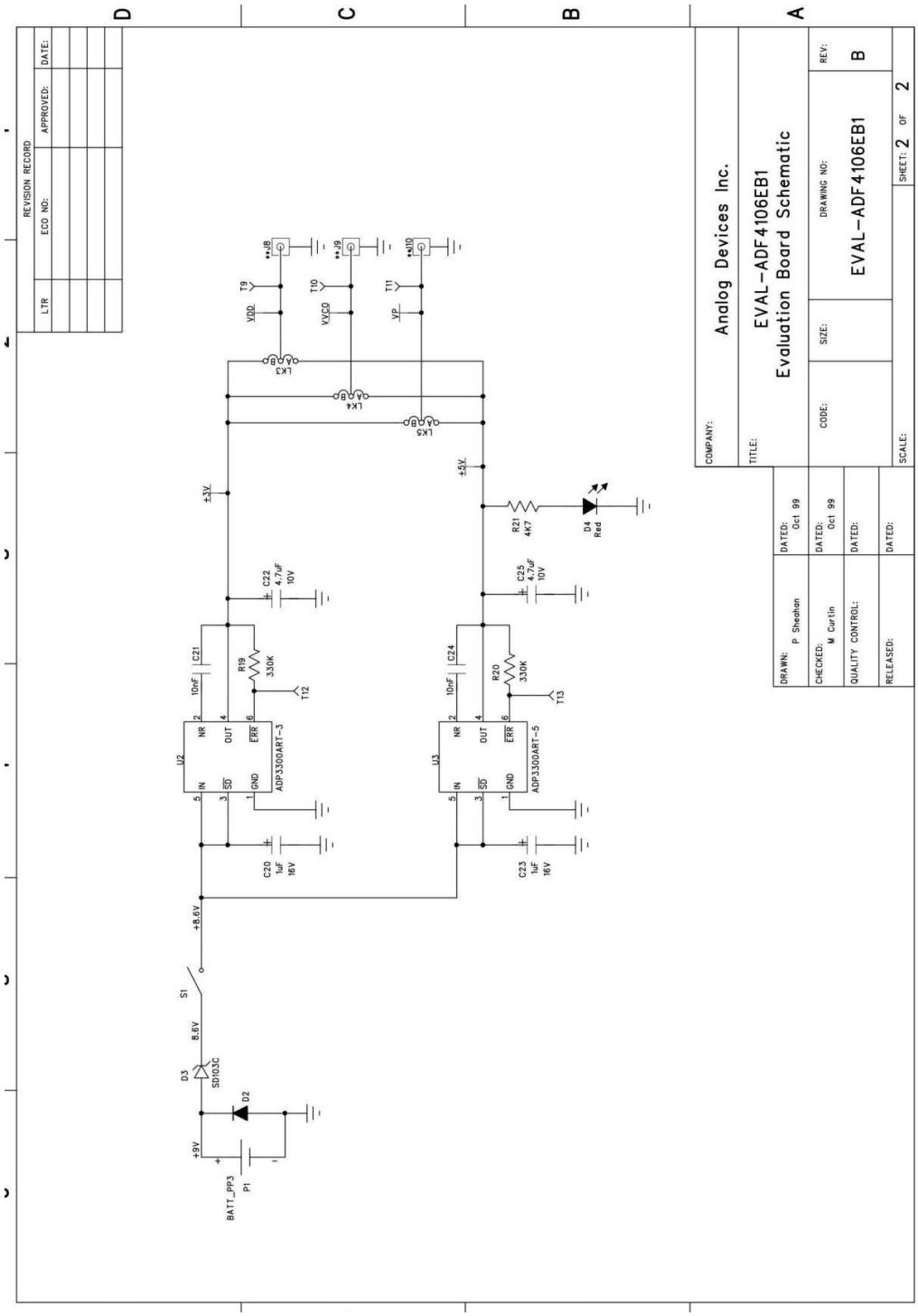

Figure 3 Testing Schematic_2

6. Testing Procedures

- Open the package of EVAL-ADF4106EB1 and read the instructions carefully.
- Install the EVB software into PC and connect the EVB board to PC with the cable included within the EVB package.
- Power on the EVB board with 9V DC battery.
- Set Power Switch S1 to ON and Power Indicator D4 lights.
- Connect RFOUT SMA Connector J2 on the EVB board to the spectrum analyzer through RF cable.
- Input design parameters to the EVB software and capture the testing results using spectrum analyzer and digital oscilloscope.
- Simulate the PLL circuit according to the EVB testing parameters.
- Compare the simulation results with testing results.

7. Testing Results

Before the test, the testing results of ADF4106 EVB are simulated by ADIsimPLL V3.30. The simulation and testing PLL parameters are set as below.

Reference Input Frequency	10.000MHz
RF Output Frequency	5.8GHz
PFD Frequency	1MHz
CP Current	2.5mA/5.0mA
Loop Bandwidth	50kHz
Loop Phase Margin	45 degrees

Table 2 Testing Parameters

7.1 Phase Noise

The EVAL-ADF4106EB1 is set to output the frequency of 5.8GHz with the power of -13dBm.

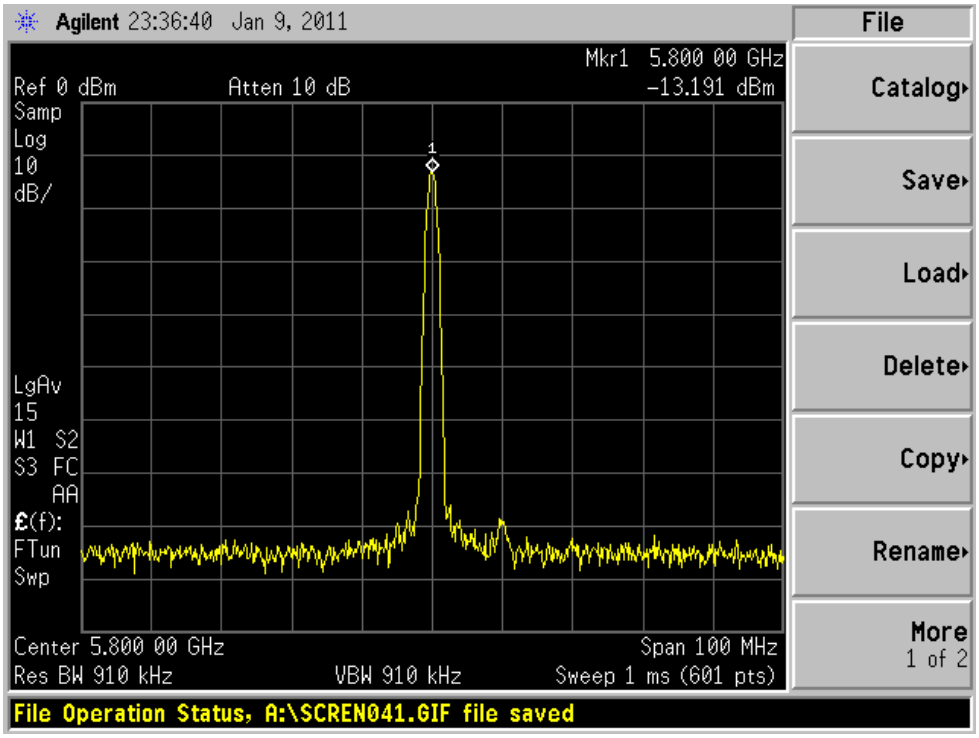

Figure 4 -13dBm@5.8GHz Output Spectrum

After PLL locking well, MUXOUT is set to Digital Lock Detect (DLD) and the output is measured as 2V. Then, MUXOUT is set to R-Counter Output. Measure the output with digital oscilloscope, the output wave is attached as below.

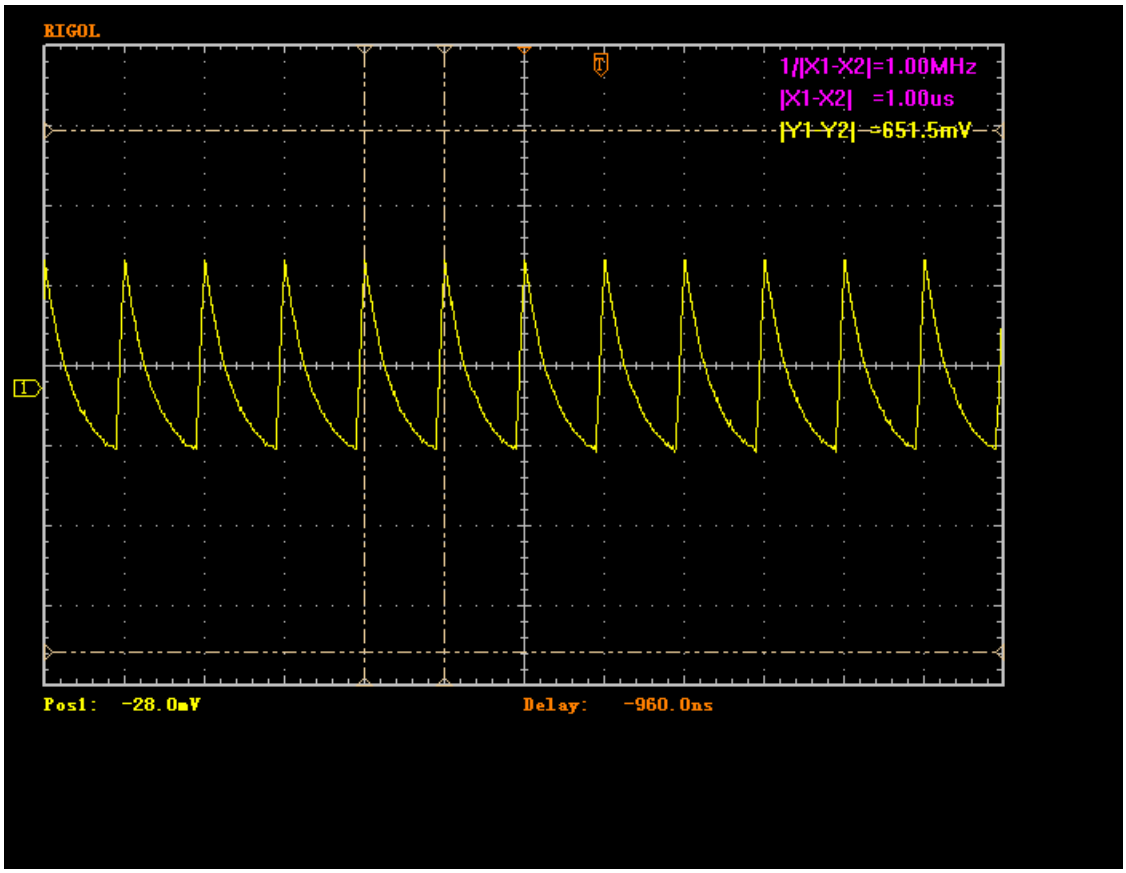

Figure 5 R-Counter Output of MUXOUT when PLL locks

The frequency of the pulse of MUXOUT output is 1MHz which equals to Phase Frequency Detector frequency.

The phase noise is tested as below.

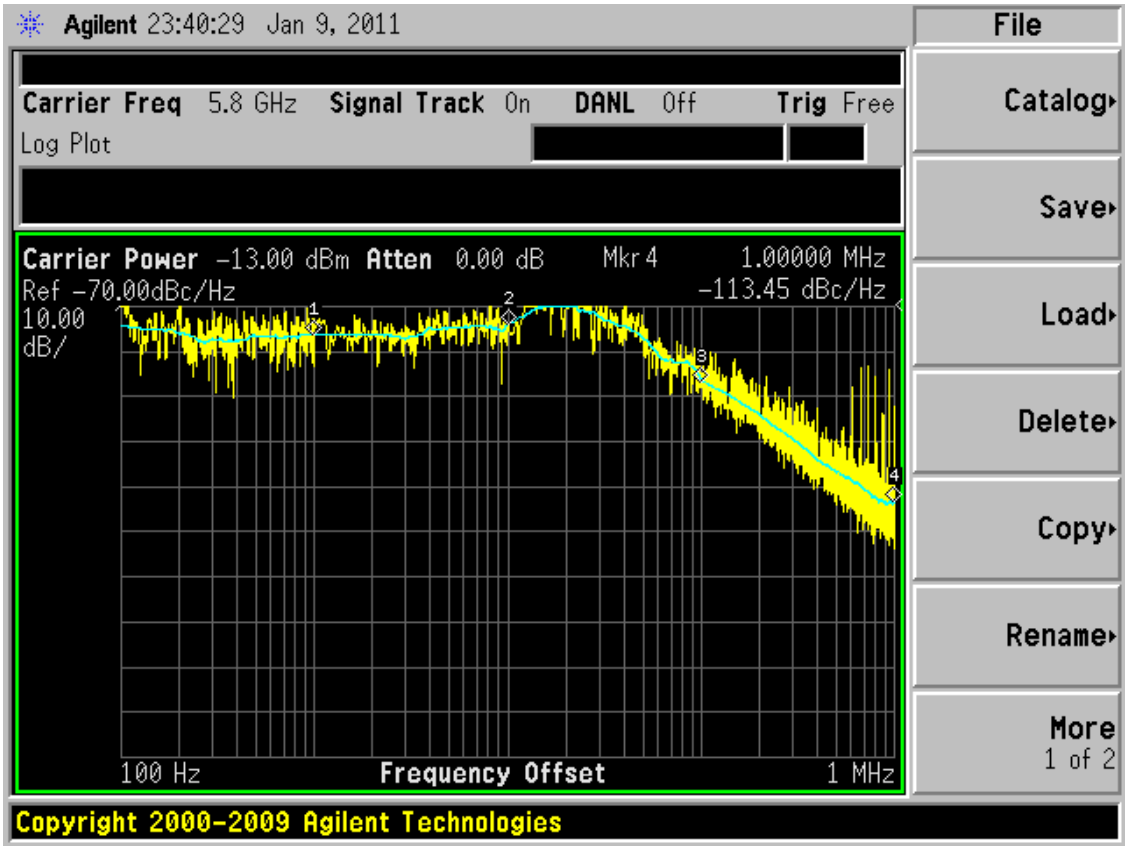

Figure 6 Phase Noise Spectrum of -13dBm@5.8GHz

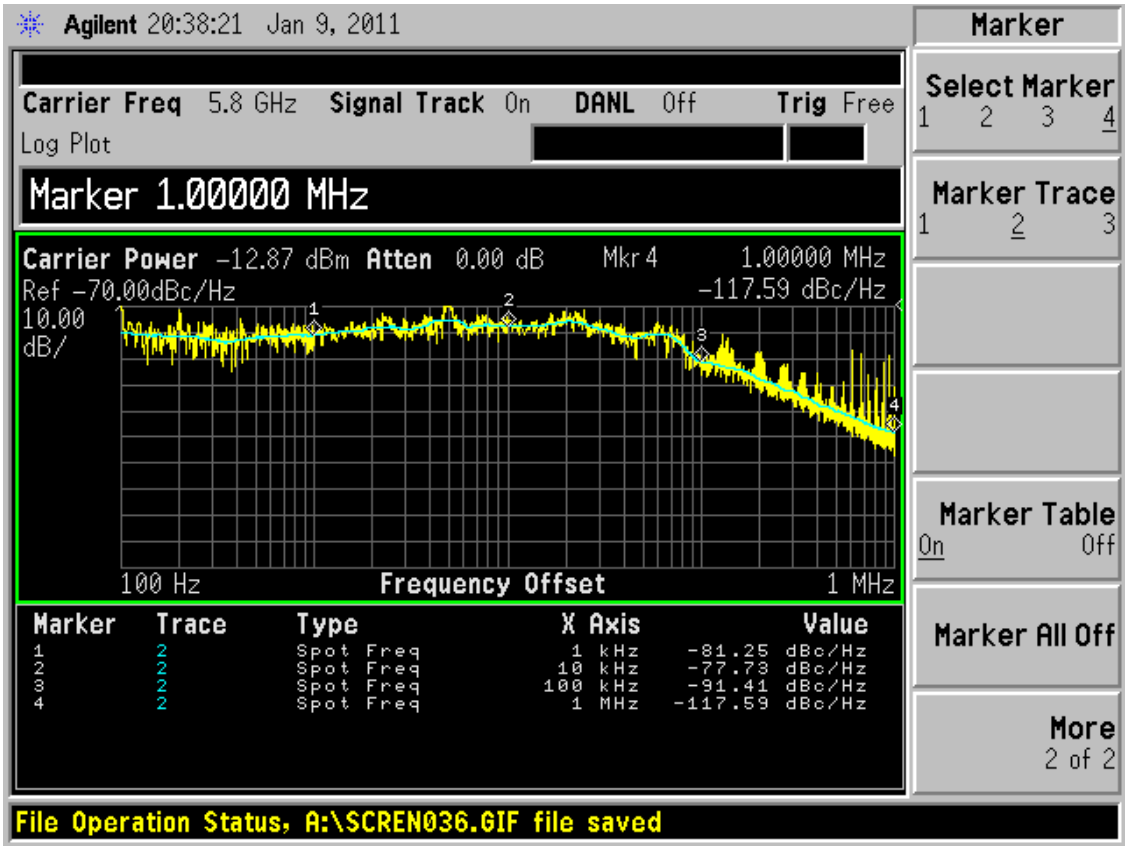

Figure 7 Phase Noise Spectrum and Table of -13dBm@5.8GHz

The testing results are shown in the table as below.

RF Output Frequency / MHz	RF Output Power / dBm	Frequency Offset / @kHz	Phase Noise / dBc/Hz
5800	-13	**1**	-81.25
		10	-77.73
		100	-91.41
		1000	-117.59

Table2 Phase Noise Table of -13dBm@5.8GHz

The simulation results of ADIsimPLL V3.30 are below.

PLL Chip is ADF4106

VCO is V940ME03

Reference is custom

Loop Filter designed at a VCO frequency of 5.80GHz with a Kv of 105MHz/V

Frequency Domain Analysis of PLL

Analysis at PLL output frequency of 5.8GHz

Phase Noise Table

Freq	***Total***	***VCO***	***Ref***	***Chip***	***Filter***
100	*-84.19*	*-146.1*	*--*	*-84.19*	*-136.7*
1.00k	*-87.20*	*-126.1*	*--*	*-87.21*	*-116.7*
10.0k	*-86.44*	*-106.4*	*--*	*-86.87*	*-97.08*
100k	*-90.60*	*-103.8*	*--*	*-92.37*	*-96.02*
1.00M	*-125.3*	*-127.0*	*--*	*-137.8*	*-131.2*

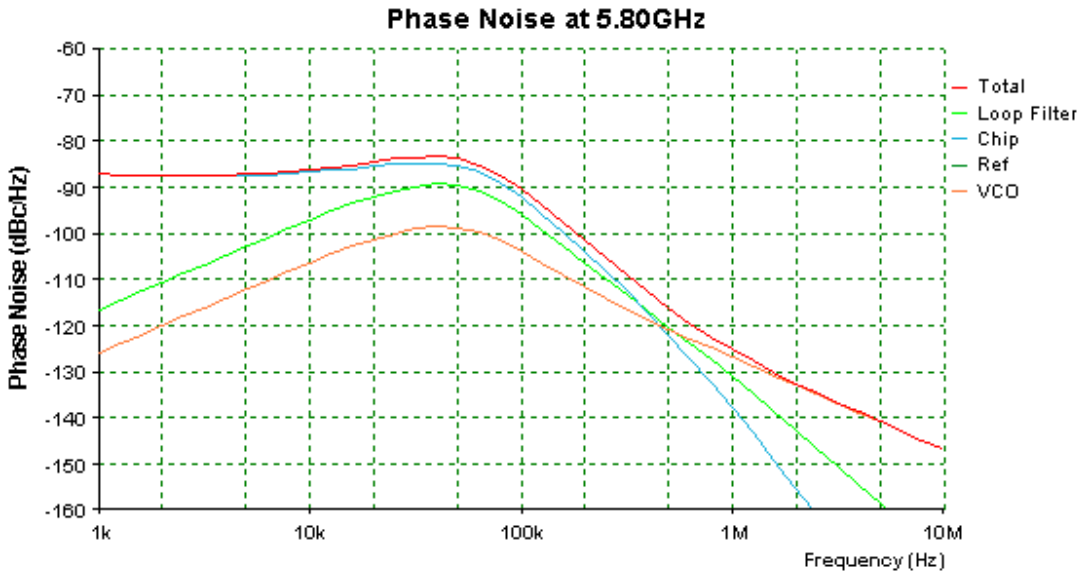

Figure 8 Simulation Results of Phase Noise Spectrum of -13dBm@5.8GHz by ADIsimPLL V3.30

7.2 Lock Time

The lock time of EVAL-ADF4106EB1 is tested. The frequency hopping is from 5.85GHz to 5.8GHz with the loop bandwidth of 50 kHz. The result is as below.

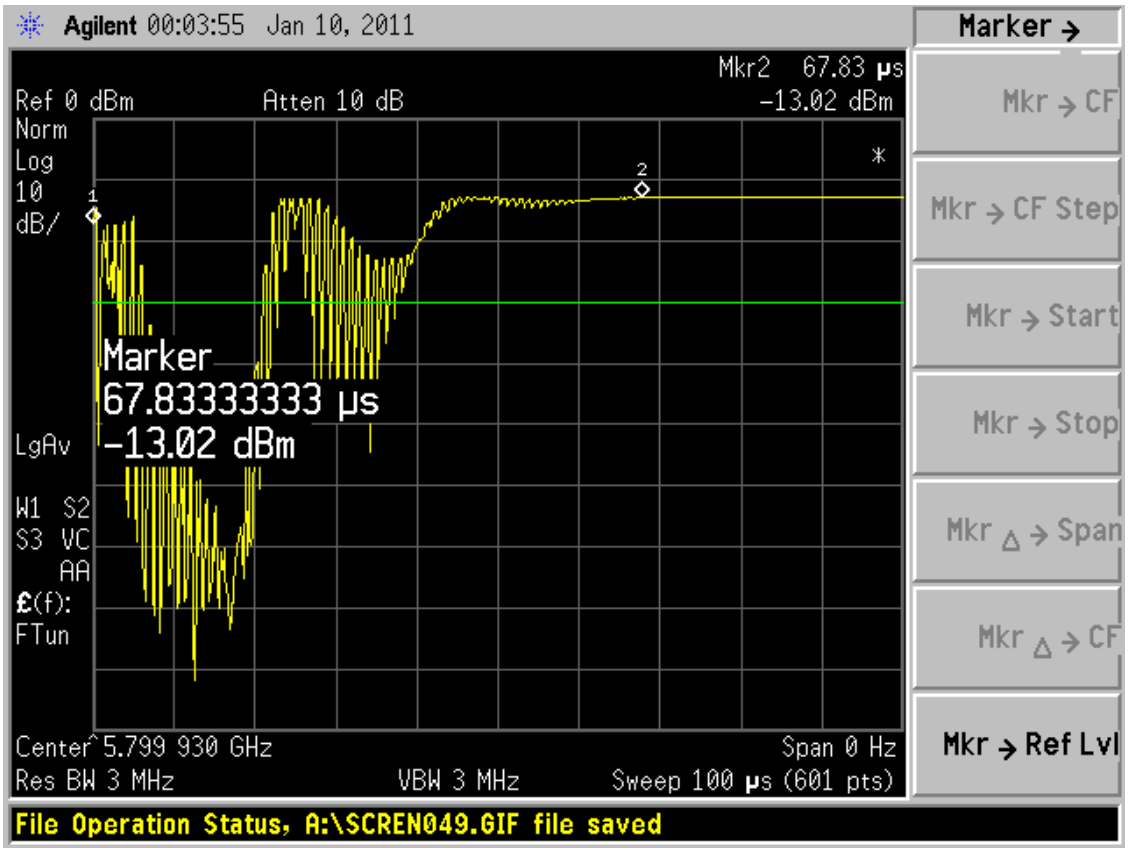

Figure 9 Lock Time of frequency hopping from 5.85GHz to 5.8GHz with Icp of 2.5mA

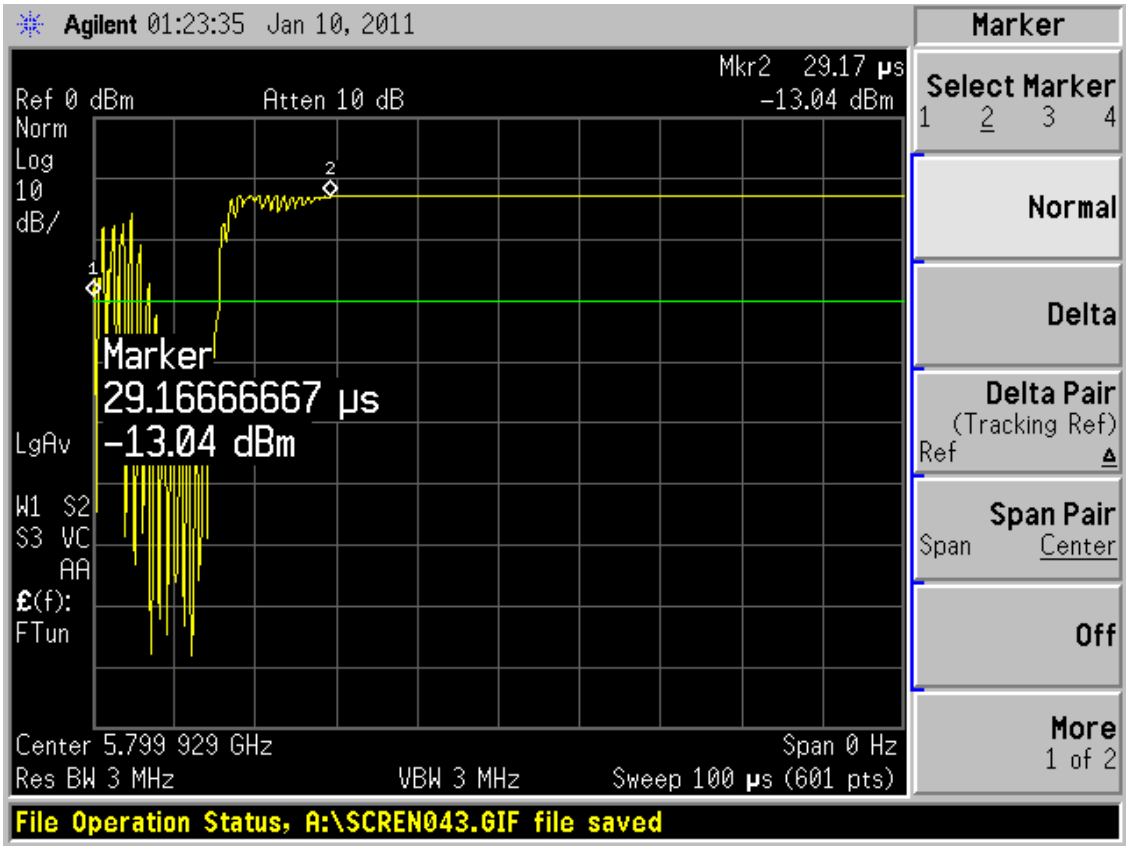

Figure 10 Lock Time of frequency hopping from 5.85GHz to 5.8GHz with Icp of 5.0mA

The simulation results of ADIsimPLL V3.30 are below.

Frequency Locking

Time to lock to 1.00 kHz is 63.5us

Time to lock to 10.0 Hz is 85.4us

Phase Locking (VCO Output Phase)

Time to lock to 10.0 deg is 54.2us

Time to lock to 1.00 deg is 65.3us

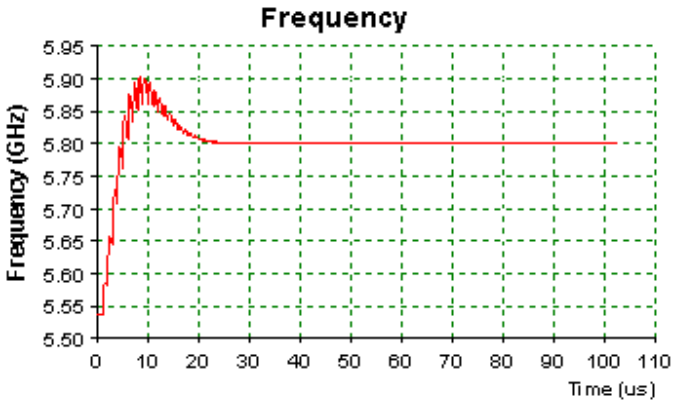

Figure 11 Simulation Results of Lock Time by ADIsimPLL V3.30

7.3 Testing Conclusion

From the testing results, the performance of phase noise and spur is the same as it declared in the user guide of EVAL-ADF4106EB1. It is said in the user guide that typical phase noise performance of -81dBc/Hz @ 1kHz offset. But the testing results are worse than the simulation results. The testing result of lock time is approximately equal to the simulation result. Bigger Icp has faster lock time.

8. Matters Need Attention in the Test and Use of DUT

1. After entering the EVB software, it is also needed to set the EVB mode. Click in the dialogue box of “Evaluation Board” in the main panel.

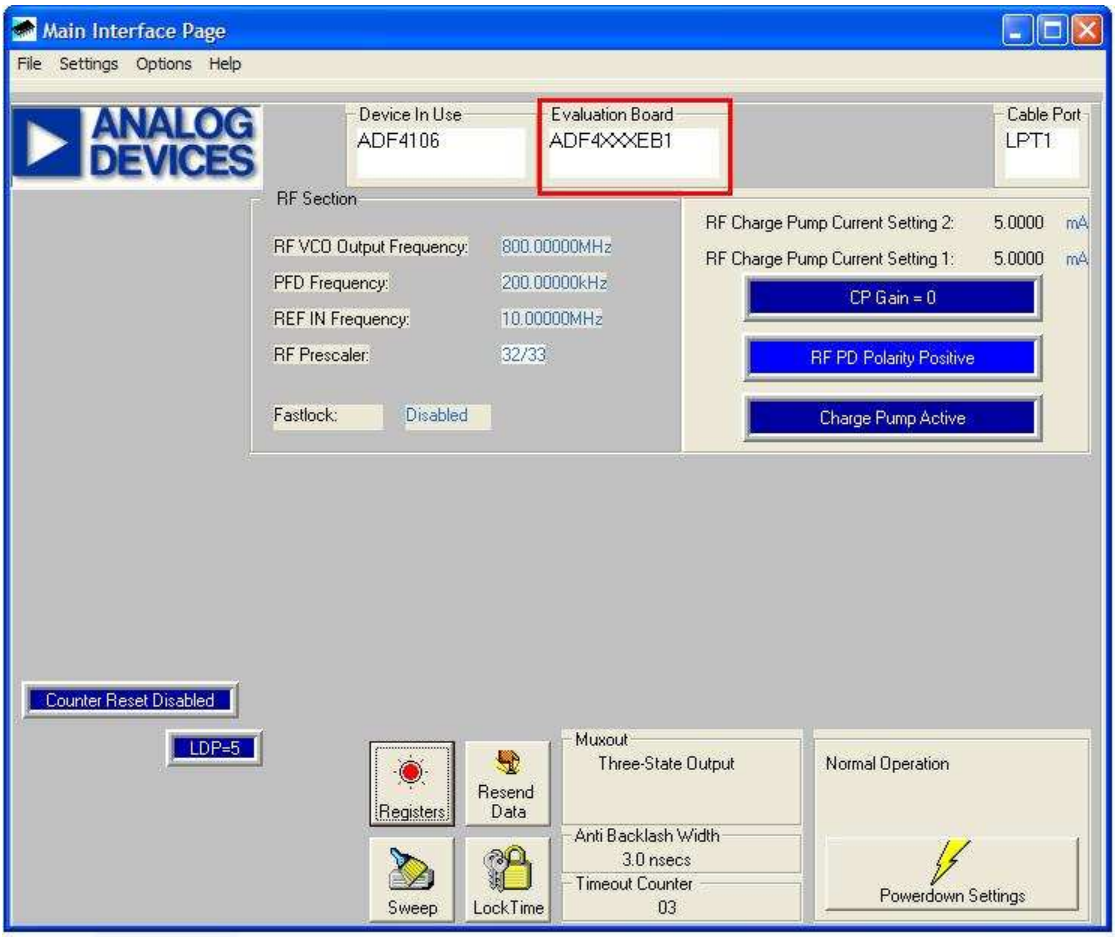

Figure 12 Evaluation Board Selections in the Main Panel

Select “ADF4106EB1” in the popup dialog box.

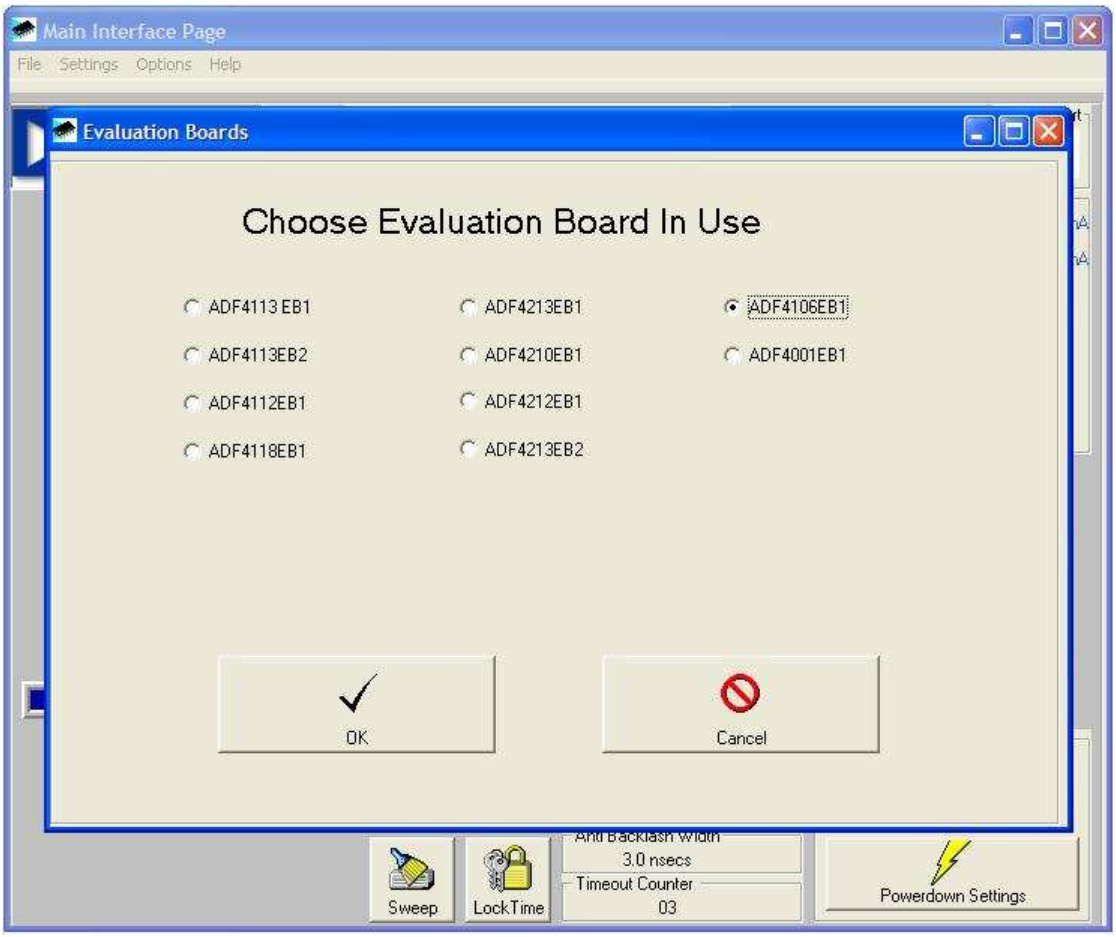

Figure 13 Evaluation Board Selections in the Popup Dialogue Box

The EVAL-ADF4106EB1 is shown in the main panel. The EVB board can be controlled by the EVB software.

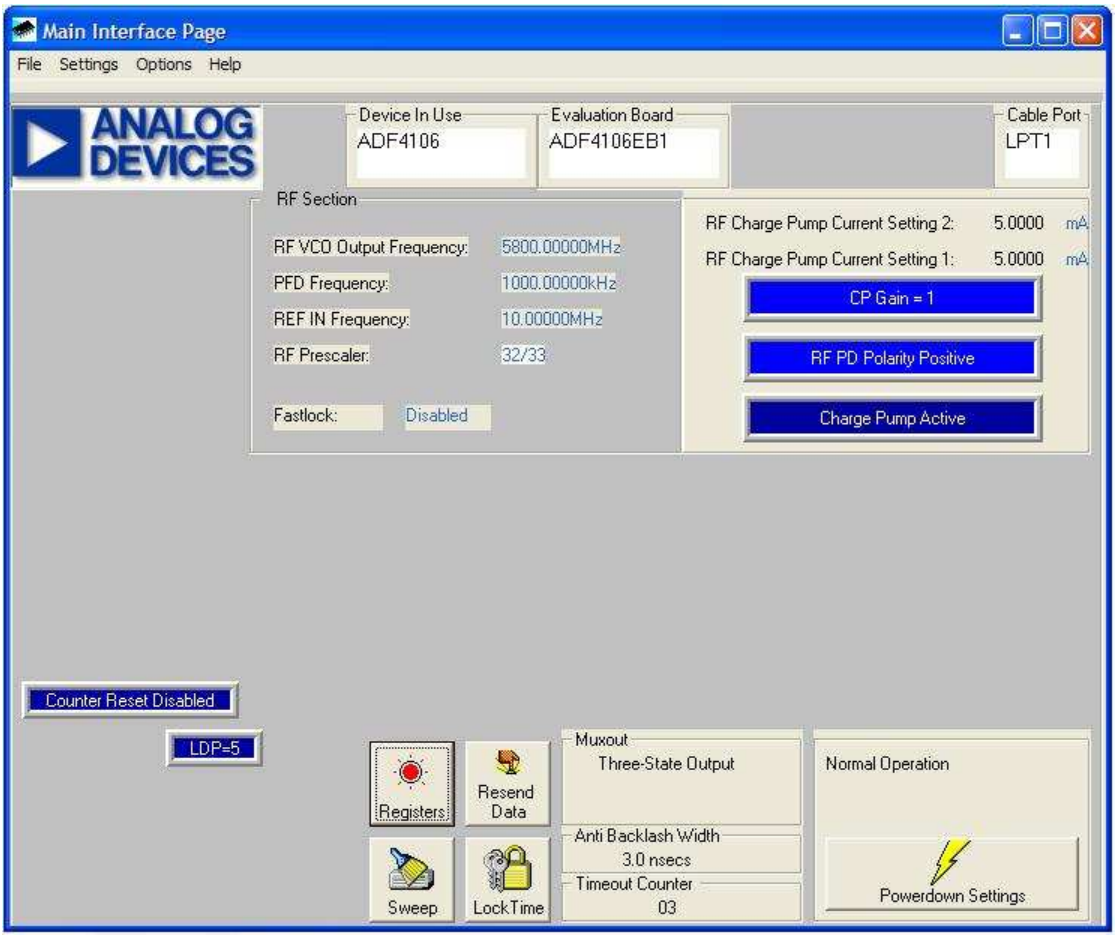

Figure 14 Evaluation Board Selections Shown in the Main Panel

2. After setting the parameters in the EVB software, it is needed to press “Register” button to refresh the values in the registers and get the right output.

9. Testing Report Modified Records

Date	Modified Reasons	Author
2011/01/20	Draft	Yu Qin

(Date is in the format of yy/mm/dd)

10. Reference Materials

1. ADF4106 Datasheet, Analog Devices Inc., Rev C
2. LMDS Evaluation Board For PLL Frequency Synthesizer, REV. PrB 01/03, Analog Devices Inc., 1999
3. Ask the Applications Engineer—30, Adrian Fox, Analog Dialogue 36-03, Analog Devices Inc., 2002

11. Abbreviations