AN66444

PSoC® 3 and PSoC 5 Correlated Double Sampling to Reduce Offset, Drift, and Low Frequency Noise

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Abstract

The implementation of correlated double sampling (CDS) in PSoC® 3 and PSoC 5, for DC offset cancellation and noise reduction is explained in this Application Note. This method reduces low frequency (1/f) noise and nulls DC offset in slow-changing analog signals. AN66444 provides a brief introduction to CDS and details of its implementation in PSoC 3 and PSoC 5. For theory of the CDS technique, see AN2226 - PSoC® 1 - Correlated Double Sampling for Thermocouple Measurement.

Introduction

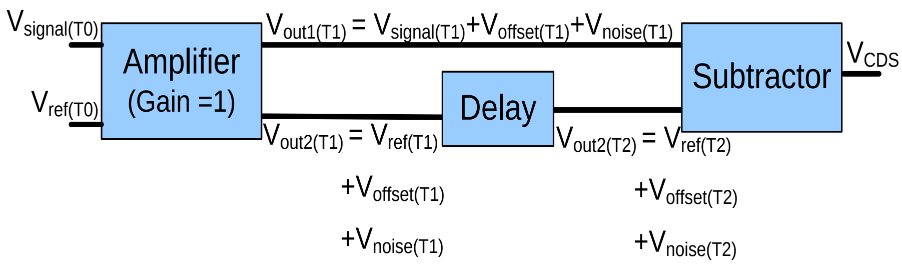
Correlated double sampling (CDS) is a signal processing technique used to suppress the low-frequency (1/f) noise and null any offset. The 1/f noise is inherent in any semiconductor device and cannot be eliminated. Only the effect on the signal can be reduced. CDS acts similarly to a high-pass filter for noise, thus suppressing the low-frequency noise and nulls DC noise (offset). This technique is applicable to slow-changing low-amplitude signals, such as the output of thermocouple, hall-effect, and capacitive sensors. Because the low amplitude signals can be over shadowed by the noise and offset, it is important to eliminate them.

Correlated Double Sampling

When measuring small signals, the limiting factors of a system are the non-ideal characteristics of the devices such as noise and offset. Consider a signal (V_{signal}) to be measured and processed in a system. When it passes through opamp based devices such as amplifiers, undesired offset (V_{offset}) and noise (V_{noise}) are added to it. To get the desired signal, a processing technique such as CDS is applied. CDS is implemented by subtracting a reference signal at the output of the amplifier from the desired (input) signal that is passed through the same amplifier.

Figure 1 represents CDS as a block diagram. The opamp based device is shown as an amplifier. The amplifier adds noise and offset to the signal. Both desired and reference signal pass through the same amplifier after a delay is added to one of the paths. The delay block can also be placed before or after the amplifier stage, resulting in the same output. The reference is then subtracted from the signal to eliminate offset and reduce noise.

Figure 1. Block Diagram for CDS



Based on Figure 1, the signals at the input of the subtractor are as follows:

$$V_{out1(T1)} = V_{signal(T1)} + V_{offset(T1)} + V_{noise(T1)}$$
$$V_{out2(T2)} = V_{refl(T2)} + V_{offset(T2)} + V_{noise(T2)}$$

Equation 1

In these equations:

- Signal and reference do not change between T1 and T2. This is due to the assumption of slow-changing signal and definition of reference, respectively. Therefore, the timestamp is dropped during their subtraction.
- Offset does not change in the short time considered. Thus it is canceled out when the two signals are subtracted.
- Noise due to the system changes with time, thus CDS has an effect on the noise, as shown in Equation 2.

$$V_{CDS} = V_{out1(T1)} - V_{out2(T2)} = (V_{signal} - V_{ref}) + (V_{noise(T1)} - V_{noise(T2)})$$

Equation 2

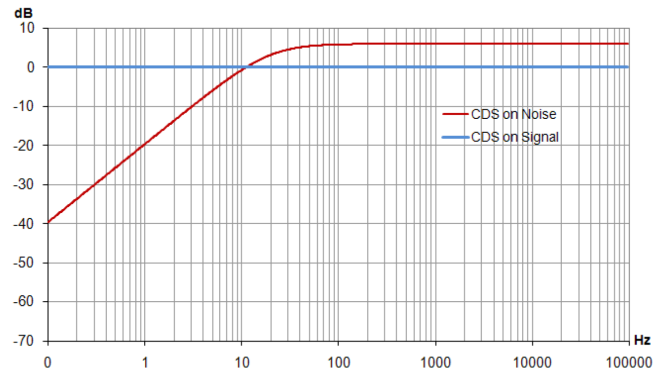
The above equation is in time-domain. The frequency-domain equivalent response of the system is provided in AN2226 and is shown in Equation 3.

$$\boldsymbol{V_{CDS} = V_{signal} - V_{noise}\left(\frac{2s}{s + 2f_{SAMPLE}}\right)}$$

Equation 3

Figure 2 shows the frequency response of CDS on noise and signal based on Equation 3. It can be observed that the frequency response of CDS on noise is equivalent to a high-pass filter and does not have any effect on the signal. This reduces low-frequency noise such as 1/f noise.

Figure 2. Frequency Response of CDS on Signal and Noise



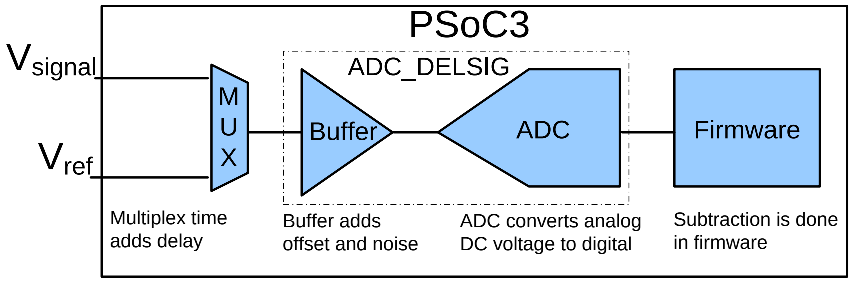
When high-frequency noise has to be eliminated along with the low-frequency noise, CDS has to be followed by an infinite impulse response (IIR) filter.

Implementation in PSoC 3 and PSoC 5

The implementation of CDS can be done in different devices in different ways. For example, CDS can be implemented with a sample and hold circuit, followed by a subtractor.

In PSoC 3 and PSoC 5, the most widely applicable method is the shown in Figure 3. The multiplexer routes the desired signal and reference signal into the system, one after the other. Thus the sampling time between the two signals acts as the delay. The input buffer of the ADC adds the undesired offset and noise. The source of offset and noise can be a result of multiple devices in the signal path; the buffer is just an example. It is important to make sure that the reference signal also follows the same path.

Figure 3. Block Diagram of CDS Implementation in PSoC 3



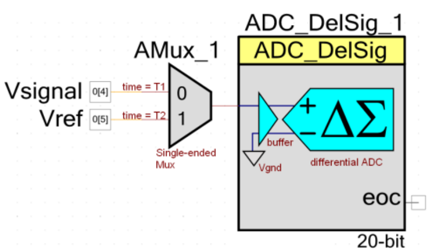
The analog to digital converter (ADC) is used to convert the input and reference signals into the digital domain. These values are then accessed and subtracted in firmware.

The ADC in PSoC 3 and PSoC 5 can be set up as a single ended or a differential ADC. Inherently it is a differential mode ADC. When setup as single ended, the second input is connected to the internal ground. CDS can be performed for both modes of ADC.

CDS with Single-Ended ADC

Figure 4 shows the connections for CDS implementation.

Figure 4. Schematic for CDS with Single-Ended ADC



Equation 4 is based on Figure 4. The multiplexer output is connected to V_{signal} at T1 and to V_{ref} at T2. V_{out1} and V_{out2} are the corresponding outputs of ADC.

$$V_{out1} = \left(V_{signal(T1)} - V_{gnd(T1)}\right) + V_{offset(T1)} + V_{Noise(T1)}$$

$$V_{out2} = \left(V_{ref(T2)} - V_{gnd(T2)}\right) + V_{offset(T2)} + V_{Noise(T2)}$$

Equation 4

Based on the facts stating for Equation 2, the offset is canceled as follows:

$$V_{cds} = \left(V_{signal} - V_{ref}\right) + V_{Noise(T1)} + V_{Noise(T2)}$$

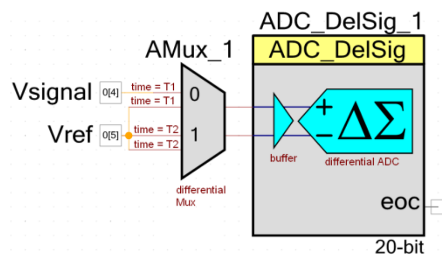
Equation 5

This is assuming that the V_{gnd} is constant, but Vgnd adds some additional noise as shown later. It can be observed that Equation 5 is same as Equation 1, signifying that CDS is achieved with both single ended and differential ended ADC. If the system is required to be single ended and Vsignal is desired at the output, the reference signal can be ground.

CDS with Differential ADC

Figure 5 shows the connections when the ADC is in differential mode.

Figure 5. Schematic for CDS with Differential ADC



The multiplexer is connected to V_{signal} and V_{ref} during T1 and V_{ref} and V_{ref} during T2. Based on these connections, the corresponding ADC outputs are provided in Equation 6.

$$V_{out1} = \left(V_{signal(T1)} - V_{ref(T1)}\right) + V_{offset(T1)} + V_{Noise(T1)}$$

$$V_{out2} = \left(V_{ref(T2)} - V_{ref(T2)}\right) + V_{offset(T2)} + V_{Noise(T2)}$$

Equation 6

$$V_{cds} = \left(V_{signal} - V_{ref}\right) + V_{Noise(T1)} + V_{Noise(T2)}$$

Equation 7

Thus CDS can be achieved with ADC in both the configurations. Theoretically, the implementations lead to the same result, but practically, the differential ADC is more accurate. This is due to the noise effect of the internal V_{gnd} signal. The graph for the comparison is provided in the "results" section.

IIR Filter

To decrease the noise effect further, the CDS implementation is followed by an IIR filter. The implementation of the IIR filter is based on "Single-Pole IIR Filters: To Infinity And Beyond - AN2099". In the IIR filter implementation, the weighted sum of the previous accumulated value and the current value provides the output. For example, if the step size of the filter is IIR_STEP, then the IIR filter output is provided by Equation 8.

$$V_{IIR\_Acc} = V_{IRR\_Curr} * \frac{1}{\mathrm{IIR\_STEP}} + V_{IIR\_Acc} * \frac{(1 - \mathrm{IIR_{STEP}})}{\mathrm{IIR\_STEP}}$$

Equation 8

Firmware for CDS

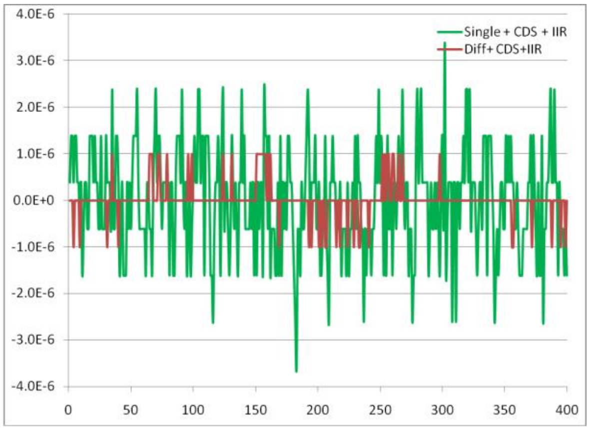
The firmware implementation for the two modes remains the same. The two signals are selected using the multiplexer (AMux) and measured by ADC (ADC_DelSig). The multiplexing of the signals adds the delay required between the signal and reference. The V_{out1} and V_{out2} samples mentioned in the firmware correspond to Equation 4 and Equation 6 in single-ended and differential setup, respectively. These samples are then subtracted to obtain V_{cds}. The IIR filter is implemented based on Equation 8. To avoid floating-point path, shifts are used to get the equivalent of division. A shift right by 1 is equivalent to division by 2. The output can then be used in the firmware or displayed as a result.

```
/*AMUX selections*/
#define Select_Single 0
#define Select_Reference 1

/*IIR Filter parameters*/
#define IIR_FILTER_STEP 16
#define IIR_SHIFT 4
void main()
{
int32 iVout1, iVout2, iVcds;
 for(;;)
 {
 iVcds_acc = 0;
 for(iLoop =0; iLoop < IIR_FILTER_STEP;
iLoop++)
 {
/*Get the first sample Vout1*/
   AMux_1_Select(0);
   ADC_DelSig_1_StartConvert();
  ADC_DelSig_1_IsEndConversion(ADC_DelSig_
  1_WAIT_FOR_RESULT);
   iVout1 = ADC_DelSig_1_GetResult32();
   ADC_DelSig_1_StopConvert();

/*Get the second sample Vout2*/
  AMux_1_Select(1);
  ADC_DelSig_1_StartConvert();
  ADC_DelSig_1_IsEndConversion(ADC_DelSig_1
  _WAIT_FOR_RESULT);
  iVout2 = ADC_DelSig_1_GetResult32();
  ADC_DelSig_1_StopConvert();

/*perform CDS*/
  iVcds = iVout1 - iVout2;

/* IIR Filter*/
  iVcds_curr = iVcds;
  iVcds_acc += (iVcds_curr - iVcds_acc) >>
4;
  }
}
}
```

Results

The output of the system, after CDS and IIR filter, is streamed out through UART. Figure 4 compares the CDS+IIR implementation with single-ended ADC to that with differential ADC. The error with single-ended ADC is higher than that with differential ADC. The error in CDS with single-ended ADC was ±2.5 µV more than differential ADC.

Figure 6. CDS + IIR of Single-Ended Versus Differential ADC



Summary

CDS is used in slow-changing low-amplitude signal measurement to eliminate low-frequency noise and offset. The implementation in PSoC 3 can be performed in single-ended or differential mode ADC. Due to the inherent configuration of ADC, implementing CDS with ADC in differential mode is the best option.

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**	3130827	YARA	01/07/2011	New Spec.
*A	3444871	YARA	12/01/2011	Template update Title updated to show the use of CDS Highlighting PSoC 5 along with PSoC 3 Minor text changes

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