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To: Ramtron Sales
From: Craig Taylor
Subject: Radiation and FRAM

Many of your customers have asked about the susceptibility of FRAM memory to external electromagnetic fields, and radiation in general.

The ferroelectric material we use is PZT (Lead (Pb) Zirconate (Zr) Titanate (Ti) with some Oxygen (O)). The term ferroeletric refers to a property of the material such that if you plot Q (Charge) vs. V (Voltage) for these materials in a varying electric field the result is a hysterisis loop. It behaves like Iron in the domain of electricity and is therefore called a ferroelectric. We all believe that this is a misnomer but we are stuck with it (just like we're stuck with current going the wrong way). There is no Iron in Lead Zirconate Titanate and therefore FRAM memories are undisturbed by external magnetic fields.

Our ferroelectric memories store state not charge and therefore they are very tolerant to radiation, and ionic bombardment. FRAM memories are fabricated on standard CMOS processes and the effects of radiation on the transistors are, as you would expect from other CMOS integrated circuits. The data, however, is stored as state in the ferroelectric film and is not disturbed even under relatively high-energy conditions.

We have periodically provided product when requested for radiation testing. Attached are results on total dose, low energy heavy ion and high-energy heavy ion done by the Defense Research Establishment Ottawa (DREO). Attached also are the results of radiation tests done by VH&S in Germany.

We are always willing to supply product free of charge to anyone that wishes to do additional experiments. We only ask that they share the data with us.

vH&S vonHOERNER&SULGER
FORSCHUNG • RAUMFAHRT • INDUSTRIE

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Ramtron International Corp.
attn. Michael Alwais
Director of Product Marketing
1850 Ramtron Drive
Colorado Springs, CO 80921
U.S.A.

Ihr Zeichen	Ihre Nachricht vom	Unser Zeichen	Schwetzingen, den
		HE/dj	Dec. 2, 1996

FRAM Radiation Test

Dear Mr. Alwais,

appended please find the outcome of our radiation tests at ESTEC. The results were so promising, that the ESTEC people kept all components and the test setup for further heavy-ion tests in Belgium, under power-up condition.

The opinion was, that the main problem of data retention might be *not* necessarily the physics of bit storage (e. g. ferroelectric principle), but the rest of CMOS circuitry, which might degrade earlier than the RAM cells, rendering the stored data useless. Another problem could arise in powered operation, where a single-event upset (SEU) could occur in the CMOS control, so that FRAM cells are *programmed*, even if they are pretty rad-hard. That is the reason, why the FRAMs should be also checked with power supply on. At least without bias, everything works quite well, as you can see from the memo.

As soon as I have any more results, you will be notified.

Sorry, it was not possible to include XICOR EEPROMs, since they arrived too late, on last Tuesday.

Best Regards

H. Henkel

Dr.-Ing. Hartmut Henkel

encl:
Memo (5 pages)

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Total Dose Radiation Tests at FRAM Non-Volatile Memories

vH&S-Internal Memo

1 Introduction

The radiation tests at ferroelectric RAMs of company RAMTRON as described in this text, were done as a small-scale activity during design phase of the COSIMA/ROSETTA space experiment.

The author would like to thank very much ESTEC personnel for making these tests possible, and for their friendly and active support as well as fruitful discussions.

Many thanks also to RAMTRON, who kindly provided the gratuitous FRAM devices.

1.1 Disclaimer

No warranty can be given for correctness of any figure or result. The results might not be useful at all.

2 Test Description

2.1 Test type

Total ionizing dose at unbiased components.

2.2 Location

Tests were performed with the Co^{60} γ-ray source at ESTEC, Noordwijk, The Netherlands.

2.3 Tested items

- 6 devices RAMTRON FRAM, type FM24C04-C, 512×8 bit (device 1...6)
- 5 devices RAMTRON FRAM, type FM24C16-C, 2048×8 bit (device 7...11)

(Lot numbers of packages currently not available.) All packages: Ceramic DIP-8. Devices are numbered from 1 to 11 by binary-coded scratches (×) at pin 1 (MSB)...pin 4 (LSB), e.g.:

pin:	1	2	3	4	
scratch:				×	= device no. 1
scratch:	×		×	×	= device no. 11

2.4 Test setup

For electrical measurements and programming/readout, devices are plugged into a socket on a hand-wired I^2C-bus breadboard interface, which in turn is connected by flatband cable to a parallel-port I/O board within a PC. The power supply (+5V) of the interface board comes from the PC. The power supply to the FRAM can be switched on and off by one PNP-transistor, controlled by software through one parallel output port line. Other parallel port lines handle the SCL and SDA signals. The FRAM supply current is monitored by a digital multimeter, range 0.0...200.0 μA, display step 0.1 μA.

The power on/off, as well as various read/write/verify functions are controlled by a program, which also emulates an I^2C bus master. This is written in C, and runs under MS-DOS on a 286 AT-PC.

The SCL clock frequency is about 3600 Hz for FRAM writing, and 6800 Hz for reading/verify.

2.5 Electrical test sequence

The test steps are performed on the FRAM devices in the following sequence, with steps omitted sometimes:

1. Measure standby supply current, no SCL/SDA activity
2. Verify device contents by bulk reading once
3. Bulk read device once into file (only if error occured during verify)
4. Repeatedly bulk read device, measure supply current
5. Repeatedly bulk write device with same random test pattern from file, measure supply current
6. Repeatedly bulk write device with changing random test pattern, measure supply current
7. Bulk write device once with random test pattern from file
8. Verify device contents by bulk reading once

2.6 Test pattern

For FRAM write/verify, one fixed pseudo-random data pattern is generated and written to a file before the tests. This same file is read in by the test program, and used in test steps 2, 5, and 7. In these cases, every FRAM bit is always (re)programmed to the same value, even if programming is done repeatedly. A changing pseudo-random bitpattern is used for test step 6. In this case, each FRAM bit changes with probability of about 0.5 with every programming run during repeated bulk write.

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3 Measurements

In the tables below, the dash (–) in an entry denotes, that the corresponding operation/measurement was not done. Readout/verify was avoided at most devices in intermediate dose levels, since by readout also the RAM contents would have been refreshed (due to the FRAM working principle). This would have disturbed the data retention result at the final total dose.

The current figures I_{supply} during writing and readout are depending on the SCL clock frequency, which was constant for all measurements.

3.1 Measurements before exposure

Total Dose = 0.0 kRad (Si)
Date: 24.11.96, Time: 16:30

Device No.	Step 1 I_{supply} μA	Step 2 Bit-Errors	Step 3	Step 4 I_{supply} μA	Step 5 I_{supply} μA	Step 6 I_{supply} μA	Step 7,8 Bit-Errors
1	9.4	0	–	13.0	11.3	11.4	0
2	9.4	0	–	13.0	11.3	11.4	0
3	9.4	0	–	12.9	11.3	11.4	0
4	9.4	0	–	13.0	11.4	11.4	0
5	9.4	0	–	13.0	11.4	11.4	0
6	9.1	0	–	12.8	11.1	11.2	0
7	0.1	0	–	11.3	9.9	9.9	0
8	0.2	0	–	11.4	9.9	9.9	0
9	0.1	0	–	11.3	9.8	9.8	0
10	0.1	0	–	11.4	9.8	9.8	0
11	0.1	0	–	11.4	9.8	9.8	0

3.2 Measurements after exposure with 10 kRad (Si) over 15 h time

Total Dose = 10 kRad (Si)
Date: 26.11.96, Time: 9:45

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Device No.	Step 1 I_{supply} μA	Step 2 Bit-Errors	Step 3	Step 4 I_{supply} μA	Step 5 I_{supply} μA	Step 6 I_{supply} μA	Step 7,8 Bit-Errors
1	9.6	0	–	13.1	11.5	11.6	0
2	9.3	–	–	–	–	–	–
3	9.4	–	–	–	–	–	–
4	9.4	–	–	–	–	–	–
5	9.4	–	–	–	–	–	–
6	9.1	–	–	–	–	–	–
7	0.1	0	–	11.4	9.9	10.0	0
8	0.2	–	–	–	–	–	–
9	0.1	–	–	–	–	–	–
10	0.1	–	–	–	–	–	–
11	0.1	–	–	–	–	–	–

3.3 Measurements after additional exposure with 9.83 kRad (Si) over 4 h time

Total Dose = 19.83 kRad (Si)
Date: 26.11.96, Time: 16:10

Device No.	Step 1 I_{supply} μA	Step 2 Bit-Errors	Step 3	Step 4 I_{supply} μA	Step 5 I_{supply} μA	Step 6 I_{supply} μA	Step 7,8 Bit-Errors
1	9.8	–	–	–	–	–	–
2	9.8	0	–	13.4	11.8	11.8	0
3	9.7	–	–	–	–	–	–
4	9.7	–	–	–	–	–	–
5	9.7	–	–	–	–	–	–
6	9.7	–	–	–	–	–	–
7	0.1	–	–	–	–	–	–
8	0.2	0	–	11.5	10.0	10.0	0
9	0.1	–	–	–	–	–	–
10	0.1	–	–	–	–	–	–
11	0.1	–	–	–	–	–	–

3.4 Measurements after additional exposure with 20.11 kRad (Si) over 15 h time

Total Dose = 39.94 kRad (Si)
Date: 27.11.96, Time: 10:00

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Device No.	Step 1 I_{supply} μA	Step 2 Bit-Errors	Step 3	Step 4 I_{supply} μA	Step 5 I_{supply} μA	Step 6 I_{supply} μA	Step 7,8 Bit-Errors
1	13.0 (–)	0	–	17.3	15.5	15.4	0
2	12.2 (12.9)	0	–	15.9	14.2	14.2	0
3	12.5 (13.5)	0	–	16.6	14.8	14.8	0
4	12.1 (12.9)	0	–	16.1	14.2	14.2	0
5	12.5 (13.6)	0	–	16.5	14.7	14.7	0
6	14.2 (16.5)	0	–	19.0	17.1	17.0	0
7	0.1	0	–	11.5	10.0	10.1	0
8	0.2	0	–	11.5	10.1	10.1	0
9	0.1	0	–	11.4	9.9	10.0	0
10	0.1	0	–	11.6	10.1	10.1	0
11	0.1	0	–	11.6	10.1	10.1	0

The current figures in brackets above, step 1, give the initial supply current after power-on. The quiescent supply current went down to the values not in brackets within 1...2 minutes. A reason for this effect, which was only observed at this total dose level, might be some trapped charge due to ionization, shifting threshold levels. This charge slowly diffuses after power-on. This effect could only be seen at the 512×8 bit FRAMs.

4 Short Result Summary

All devices were fully operational after irradiation with total dose 39.94 kRad (Si). No single bit error occured at any device.

Regarding supply current, the 2048×8 bit FRAMs were much less influenced by radiation than the 512×8 bit devices.

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Date: Nov. 30, 1996

Jan 29, 1992
Experiment: Exposure of FMx 1208 256x4 SRAM

Source: Mevex Linac

1) Device #7

- in this test we will subject the DUT to a single pulse and move it gradually move it closer to the source to incease the incident dose rate.
- pulse width from linac = 2.2 us

Distance (m)	Errors	Fill Pattern	TLD #	Dose Rate (Rad/s)
1.00	0	0101	8	9.81E+07
0.75	0	0101	9	1.94E+08
0.50	0	0101	10	5.25E+08
0.40	0	0101	11	6.62E+08
0.30	0	0101	12	8.48E+08
0.20	0	0101	13	1.72E+09
0.10	0	0101	14	2.61E+09

- the above experiments were performed on a DUT with the cover on I have removed the cover to see if there is an effect.

0.10	0	0101		
- tried two pulses				
0.10	0	0101		
- single pulse				
0.05	0	0101	15	2.74E+09
0.05			16	9.31E+08
- repeated and tried to center better				
0.05	0	0101		

Jan 26, 1992
Experiment: Exposure of FMx 1208 256x4 SRAM

Source: DREO GRM - 750 Co 60
Device: #1
1) Expose at 1m, Dose Rate = 337.32 R/h

Time (secs)	Time (hrs)	Fill Pattern	Upsets	Rads
0		1	0	0
4074	1.13	1	0	381.73
8270	2.30	1	0	774.90
11380	3.16	1	0	1066.31
13464	3.74	1	0	1261.58

- the metal cap on the device was removed to see if there was any contributing factors.

2020	0.56	1	0	189.27
4630	1.29	1	0	433.83
6805	1.89	1	0	637.63
69380	19.27	1	0	6500.91
87970	24.44	1	0	8242.79

2) DUT moved to .581m, Dose Rate = 1000 R/h

67045	18.62	1	0	18623.61
79620	22.12	1	0	22116.67
96284	26.75	1	0	26745.56
230607	64.06	0101	256	64057.50

- the IC was not resetable and would not accept all 1's or all 0's, however, it would allow me to write the checkerboard back in, but the areas for 0's showed error, the areas for 1's were OK. These results were saved in Mosaid Fcrs as follows:

DREO001 = all 0
DREO002 = checkerboard
DREO003 = all 1

- it was obvious from these results that the device had latched.

Jan 27,1992

Source: DREO GB150C Co 60

3) Expose at .718m, Dose Rate = 10000 R/h
Device: #2

Time (mins)	Time (hrs)	Fill Pattern	Upsets	Rads	FCR File
85	1.42	0101	88	14166.67	DREO004

- the device was latched with a latch current of 16.4 mA

4) Device #3, same exposure.

Time (mins)	Time (hrs)	Fill Pattern	Upsets	Rads	FCR File
23	0.38	0101	0	3833.33	
48	0.80	0101	0	8000.00	
98	1.63	0101	274	16333.33	DREO005

- device was latched at 20.32 mA latch current. When DUT powered down then up, current was approximately 5 mA, but device was not operational in either read or write mode.

Note: all latchups were destructive, device did not recover on power down and up. This was probably due to a CMOS latchup. We have seen in the past that an unhardened CMOS can be expected to latch in 1e4 Rad.

Jan 29, 1992
Experiment: Exposure of FMx 1208 256x4 SRAM

Source: Mevex Linac

1) Device #7

Facility: Chalk River Nuclear Labs
Tandem Accelerator SuperConducting Cyclotron

Date: March 2 - 6, 1992

Comparison of High and Low energy data taken at Chalk River TASCC facility for the Ramtron RMx1208 2k x 8 SRAM.

New DUT

DUT RMx 1208 2K x 8 SRAM - device #8

DUT positioned at 0 degrees to beam line.

- as a test of the DUT's sensitivity it was quickly tested at a beam current of .2nA. There were no errors observed, hence, the beam current was moved up to .8nA.

C12I = .8nA

Time (sec)	FCR (CHLK---)	Pattern	Upsets	Fluence (p/cm^2)	Xsect
120		0	0	61239.9	
120		1	0	61239.9	

Rotate the DUT to 60 degrees from incedent beam:

Time (sec)	FCR (CHLK---)	Pattern	Upsets	Fluence (p/cm^2)	Xsect
120	055	0	12	61239.9	1.20E-08
60	056	1	4	30619.9	7.97E-09
120	057	1	4	61239.9	3.99E-09
120	058	0	21	61239.9	2.09E-08
60	059	0	21	30619.9	4.19E-08
30	060	0	21	15310.0	8.37E-08
30	061	1	4	15310.0	1.59E-08

Note: the IC got in a funny state: after the last run, the DUT could be written to with no errors, but when reading back with a straight read there were errors for both the 1 and 0 patterns. When I powered down then up the DUT this phenomena went away and no errors occured with a read. There was no beam coming through during these read observations, also, it appeared that with the beam, the DUT was getting progressively softer until the power down/up point. Also, an analysis of the bit errors showed that it was the same bits corrupting in cases CHLK058 - CHLK060.

- returned the DUT to 0 degrees:

Time (sec)	FCR (CHLK---)	Pattern	Upsets	Fluence (p/cm^2)	Xsect
30		0	0	15310.0	
60		0	0	30619.9	
120		0	0	61239.9	
120		1	0	61239.9	
300		1	0	153099.7	

Rotate DUT to intermediate angle of 45 degrees from incedent beam

Time (sec)	FCR (CHLK---)	Pattern	Upsets	Fluence (p/cm^2)	Xsect
30		0	0	15310.0	
60		0	0	30619.9	
120		0	0	61239.9	
30		1	0	15310.0	
60		1	0	30619.9	
120		1	0	61239.9	

Changed DUT

DUT RMx 1208 2K x 8 SRAM - device #9

C12I = .8nA

Time (sec)	FCR (CHLK---)	Pattern	Upsets	Fluence (p/cm^2)	Xsect
30		0	0	15310.0	
60		0	0	30619.9	
120		0	0	61239.9	
30		1	0	15310.0	
60		1	0	30619.9	
120		1	0	61239.9	

Rotate the DUT to 60 degrees from incedent beam:

Time (sec)	FCR (CHLK---)	Pattern	Upsets	Fluence (p/cm^2)	Xsect
30		0	0	15310.0	
60		0	0	30619.9	
120		0	0	61239.9	
180		0	0	91859.8	

- at this point it seemed there were no errors since the DUT read back data correctly, however, when I attempted to write an all 1's pattern to the DUT it was obvious that the DUT had latched. Powered down/up and DUT recovered.

- DUT still at 60 degrees:

Time (sec)	FCR (CHLK---)	Pattern	Upsets	Fluence (p/cm^2)	Xsect	
30		0	0	15310.0		no latch
60		0	0	30619.9		no latch
120		0	0	61239.9		no latch
180	062	0	4	91859.8	4.25E-08	latch
	063	<- attempt to write all 1's to DUT during latch				
30		1	0	15310.0		no latch
60		1	0	30619.9		no latch
120	064	1	51	61239.9	5.08E-08	latch
	065	<- attempt to write all 0's to DUT during latch				

Note 1: DUT latch current = 129mA
Note 2: all latches were non-destructive.

Rotate DUT to intermediate angle of 45 degrees from incedent beam

Time (sec)	FCR (CHLK---)	Pattern	Upsets	Fluence (p/cm^2)	Xsect	
30		1	0	15310.0		no latch
60		1	0	30619.9		no latch
120		1	0	61239.9		no latch
180		1	0	91859.8		no latch
180	066			0.0		
120		0	11	91859.8	7.31E-09	latch
		0	0	61239.9		no latch

Note: again latch was non-destructive.

Changed DUT

Beam = 110 MeV (127) I LET=48.7, RANGE=15.9um

DUT = Ramtron RMx1208 2k x 8 SRAM - device #9

DUT positioned at 0 degrees to beam line.

Time (sec)	FCR (CHLK---)	Pattern	Upsets	Fluence (p/cm^2)	Xsect
60		0	0	24134.7	
120		0	0	48269.4	
180		0	0	72404.2	
60		1	0	24134.7	
120		1	0	48269.4	
180		1	0	72404.2	

Rotate the DUT to 60 degrees from incedent beam:

Time (sec)	FCR (CHLK---)	Pattern	Upsets	Fluence (p/cm^2)	Xsect
30		0	0	12067.4	
60		0	0	24134.7	
120		0	0	48269.4	
5400		0	0	2.2E+06	
240		1	0	96538.9	

Purpose : The week of Jan 27 - Feb 2, 1995 was procured at the Tandem Accelerator Super Conducting Cyclotron (TASCC) facility as part of a joint Canadian - US showcase experiment for industry. As part of these experiments, several Canadian and US companies participated in a variety of experiments using the very high and low energy ions produced at TASCC.

Experiment: As part of DREOs involvement, we tested the Ramtron FMX1608 in two of the high energy beams produced. The results of these experiments are shown in table one.

Canadian firms involved with these showcase experiments included DREO, Thompson & Nielson, SPAR Aerospace, and the Canadian Space Agency. From the United States, such firms as US Naval Research Laboratory (NRL), NASA, John's Hopkins Applied Physics Lab, Aerospace Corp., Defence Nuclear Agency and US Airforce Rome Labs participated.

Results: The experimental results for the Ramtron FMX1608 (8k x 8) FRAM are summarized in table 1. Briefly, they show clearly that the Ramtron device showed no susceptibility to the ion energies used here. All other industry standard SRAMs/DRAMs either latched, or showed significant upset cross sections using these ion species.

Table 1: Summary of Results

Energy & Ion	LET (Mev/(mg/cm^2))	Range (um)	Fluence (p/cm^2)	Bit Pattern
2 Gev Au	89.7	105.12	139200	1
			121800	0
2 Gev I	45.5	162	301924	1
			504733	0